INTEGRATED CIRCUITS

DATA HANDBOOK

Radio, audio and associated systems Bipolar, MOS TDA1512 to μA758

BOOK IC01b 1990

Philips Components

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RADIO, AUDIO AND ASSOCIATED SYSTEMS
BIPOLAR, MOS
TDA1512 TO μA758
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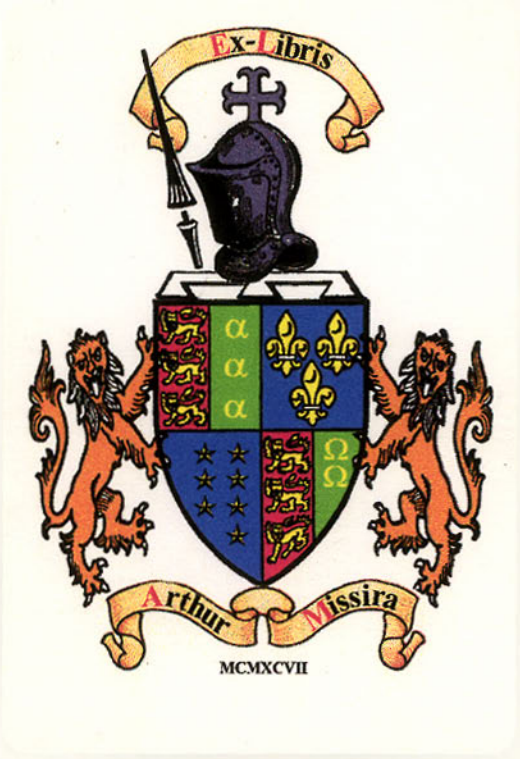
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RADIO, AUDIO AND ASSOCIATED SYSTEMS
BIPOLAR, MOS

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PCA80C51BH-3	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 12 MHz; −40 to + 125 °C	209
PCA80C552	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; −40 to + 125 °C	213
PCA80C562	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2-pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; −40 to + 125 °C	215
PCA80C652	microcontroller; 256 x 8 RAM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; −40 to + 125 °C	217
PCA83C552	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; −40 to + 125 °C	213
PCA83C562	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2-pulse-width modulated signals; 8 multiplexed input lines; 1.2 to 12 MHz; −40 to + 125 °C	215
PCA83C652	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; −40 to + 125 °C	217
PCA83C654	microcontroller; 256 x 8 RAM; 16K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; −40 to + 125 °C	219
PCB80C31BH-3	microcontroller; 128 x 8 RAM; 0.5 to 12 MHz; 0 to +70 °C	209
PCB80C31BH-3	microcontroller; 128 x 8 RAM; 1.2 to 16 MHz; 0 to +70 oC	209
PCB80C51BH-3	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 0.5 to 12 MHz; 0 to +70 °C	209
PCB80C51BH-3	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 16 MHz; 0 to +70 °C	209

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8051/80C51 family CMOS (continued)		
PCB80C552	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; two pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I²C-bus; 1.2 to 12 MHz; 0 to +70 °C	213
PCB80C562	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; 0 to + 70 °C	215
PCB80C652	microcontroller; 256 x 8 RAM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; 0 to +70 °C	217
PCB80C851	microcontroller; 128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; 0 to + 70 °C	221
PCB83C552	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; two pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I²C-bus; 1.2 to 12 MHz; 0 to + 70 °C	213
PCB83C562	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8 multiplexed input lines; 1.2 to 12 MHz; 0 to +70 °C	215
PCB83C652	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; 0 to +70 °C	217
PCB83C654	microcontroller; 256 x 8 RAM; 16K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; 0 to +70 °C	219
PCB83C851	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; 0 to + 70 °C	221
PCF80C31BH-3	microcontroller; 128 x 8 RAM; 1.2 to 12 MHz; −40 to +85 °C	209
PCF80C51BH-3	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 12 MHz; −40 to +85 °C	209
PCF80C552	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I²C-bus; 1.2 to 12 MHz; −40 to +85 °C	213
PCF80C562	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; −40 to +85 °C	215
PCF80C652	microcontroller; 256 x 8 RAM; serial I/O; UART; I²2C-bus; 1.2 to 12 MHz; −40 to +85 °C	217
PCF80C851	microcontroller; 128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; −40 to + 85 °C	221
PCF83C552	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I²C-bus; 1.2 to 12 MHz; −40 to +85 °C	213

type no.	description	page
PCF83C562	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8 multiplexed input lines; 1.2 to 12 MHz; −40 to +85 °C	215
PCF83C652	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to +85 °C	217
PCF83C654	microcontroller; 256 x 8 RAM; 16K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to +85 °C	219
PCF83C851	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; −40 to +85 °C	221
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PCF84C21	microcontroller; 64 x 8 RAM; 2K x 8 ROM; plus 8-bit LED driver; I²C-bus; −40 to +85 °C	283
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PCF84C41	microcontroller; 128 x 8 RAM; 4K x 8 ROM; plus 8-bit LED driver; I²C-bus; −40 to +85 °C	283
PCF84C42	low cost microcontroller; 64 x 8 RAM; 4K x 8 ROM	285
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MAB8421	microcontroller; 64 x 8 RAM; 2K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; 0 to +70 °C	79
MAB8422	microcontroller; 64 x 8 RAM; 2K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I²C-bus; 1.0 to 6 MHz; 0 to +70 °C	81
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MAF84A22	microcontroller; 64 x 8 RAM; 2K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I²C-bus; 1.0 to 5 MHz; −40 to +110 °C	81
MAF84A41	microcontroller; 128 x 8 RAM; 4K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 5 MHz; −40 to +110 °C	79
MAF84A42	microcontroller; 128 x 8 RAM; 4K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I²C-bus; 1.0 to 5 MHz; −40 to +110 °C	81
MAF84A61	microcontroller; 128 x 8 RAM; 6K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 5 MHz; −40 to +110 °C	79
MAF8411	microcontroller; 64 x 8 RAM; 1K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; −40 to +85 °C	79
MAF8421	microcontroller; 64 x 8 RAM; 2K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; −40 to +85 °C	79
MAF8422	microcontroller; 64 x 8 RAM; 2K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I²C-bus 1.0 to 6 MHz; −40 to +85 °C	81
MAF8441	microcontroller; 128 x 8 RAM; 4K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; −40 to + 85 °C	79
MAF8442	microcontroller; 128 x 8 RAM; 4K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I²C-bus; 1.0 to 6 MHz; −40 to +85 °C	81
MAF8461	microcontroller; 128 x 8 RAM; 6K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; −40 to +85 °C	79
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PCB80C39	microcontroller; 128 x 8 RAM; 1.0 to 15 MHz; 0 to +70 °C	211
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PCF80C39	microcontroller; 128 x 8 RAM; 1.0 to 15 MHz; −40 to +85 °C	211
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TDA7050T	150 mW BTL or 2 x 75 mW stereo audio power amplifier; low voltage	1427
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MAF8421P	microcontroller; 64 x 8 RAM; 2K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; −40 to + 85 °C	79
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PCA80C49WP	microcontroller; 128 x 8 RAM; 2K x 8 ROM; 1.0 to 15 MHz; −40 to + 110 °C	211

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PCA80C51BH-3WP	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 12 MHz; −40 to + 125 °C	209
PCA80C552WP	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I²C-bus; 1.2 to 12 MHz; −40 to + 125 °C	213
PCA80C562WP	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; −40 to + 125 °C	215
PCA80C652P	microcontroller; 256 x 8 RAM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to + 125 °C	217
PCA80C652WP	microcontroller; 256 x 8 RAM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to + 125 °C	217
PCA83C552WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I²C-bus; 1.2 to 12 MHz; −40 to + 125 °C	213
PCA83C562WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8 multiplexed input lines; 1.2 to 12 MHz; −40 to + 125 °C	215
PCA83C652P	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to + 125 °C	217
PCA83C652WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to + 125 °C	217
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PCB80C39P	microcontroller; 128 x 8 RAM; 1.0 to 15 MHz; 0 to + 70 °C	211
PCB80C39WP	microcontroller; 128 x 8 RAM; 1.0 to 15 MHz; 0 to + 70 °C	211
PCB80C49P	microcontroller; 128 x 8 RAM; 2K x 8 ROM; 1.0 to 15 MHz; 0 to + 70 °C	211
PCB80C49WP	microcontroller; 128 x 8 RAM; 2K x 8 ROM; 1.0 to 15 MHz; 0 to + 70 °C	211

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PCB80C51BH-3P	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 0.5 to 12 MHz; 0 to + 70 °C	209
PCB80C51BH-3WP	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 0.5 to 12 MHz; 0 to + 70 °C	209
PCB80C51BH-3P	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 16 MHz; 0 to + 70 °C	209
PCB80C51BH-3WP	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 16 MHz; 0 to + 70 °C	209
PCB80C552WP	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; two pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	213
PCB80C562WP	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; 0 to + 70 °C	215
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PCB80C851WP	microcontroller; 128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; 0 to + 70 °C	221
PCB80C652P	microcontroller; 256 x 8 RAM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	217
PCB80C652WP	microcontroller; 256 x 8 RAM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	217
PCB83C552WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; two pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	213
PCB83C562WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8 multiplexed input lines; 1.2 to 12 MHz; 0 to + 70 °C	215
PCB83C652P	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	217
PCB83C652WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	217
PCB83C654P	microcontroller; 256 x 8 RAM; 16K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	219
PCB83C654WP	microcontroller; 256 x 8 RAM; 16K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	219
PCB83C851P	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; 0 to + 70 °C	221
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PCF80C31BH-3WP	microcontroller; 128 x 8 RAM; 1.2 to 12 MHz; −40 to + 85 °C	209
PCF80C39P	microcontroller; 128 x 8 RAM; 1.0 to 15 MHz; −40 to + 85 °C	211
PCF80C39WP	microcontroller; 128 x 8 RAM; 1.0 to 15 MHz; −40 to + 85 °C	211
PCF80C49P	microcontroller; 128 x 8 RAM; 2K x 8 ROM; 1.0 to 15 MHz; −40 to + 85 °C	211
PCF80C49WP	microcontroller; 128 x 8 RAM; 2K x 8 ROM; 1.0 to 15 MHz; −40 to + 85 °C	211
PCF80C51BH-3P	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 12 MHz; −40 to + 85 °C	209
PCF80C51BH-3WP	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 12 MHz; −40 to + 85 °C	209
PCF80C552WP	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I²C-bus; 1.2 to 12 MHz; −40 to + 85 °C	213
PCF80C562WP	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; −40 to + 85 °C	215
PCF80C652P	microcontroller; 256 x 8 RAM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to + 85 °C	217
PCF80C652WP	microcontroller; 256 x 8 RAM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to + 85 °C	217
PCF80C851P	microcontroller; 128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; −40 to + 85 °C	221
PCF80C851WP	microcontroller; 128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; −40 to + 85 °C	221
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PCF83C552WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I²C-bus; 1.2 to 12 MHz; −40 to + 85 °C	213
PCF83C562WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8 multiplexed input lines; 1.2 to 12 MHz; −40 to + 85 °C	215

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PCF83C652WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to + 85 °C	217
PCF83C654P	microcontroller; 256 x 8 RAM; 16K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to + 85 °C	219
PCF83C654WP	microcontroller; 256 x 8 RAM; 16K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to + 85 °C	219
PCF83C851P	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; −40 to + 85 °C	221
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PCF84C41P	microcontroller; 128 x 8 RAM; 4K x 8 ROM; plus 8-bit LED driver; I²C-bus; −40 to + 85 °C	283
PCF84C41T	microcontroller; 128 x 8 RAM; 4K x 8 ROM; plus 8-bit LED driver; I²C-bus; −40 to + 85 °C	283
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PCF8582AT	256 x 8-bit EEPROM; I^2C-bus; −40 to + 85 °C	481
PCF8583P	clock calendar with 256 x 8-bit static RAM; I^2C-bus	491
PCF8583T	clock calendar with 256 x 8-bit static RAM; I^2C-bus	491
PCF8591P	8-bit ADC/DAC; I^2C-bus	509
PCF8591T	8-bit ADC/DAC; I^2C-bus	509
PNA7509P	7-bit ADC; 22 MHz; 3-state output	527
PNA7518P	8-bit multiplying DAC; 30 MHz	539

type	description	page
SA571F	compandor	95
SA571N	compandor	95
SA572D	programmable analogue compandor	103
SA572F	programmable analogue compandor	103
SA572N	programmable analogue compandor	103
SA5534N	dual and single low noise operational amplifier	135
SA5534AD	dual and single low noise operational amplifier	135
SA5534AN	dual and single low noise operational amplifier	135
SA602D	double balanced mixer and oscillator	143
SA602N	double balanced mixer and oscillator	143
SA602FE	double balanced mixer and oscillator	143
SA604AD	high performance low-power FM IF system	149
SA604AN	high performance low-power FM IF system	149
SA605D	low-power FM IF system	159
SA605F	low-power FM IF system	159
SA605N	low-power FM IF system	159
SA614AD	low-power FM IF system	169
SA614 AN	low-power FM IF system	169
SAA1057	radio tuning PLL frequency synthesizer (SYMO II)	545
SAA1064P	4-digit LED driver; I^2C-bus	555
SAA1099	stereo sound generator for sound effects and music synthesis (μC-controlled)	565
SAA1300	tuner switching circuit; I^2C-bus	581
SAA3004P	high performance transmitter (455 kHz) for infrared remote control; up to 448 commands	585
SAA3004T	high performance transmitter (455 kHz) for infrared remote control; up to 448 commands	585
SAA3006P	high performance transmitter (RC-5) for infrared remote control; up to 2048 commands	595
SAA3007P	high performance transmitter (455 kHz) for infrared remote control; up to 1280 commands; low voltage	609
SAA3007T	high performance transmitter (455 kHz) for infrared remote control; up to 1280 commands; low voltage	609
SAA3008P	high performance transmitter (38 kHz) for infrared remote control; low voltage	623
SAA3008T	high performance transmitter (38kHz) for infrared remote control; low voltage	623
SAA3009P	infrared remote control decoder; decodes 64 commands (RECS80/RC-5); up to 32 subaddresses; high current output capability for direct LED drive	637
SAA3010P	high performance transmitter (RC-5) for infrared remote control; low voltage	647
SAA3010T	high performance transmitter (RC-5) for infrared remote control; low voltage	647
SAA3028	high performance transcoder (RC-5) for infrared remote control; I^2C-bus	663
SAA3049P	infrared remote control decoder, low current version of SAA3009	637

type	description	page
SAA3049T	infrared remote control decoder, low current version of SAA3009	637
SAA7210	decoder for Compact Disc (second generation)	671
SAA7220	digital filter and interpolator for Compact Disc (second generation)	693
SAA7274P	audio digital input circuit (ADIC)	715
SAA7274T	audio digital input circuit (ADIC)	715
SAA7310P	decoder for Compact Disc (third generation)	727
SAA7310GP	decoder for Compact Disc (third generation)	727
SAA7320GP	stereo DAC for Compact Disc	757
SAD7630P	CCD delay line for error correction in video and sound carrier timebases (laservision players)	777
SAF1032P	receiver/decoder for infrared remote control	787
SAF1039P	transmitter for infrared remote control	787
SE5410F	10-bit high-speed multiplying DAC	119
SE5532FE	internally-compensated dual low noise operational amplifier	129
SE5532AFE	internally-compensated dual low noise operational amplifier	129
SE5534N	dual and single low noise operational amplifier	135
SE5534AN	dual and single low noise operational amplifier	135
SE5534FE	dual and single low noise operational amplifier	135
SE5534AFE	dual and single low noise operational amplifier	135
TDA1001B	interference and noise suppression circuit for FM receivers	801
TDA1001BT	interference and noise suppression circuit for FM receivers	801
TDA1010A	6 W audio power amplifier for in-car applications/10 W audio power amplifier for mains-fed applications	811
TDA1011	2 to 6 W audio power amplifier with preamplifier	829
TDA1013B	4 W audio power amplifier with DC volume control	841
TDA1015	1 to 4 W audio power amplifier with preamplifier	849
TDA1015T	0.5 W audio power amplifier with preamplifier	859
TDA1016	2 W recording/playback audio power amplifier with preamplifier, automatic level control, short circuit and thermal protection	865
TDA1020	12 W audio power amplifier with preamplifier for car radios	871
TDA1029	signal-sources switch (4 x two channels)	877
TDA1059B	motor speed regulator with thermal shut-down; multiplication coefficient = 9; drop-out voltage = 1.8 V	891
TDA1072A	AM receiver circuit for hi-fi and car radios	897
TDA1072AT	AM receiver circuit for hi-fi and car radios	913
TDA1074A	dual tandem electronic potentiometer circuit	931
TDA1510	24 W BTL or 2 x 12 W stereo car radio power amplifier	941
TDA1510A	24 W BTL or 2 x 12 W stereo car radio power amplifier	941
TDA1512	12 to 20 W hi-fi audio power amplifier	983
TDA1512Q	12 to 20 W hi-fi audio power amplifier	983
TDA1514A	50 W hi-fi power amplifier for digital audio (e.g. Compact Disc)	989
TDA1515B	24 W or 2 x 12 W stereo car radio power amplifier	997
TDA1516Q	22 W BTL or 2 x 11 W stereo car radio power amplifier; closed loop voltage gain 26 dB	1003
TDA1517	2 x 6 W stereo car radio audio power amplifier (20 dB gain)	1011

type	description	page
TDA1518Q	22 W BTL or 2 x 11 W stereo car radio power amplifier; closed loop voltage gain 46 dB	1019
TDA1519	2 x 6 W stereo car radio audio power amplifier (40 dB gain)	1027
TDA1519A	22 W BTL or 2 x 11 W stereo car radio power amplifier	1035
TDA1519B	12 W BTL or 2 x 6 W stereo car radio power amplifier	1045
TDA1520B	20 W hi-fi audio power amplifier; complete SOAR protection	1055
TDA1520BQ	20 W hi-fi audio power amplifier; complete SOAR protection	1055
TDA1521	2 x 12 W hi-fi stereo audio power amplifier	1061
TDA1521A	2 x 6 W hi-fi stereo audio power amplifier	1071
TDA1521Q	2 x 12 W hi-fi stereo audio power amplifier	1061
TDA1522	stereo playback amplifier/equalizer with mute switch	1081
TDA1524A	stereo tone/volume control circuit	1091
TDA1525	stereo tone/volume control circuit	1103
TDA1534	14-bit ADC	1117
TDA1535	high-speed sample-and-hold amplifier	1125
TDA1541A	dual 16-bit DAC	1129
TDA1542	active element for post filtering (dual channel)	1137
TDA1543	dual 16-bit economy DAC (I^2S-bus format)	1145
TDA1572	AM receiver circuit for stereo hi-fi and car radios	1153
TDA1572T	AM receiver circuit for stereo hi-fi and car radios	1171
TDA1574	integrated FM tuner for radio receivers	1187
TDA1574T	integrated FM tuner for radio receivers	1195
TDA1576	FM/IF amplifier and detector	1205
TDA1578A	time multiplex PLL stereo decoder for hi-fi and car radios	1217
TDA1579	traffic warning decoder circuit (AM carriers); ARI system	1231
TDA1579T	traffic warning decoder circuit (AM carriers); ARI system	1231
TDA1589	traffic control message and warning tone circuit; ARI system	1241
TDA1596	FM/IF amplifier and detector	1249
TDA1596T	FM/IF amplifier and detector	1267
TDA1598	time multiplex PLL stereo decoder for hi-fi and car radios	1285
TDA1600	multi-function oscillator switch for audio cassette recorders	1293
TDA2611A	5 W audio power amplifier	1305
TDA2613	6 W hi-fi audio power amplifier	1315
TDA3047P	high performance receiver for infrared remote control; positive output voltage	1323
TDA3047T	high performance receiver for infrared remote control; positive output voltage	1323
TDA3048P	high performance receiver for infrared remote control; negative output voltage	1329
TDA3048T	high performance receiver for infrared remote control; negative output voltage	1329
TDA3810	spatial, stereo and pseudo-stereo sound circuit	1335
TDA5040T	DC motor drive circuit with magnetic-field detector	1339
TDA5708	photo diode signal processor for Compact Disc single-spot read-out systems	1347
TDA5709	radial error signal processor for Compact Disc	1367
TDA7000	FM radio circuit; mono (in plastic DIL18)	1381
TDA7010T	FM radio circuit; mono (in SO16 plastic mini-pack)	1389
TDA7021T	FM radio circuit; stereo/mono; for low voltage micro tuning system (MTS)	1397

type	description	page
TDA7030T	low voltage micro tuning system (MTS)	1407
TDA7040T	PLL stereo decoder; low voltage	1415
TDA7050	150 mW BTL or 2 x 75 mW stereo audio power amplifier; low voltage	1423
TDA7050T	150 mW BTL or 2 x 75 mW stereo audio power amplifier; low voltage	1427
TDA7052	1 W BTL mono audio amplifier for portable applications	1431
TDA7053	2 x 1 W BTL stereo audio power amplifier for portable applications	1437
TDA8420	hi-fi stereo audio processor; I^2C-bus	1445
TDA8421	hi-fi stereo audio processor; I^2C-bus	1467
TDA8425	hi-fi stereo audio processor; I^2C-bus	1489
TDA8444	octuple 6-bit DAC; I^2C-bus	1511
TDA8808AT	photo diode signal processor for Compact Disc	1519
TDA8808T	photo diode signal processor for Compact Disc	1519
TDA8808	transfer functions	1539
TDA8809T	radial error signal processor for Compact Disc	1559
TDA8809	transfer functions	1571
TDB1080	IF limiting amplifier, FM detector and audio amplifier	1583
TDB1080T	IF limiting amplifier, FM detector and audio amplifier	1583
TDD1601	equalizer for audio cassette recorders	1589
TDD1742T	low power frequency synthesizer (LOPSY)	1605
TEA0651	Dolby B & C noise reduction circuit	1627
TEA0652	Dolby B & C noise reduction circuit	1627
TEA0653T	stereo or 2-channel Dolby B noise reduction circuit	1645
TEA0654	preamplifier and electronic switch for Dolby B & C noise reduction circuits	1627
TEA0657	dual Dolby B noise reduction circuit	1651
TEA0665	Dolby B & C processor with preamplifier and electronic switch	1659
TEA0665T	Dolby B & C processor with preamplifier and electronic switch	1659
TEA0666	Dolby B & C processor with preamplifier and electronic switch; changed frequency response in relation to TEA0665	1669
TEA0666T	Dolby B & C processor with preamplifier and electronic switch; changed frequency response in relation to TEA0665	1669
TEA0670T	Dolby B & C processor with preamplifier and electronic switch; low voltage	1679
TEA5551T	single-chip AM radio circuit, plus dual AF amplifier, for pocket receivers with headphones	1685
TEA5570	AM/FM radio receiver circuit	1697
TEA5580	PLL stereo decoder for medium-fi and car radios	1711
TEA5581	PLL stereo decoder with source selector switch for medium-fi and car radios	1721
TEA5581T	PLL stereo decoder with source selector switch for medium-fi and car radios	1721
TEA5591	AM/FM radio receiver circuit	1733

type	description	page
TEA6100	FM/IF system and microcomputer-based tuning interface; I^2C-bus	1751
TEA6200	AM upconversion radio receiver; 10.7 MHz IF	1775
TEA6300	car radio preamplifier and source selector with sound and fader controls; I^2C-bus	1787
TEA6300T	car radio preamplifier and source selector with sound and fader controls; I^2C-bus	1787
TEA6310T	sound fader control circuit; I^2C-bus	1803
TSA6057	radio tuning PLL frequency synthesizer; I^2C-bus	1821
TSA6057T	radio tuning PLL frequency synthesizer; I^2C-bus	1821
μA758N	FM stereo multiplex decoder; PLL	1831

MAINTENANCE TYPE LIST

The types listed below are not included in this handbook. Detailed information will be supplied on request.

SAA1056P	PLL frequency synthesizer	successor type: SAA1057
SAA3027	infrared remote control transmitter (RC-5)	successor type: SAA3006
TCA730A	DC volume and balance stereo control circuit	
TCA740A	DC treble and bass stereo control circuit	
TDA1011A	2 to 6 W audio power amplifier	successor type: TDA1011
TDA1506	motor regulator and function controller for car cassette systems	
TDA1508	auto-reverse car radio cassette deck steering circuit	
TDA1533	PLL motor speed control circuit for hi-fi applications	
TDA7020T	low voltage FM stereo radio circuit	successor type: TDA7021T

DEVICE DATA

12 to 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1512 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Low intermodulation distortion
- Low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA
Output power at d_{tot} = 0,7%			
sine-wave power			
V_P = 25 V; R_L = 4 Ω	P_o	typ.	13 W
V_P = 25 V; R_L = 8 Ω	P_o	typ.	7 W
music power			
V_P = 32 V; R_L = 4 Ω	P_o	typ.	21 W
V_P = 32 V; R_L = 8 Ω	P_o	typ.	12 W
Closed-loop voltage gain (externally determined)	G_c	typ.	30 dB
Input resistance (externally determined)	R_i	typ.	20 kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ.	72 dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	50 dB

PACKAGE OUTLINES

TDA1512: 9-lead SIL; plastic power (SOT131).
TDA1512Q: 9-lead SIL-bent-to-DIL; plastic power (SOT157).

PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Ground potential
5. Output
6. Positive supply (V_P)
7. Externally connected to pin 6
8. Ripple rejection
9. Inverting input (feedback)

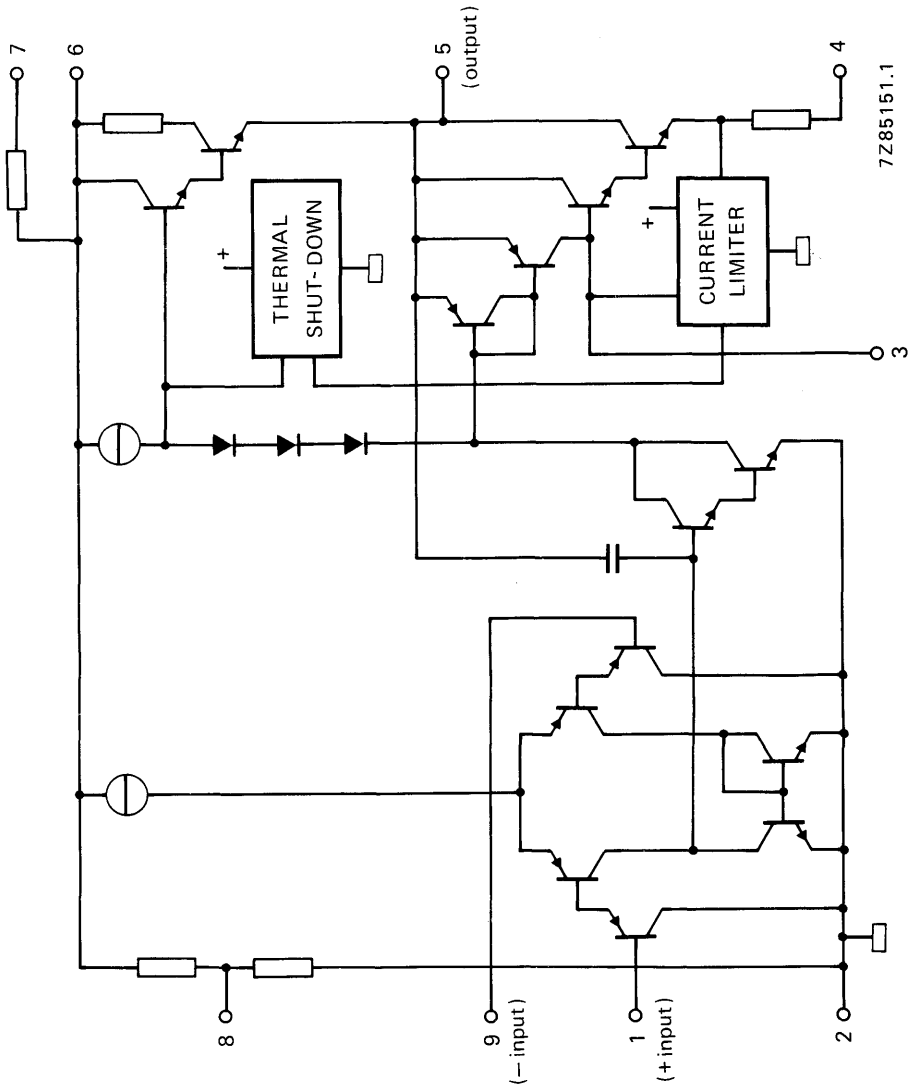


Fig. 1 Simplified internal circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Repetitive peak output current	I_{ORM}	max.	3,2 A
Non-repetitive peak output current	I_{OSM}	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C
A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 30$ V with $R_i = 4\ \Omega$	t_{sc}	max.	100 hours

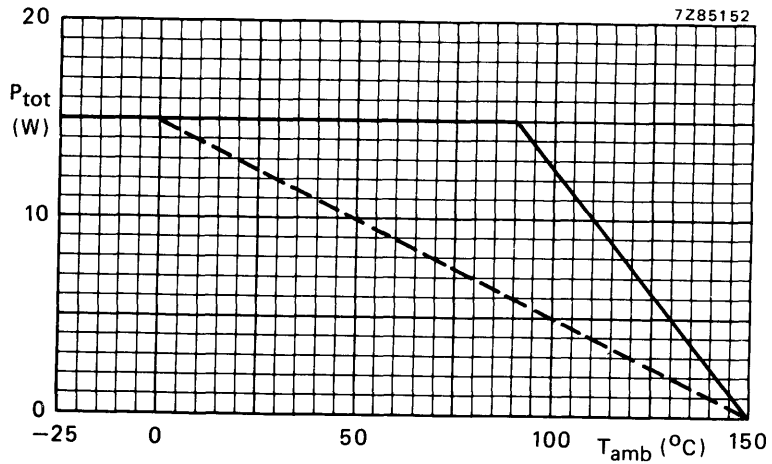


Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	typ.	3 K/W
		⩽	4 K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA

A.C. CHARACTERISTICS

V_P = 25 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power			
sine-wave power at d_{tot} = 0,7 %			
R_L = 4 Ω	P_o	typ.	13 W
R_L = 8 Ω	P_o	typ.	7 W
music power at V_P = 32 V			
R_L = 4 Ω; d_{tot} = 0,7 %	P_o	typ.	21 W
R_L = 4 Ω; d_{tot} = 10 %	P_o	typ.	25 W
R_L = 8 Ω; d_{tot} = 0,7 %	P_o	typ.	12 W
R_L = 8 Ω; d_{tot} = 10 %	P_o	typ.	15 W
Power bandwidth; −1,5 dB; d_{tot} = 0,7%	B		40 Hz to 16 kHz
Voltage gain			
open-loop	G_o	typ.	74 dB
closed-loop	G_c	typ.	30 dB
Input resistance (pin 1)	R_i	>	100 kΩ
Input resistance of test circuit (Fig. 3)	R_i	typ.	20 kΩ
Input sensitivity			
for P_o = 50 mW	V_i	typ.	16 mV
for P_o = 10 W	V_i	typ.	210 mV
Signal-to-noise ratio			
at P_o = 50 mW; R_S = 2 kΩ; f = 20 Hz to 20 kHz; unweighted	S/N	>	68 dB
weighted; measured according to IEC 173 (A-curve)	S/N	typ.	76 dB
Ripple rejection at f = 100 Hz	RR	typ.	50 dB
Total harmonic distortion at P_o = 10 W	d_{tot}	typ. <	0,1 % 0,3 %
Output resistance (pin 5)	R_o	typ.	0,1 Ω

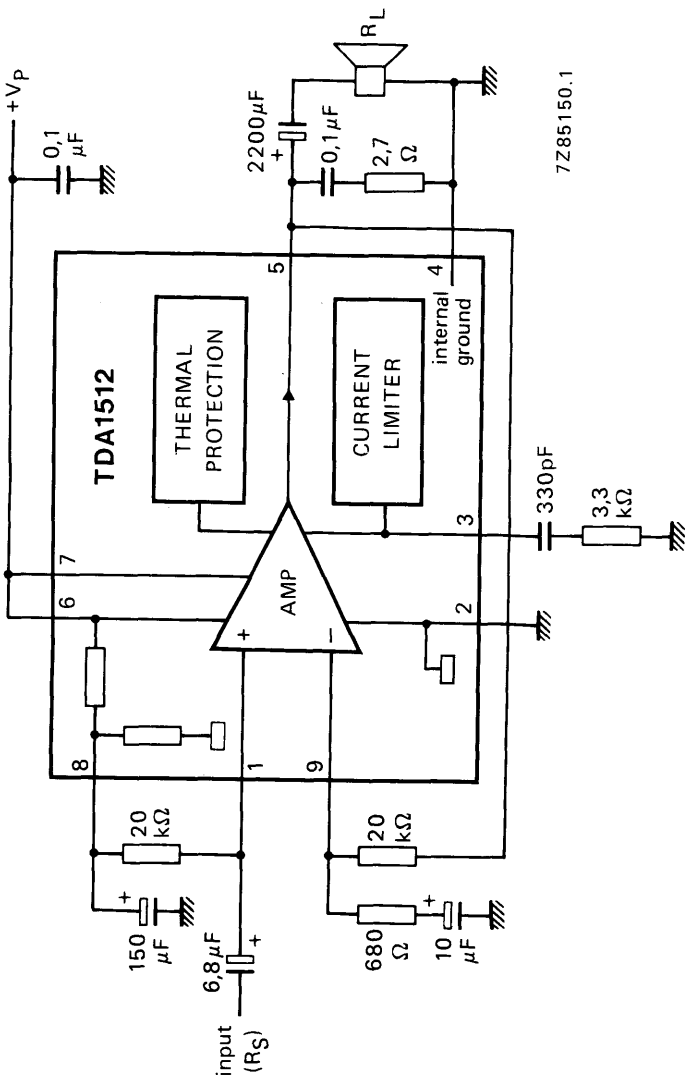


Fig. 3 Test circuit.

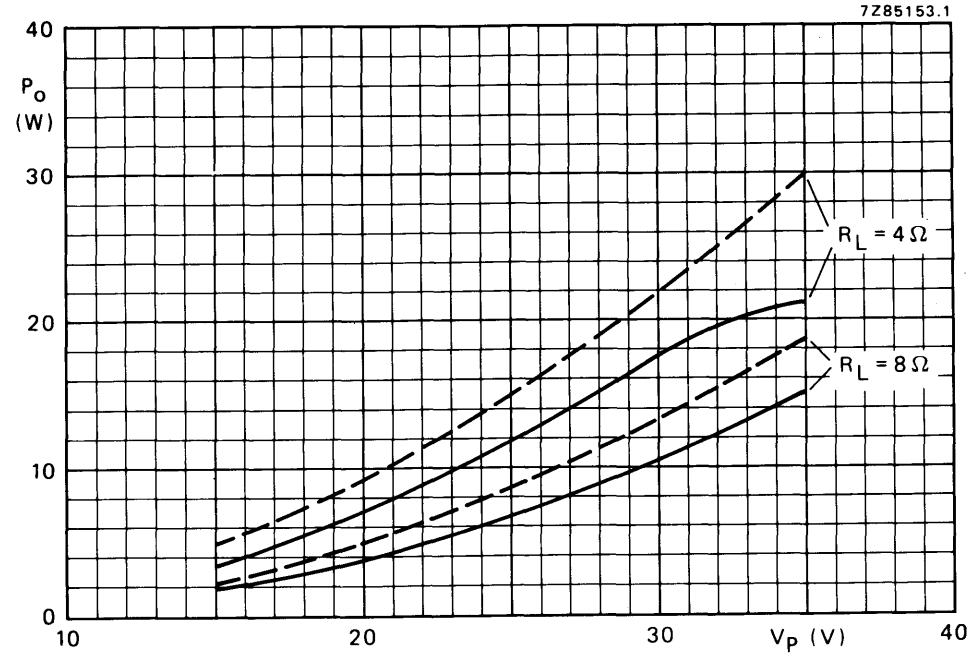


Fig. 4 Output power as a function of the supply voltage; f = 1 kHz;
——— d_{tot} = 0,7 %; – – – d_{tot} = 10 %.

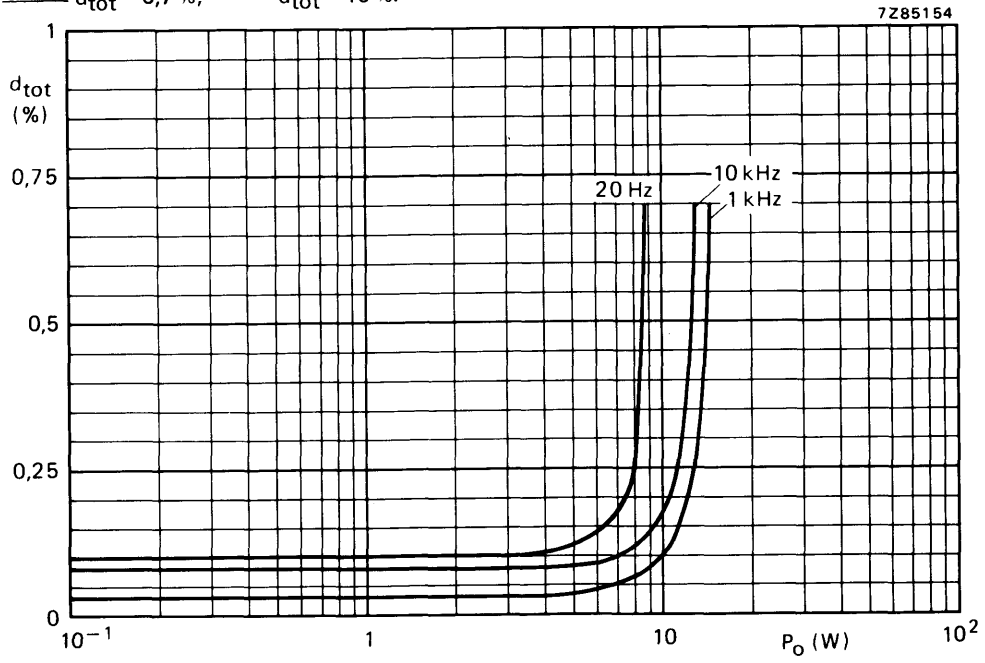


Fig. 5 Total harmonic distortion as a function of the output power.

50 W HIGH- PERFORMANCE HI-FI AMPLIFIER

GENERAL DESCRIPTION

The TDA1514A integrated circuit is a hi-fi power amplifier for use as a building block in radio, tv and other audio applications. The high performance of the IC meets the requirements of digital sources (e.g. Compact Disc equipment).
The circuit is totally protected, the two output transistors both having thermal and SOAR protection (see Fig.3). The circuit also has a mute function that can be arranged for a period after power-on with a delay time fixed by external components.
The device is intended for symmetrical power supplies but an asymmetrical supply may also be used.

Features

- High output power (also without bootstrap)
- Low offset voltage
- Good ripple rejection
- Mute/stand-by facilities
- Thermal protection
- Protected against electrostatic discharge
- No switch-on or switch-off clicks
- Very low thermal resistance
- Safe Operating Area (SOAR) protection
- Short-circuit protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6 to pin 4)		V_P	± 9	–	± 30	V
Total quiescent current	V_P = ± 27.5 V	I_{tot}	–	60	–	mA
Output power	THD = –60 dB; V_P = ± 27.5 V; R_L = 8 Ω	P_o	–	40	–	W
	V_P = ± 23 V; R_L = 4 Ω	P_o	–	50	–	W
Closed loop voltage gain	determined externally	G_c	–	30	–	dB
Input resistance	determined externally	R_i	–	20	–	kΩ
Signal plus noise-to-noise ratio	P_o = 50 mW	(S+N)/N	–	82	–	dB
Supply voltage ripple rejection	f = 100 Hz	SVRR	–	72	–	dB

PACKAGE OUTLINE

9-lead SIL, plastic power (SOT131A).

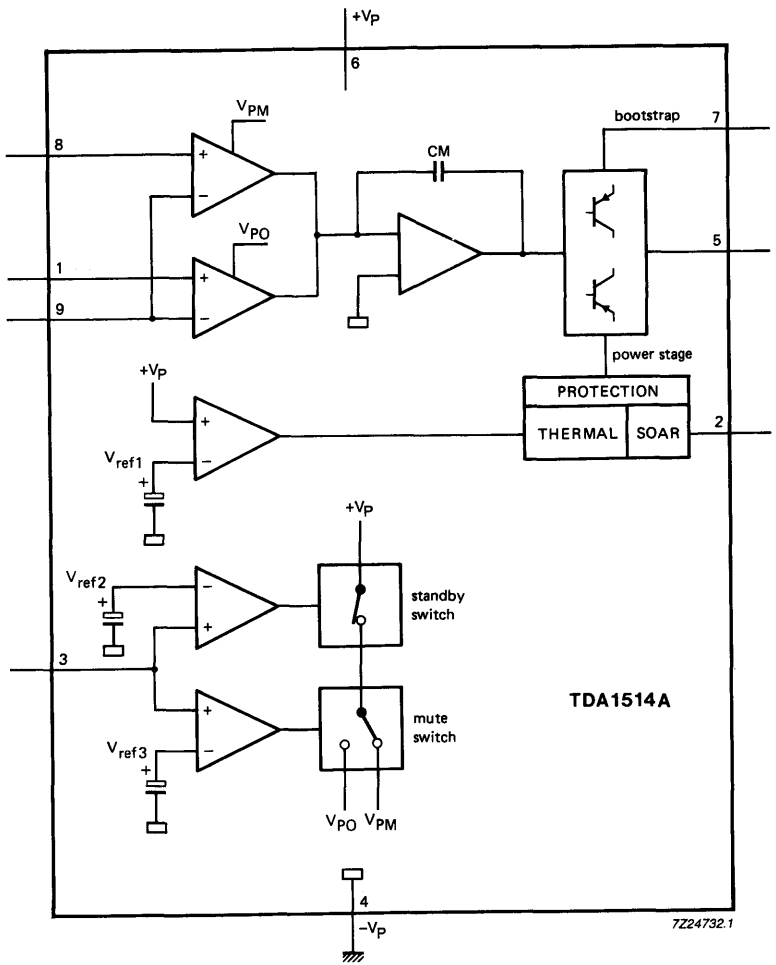


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6 to pin 4)	V_P	–	±30	V
Bootstrap voltage (pin 7 to pin 4)	V_{bstr}	–	70	V
Output current (repetitive peak)	I_o	–	8	A
Operating ambient temperature range	T_{amb}	see Fig.2		
Storage temperature range	T_{stg}	−65	+150	°C
Power dissipation		see Fig.2		
Thermal shut-down protection time	t_{pr}	–	1	hour
Short circuit protection time*	t_{sc}	–	10	min
Mute voltage (pin 3 to pin 4)	V_m	–	7	V

THERMAL RESISTANCE

From junction to mounting base

$R_{th\ j\text{-}mb}$ max. = 1 K/W

DEVELOPMENT DATA

* Symmetrical power supply: AC and DC short-circuit protected.
Asymmetrical power supply: AC short-circuit protected.
Driven by a pink-noise voltage.

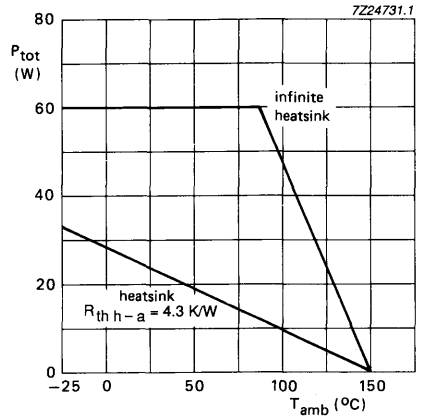


Fig.2 Power derating curve.

The theoretical maximum power dissipation for P_o = 40 W with a stabilized power supply is:

$$\frac{V_P^2}{2\pi^2 R_L} = 19\ W; \text{ where } V_P = \pm 27.5\ V;\ R_L = 8\ \Omega$$

Considering, for example, a maximum ambient temperature of 50 °C and a maximum junction temperature of 150 °C the total thermal resistance is:

$$R_{th\ j\text{-}a} = \frac{150 - 50}{19} = 5.3\ K/W$$

Since the thermal resistance of the SOT131A encapsulation is $R_{th\ j\text{-}mb} < 1$ K/W, the thermal resistance required of the heatsink is $R_{th\ h\text{-}a} < 4.3$ K/W.

SAFE OPERATING AREA (SOAR) PROTECTION

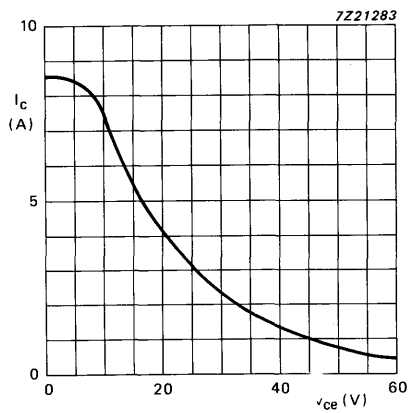


Fig.3 SOAR protection curve.

DEVELOPMENT DATA

CHARACTERISTICS

V_P = ± 27.5 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; test circuit as Fig.4; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6 to pin 4)		V_P	± 9	–	± 30	V
Maximum output current (peak value)		$I_{OM\,max}$	6.4	–	–	A
Operating state						
Input voltage (pins 3 to 4)		V_{3-4}	6	–	7	V
Total quiescent current	$R_L = \infty$	I_{tot}	30	60	90	mA
Output power	THD = –60 dB	P_o	37	40	–	W
	THD = –20 dB	P_o	–	51	–	W
Output power	V_P = ± 23 V; THD = –60 dB					
	R_L = 8 Ω	P_o	–	28	–	W
	R_L = 4 Ω	P_o	–	50	–	W
Total harmonic distortion	P_o = 32 W	THD	–	–90	–80	dB
Intermodulation distortion	P_o = 32 W note 1	d_{im}	–	–80	–	dB
Power bandwidth	(–3 dB); THD = –60 dB	B	–	20 to 25 000		Hz
Slew rate		dV/dt	–	10	–	V/μs
Closed loop voltage gain	note 2	G_c	–	30	–	dB
Open loop voltage gain		G_o	–	85	–	dB
Input impedance	note 3	$\|Z_i\|$	1	–	–	MΩ
Signal-to-noise ratio	note 4 P_o = 50 mW	S/N	80	–	–	dB
Output offset voltage		V_o	–	2	*	mV
Input bias current		I_I	–	0.1	*	μA
Output impedance		$\|Z_o\|$	–	–	0.1	Ω
Supply voltage ripple rejection	ripple frequency = 100 Hz; ripple voltage = 500 mV_{eff}; (RMS value) source resistance = 2 kΩ	SVRR	*	–	–	dB
Quiescent current into pin 2	note 5	I_2	–	–	*	μA

* Value to be fixed.

CHARACTERISTICS (continued)

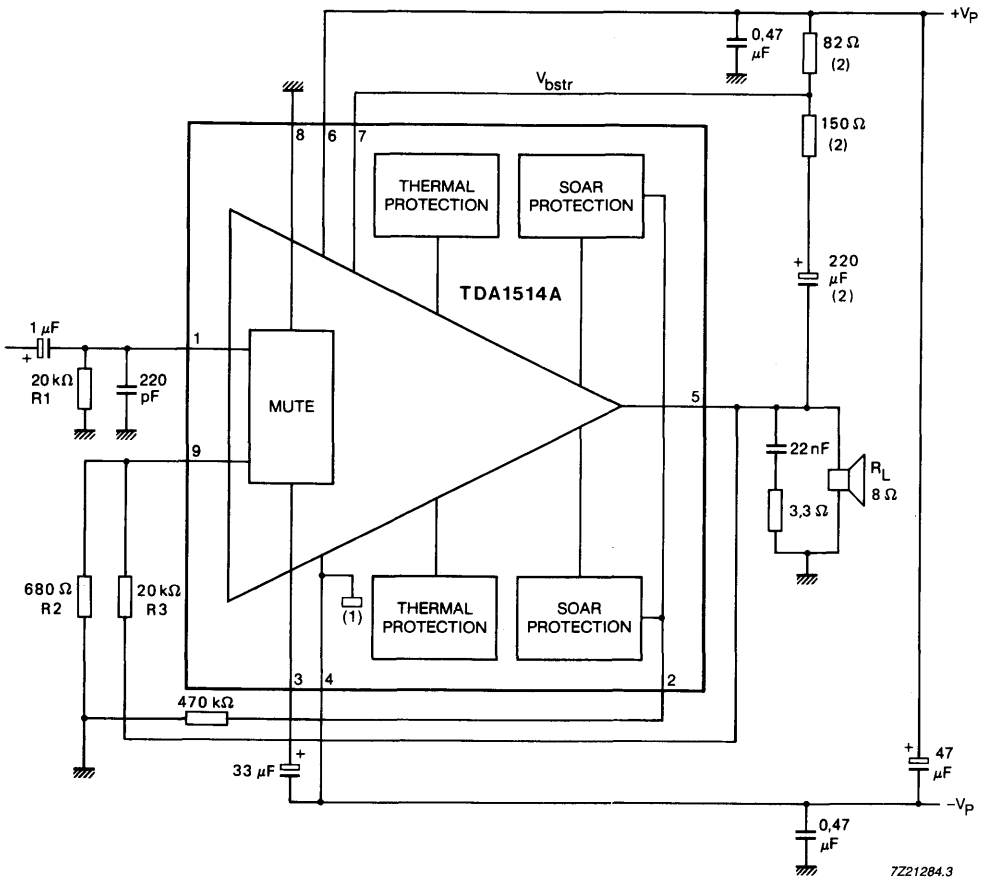
parameter	conditions	symbol	min.	typ.	max.	unit
Mute state						
Voltage on pin 3		V_{3-4}	2	–	4.5	V
Offset voltage		V_o	–	*	–	V
Output voltage	$V_{i(rms)}$ = 2 V f = 1 kHz	V_o	–	100	–	μV
Ripple rejection		RR	–	70	–	dB
Standby state						
Voltage on pin 3		V_{3-4}	0	–	1	V
Total quiescent current		I_{tot}	–	20	–	mA
Ripple rejection		RR	–	70	–	dB
Supply voltage to obtain standby state		$\pm V_P$	4.5	–	7.0	V

Notes to the characteristics

1. Measured with two superimposed signals of 50 Hz and 7 kHz with an amplitude relationship of 4 : 1.
2. The closed loop gain is determined by external resistors (Fig.4, R2 and R3) and is variable between 20 and 46 dB.
3. The input impedance in the test circuit (Fig.4) is determined by the bias resistor R1.
4. The noise output voltage is measured in a bandwidth of 20 Hz to 20 kHz with a source resistance of 2 kΩ.
5. The quiescent current into pin 2 has an impact on the mute time.

* Value to be fixed.

DEVELOPMENT DATA



(1) Mounting base connected to $-V_P$.

(2) When used without a bootstrap these components are disconnected and pin 6 is connected to pin 7 thus decreasing the output power by approximately 4 W.

Fig.4 Application and test circuit.

24 W BTL OR 2 x 12 W STEREO CAR RADIO POWER AMPLIFIER

The TDA1515A is a monolithic integrated class-B output amplifier in a 13-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1,6 Ω). At a supply voltage V_P = 14,4 V, an output power of 24 W can be delivered into a 4 Ω BTL (Bridge Tied Load), or, when used as stereo amplifier, it delivers 2 x 12 W into 2 Ω or 2 x 7 W into 4 Ω.

Special features are:

- flexibility in use – mono BTL as well as stereo
- high output power
- low offset voltage at the output (important for BTL)
- large usable gain variation
- very good ripple rejection
- internal limited bandwidth for high frequencies
- low stand-by current possibility (typ. 1 μA), to simplify required switches; TTL drive possible
- low number and small sized external components
- high reliability

The following currently required protections are incorporated in the circuit. These protections also have positive influence on reliability in the applications.

- load dump protection
- **a.c. and d.c. short-circuit safe to ground up to V_P = 18 V**
- thermal protection
- speaker protection in bridge configuration
- SOAR protection
- outputs short-circuit safe to ground in BTL
- reverse polarity safe

QUICK REFERENCE DATA

Supply voltage range (operating)	V_P		6 to 18	V
Supply voltage (non-operating)	V_P	max.	28	V
Supply voltage (non-operating; load dump protection)	V_P	max.	45	V
Repetitive peak output current	I_{ORM}	max.	4	A
Total quiescent current	I_{tot}	typ.	75	mA
Stand-by current	I_{sb}	typ.	1	μA
Switch-on current	I_{so}	<	100	μA
Input impedance	$\|Z_i\|$	>	1	MΩ
Bridge tied load application (BTL)	V_P	=	14,4 | 13,2	V
Output power at R_L = 4 Ω (with bootstrap)				
d_{tot} = **0,5%**	P_o	typ.	18 | 15	W
d_{tot} = 10%	P_o	typ.	24 | 20	W
Supply voltage ripple rejection; R_S = 0 Ω; f = 100 Hz	RR	typ.	50 | 50	dB
D.C. output offset voltage between the outputs	$\|\Delta V_{5-9}\|$	<	50 | 50	mV
Stereo application				
Output power at d_{tot} = 10% (with bootstrap)				
R_L = 4 Ω	P_o	typ.	7 | 6	W
R_L = 2 Ω	P_o	typ.	12 | 10	W
Output power at **d_{tot} = 0,5%** (with bootstrap)				
R_L = 4 Ω	P_o	typ.	5,5 | 4,5	W
R_L = 2 Ω	P_o	typ.	9 | 7,5	W
Channel separation	α	>	40 | 40	dB
Noise output voltage; R_S = 10 kΩ; according to IEC curve-A	V_n	typ.	0,2 | 0,2	mV

PACKAGE OUTLINE 13-lead SIL-bent-to-DIL; plastic power (SOT141C).

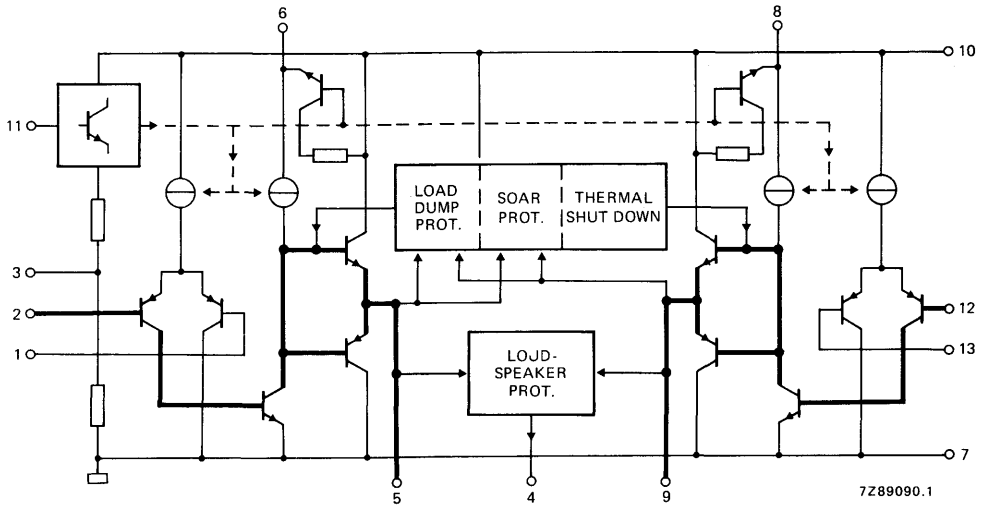


Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 10)	V_P	max.	18 V
Supply voltage; non-operating	V_P	max.	28 V
Supply voltage; during 50 ms (load dump protection)	V_P	max.	45 V
Peak output current	I_{OM}	max.	6 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	150 °C
A.C. and d.c. short-circuit safe voltage		max.	18 V
Reverse polarity		max.	10 V

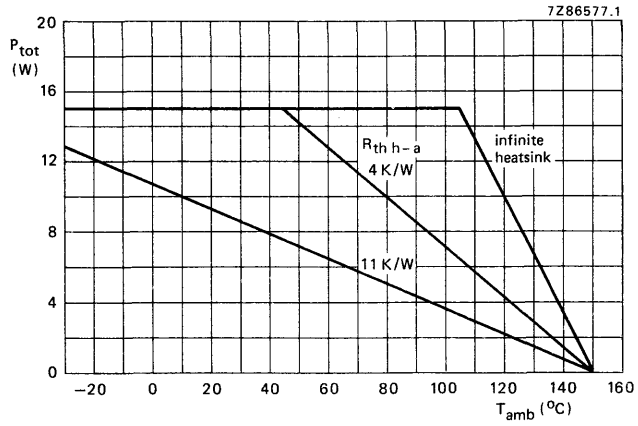


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of 3 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω)
maximum sine-wave dissipation: 12 W
T_{amb} = 65 °C maximum

$$R_{th\ h\text{-}a} = \frac{150-65}{12} - 3 = 4\ \text{K/W}.$$

2 x 7 W stereo (4 Ω)
maximum sine-wave dissipation: 6 W
T_{amb} = 65 °C maximum

$$R_{th\ h\text{-}a} = \frac{150-65}{6} - 3 = 11\ \text{K/W}.$$

D.C. CHARACTERISTICS

Supply voltage range (pin 10)	V_P		6 to 18 V
Repetitive peak output current	I_{ORM}	<	4 A
Total quiescent current	I_{tot}	typ.	75 mA
Switching level 11 : OFF	V_{11}	<	1,8 V
ON	V_{11}	>	3 V
Impedance between pins 10 and 6; 10 and 8 (stand-by position $V_{11} < 1,8$ V)	$\|Z_{OFF}\|$	>	100 kΩ
Stand-by current at V_{11} = 0 to 0,8 V	I_{sb}	typ.	1 μA
		<	100 μA
Switch-on current (pin 11) at $V_{11} \leqslant V_{10}$ (note 1)	I_{so}	typ.	10 μA
		<	100 μA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; f = 1 kHz; unless otherwise specified

Bridge tied load application (BTL); see Fig. 3

Output power at R_L = 4 Ω (with bootstrap)			
V_P = 14,4 V; **d_{tot} = 0,5%**	P_o	>	15,5 W
		typ.	18 W
V_P = 14,4 V; d_{tot} = 10%	P_o	>	20 W
		typ.	24 W
V_P = 13,2 V; **d_{tot} = 0,5%**	P_o	typ.	15 W
V_P = 13,2 V; d_{tot} = 10%	P_o	typ.	20 W
Open loop voltage gain	G_o	typ.	75 dB
Closed loop voltage gain (note 2)	G_c	typ.	40 (± 0,5) dB
Output power without bootstrap (note 9)			
V_P = 14,4 V; d_{tot} = 10 %	P_o	typ.	15 W
V_P = 14,4 V; d_{tot} = 0,5 %	P_o	typ.	12 W
V_P = 13,2 V; d_{tot} = 10 %	P_o	typ.	12 W
V_P = 13,2 V; d_{tot} = 0,5 %	P_o	typ.	9 W
Frequency response at −3 dB (note 3)	B		20 Hz to min. 20 kHz
Input impedance (note 4)	$\|Z_i\|$	>	1 MΩ
Noise input voltage (r.m.s. value) at f = 20 Hz to 20 kHz			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,2 mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,35 mV
		<	0,8 mV
R_S = 10 kΩ; according to IEC 179 curve A	V_n	typ.	0,25 mV
Supply voltage ripple rejection (note 5)			
f = 100 Hz	RR	>	42 dB
		typ.	50 dB
D.C. output offset voltage between the outputs	$\|\Delta V_{5\text{-}9}\|$	<	50 mV
		typ.	2 mV
Loudspeaker protection (all conditions) maximum d.c. voltage (across the load)	$\|\Delta V_{5\text{-}9}\|$	<	1 V
Power bandwidth; −1 dB; **d_{tot} = 0,5%**	B		30 Hz to 40 kHz

Stereo application; see Fig. 4

Output power at d_{tot} = 10%; with bootstrap (note 6)			
V_P = 14,4 V; R_L = 4 Ω	P_o	>	6 W
		typ.	7 W
V_P = 14,4 V; R_L = 2 Ω	P_o	>	10 W
		typ.	12 W
V_P = 13,2 V; R_L = 4 Ω	P_o	typ.	6 W
V_P = 13,2 V; R_L = 2 Ω	P_o	typ.	10 W
Output power at d_{tot} = **0,5%**; with bootstrap (note 6)			
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	5,5 W
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	9 W
V_P = 13,2 V; R_L = 4 Ω	P_o	typ.	4,5 W
V_P = 13,2 V; R_L = 2 Ω	P_o	typ.	7,5 W
Output power at d_{tot} = 10%; without bootstrap			
V_P = 14,4 V; R_L = 4 Ω (notes 6, 8 and 9)	P_o	typ.	6 W
Frequency response at −3 dB (note 3)	B	40 Hz to min.	20 kHz
Supply voltage ripple rejection (note 5)	RR	typ.	50 dB
Channel separation; R_S = 10 kΩ; f = 1 kHz	α	>	40 dB
		typ.	50 dB
Closed loop voltage gain (note 7)	G_c	typ.	40 dB
Noise output voltage (r.m.s. value) at f = 20 Hz to 20 kHz			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,15 mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,25 mV
R_S = 10 kΩ; according to IEC 179 curve A	V_n	typ.	0,2 mV

Notes

1. The internal circuit impedance at pin 11 is > 5 kΩ if $V_{11} > V_{10}$.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components. For further gain reduction see Application Report.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 kΩ.
5. Supply voltage ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude: 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 to reach symmetrical clipping.
9. Without bootstrap the 100 μF capacitor between pins 5 and 6 (8 and 9) can be omitted. Pins 6, 8 and 10 have to be interconnected.

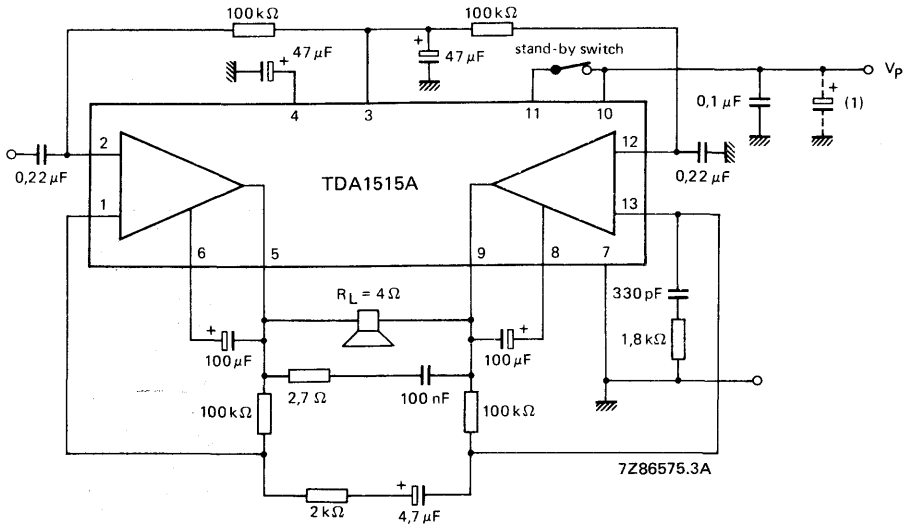


Fig. 3 Test/application circuit bridge tied load (BTL).

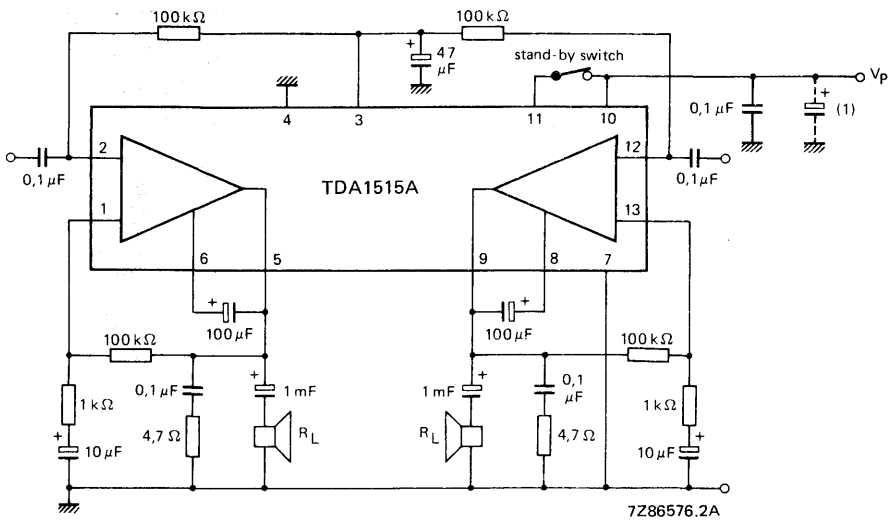


Fig. 4 Test/application circuit stereo.

1. Belongs to power supply.

22 W BTL OR 2 × 11 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1516Q is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The device is primarily developed for car radio applications.

FEATURES

- Requires very few external components
- Flexibility in use – stereo as well as mono BTL
- High output power (without bootstrap)
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- A.C. and d.c. short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1518Q (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30,0	V
load dump protected		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	30	–	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 10%; 4 Ω	P_o	–	6	–	W
	THD = 10%; 2 Ω	P_o	–	11	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	50	–	μV
BTL application						
Output power	THD = 10%; 4 Ω	P_o	–	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	RR	48	–	–	dB
D.C. output offset voltage		$\|\Delta V_O\|$	–	–	100	mV

PACKAGE OUTLINE

13-lead SIL-bent-to-DIL; plastic power (SOT141C).

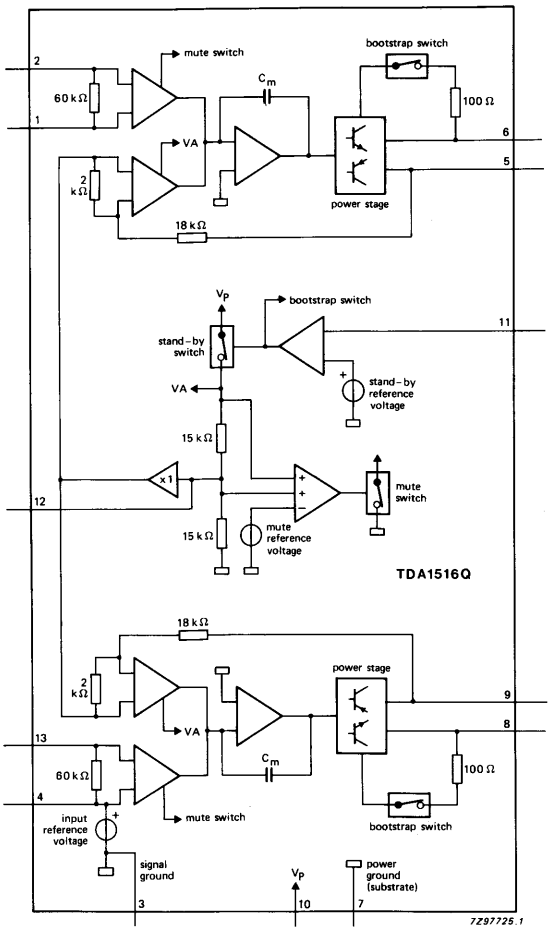


Fig. 1 Block diagram.

PINNING

1	−INV1	non-inverting input 1
2	INV	inverting input
3	GND1	ground (signal)
4	V_{ref}	reference voltage
5	OUT1	output 1
6	BS1	bootstrap 1
7	GND2	ground (substrate)
8	BS2	bootstrap 2
9	OUT2	output 2
10	V_P	supply voltage
11	M/SS	mute/stand-by switch
12	RR	supply voltage ripple rejection
13	−INV2	non-inverting input 2

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA1516Q contains two identical amplifiers with differential input stages. This device can be used for stereo or bridge applications. The gain of each amplifier is fixed at 20 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
A.C. and d.c. short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}	–	25	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	–65	+ 150	°C

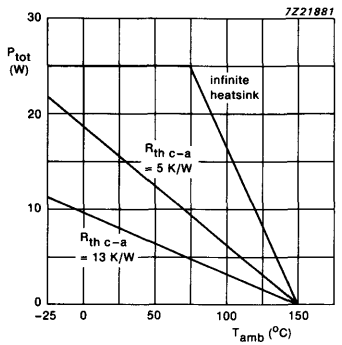


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS (note 1)

V_P = 14,4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	40	80	mA
D.C. output voltage at approximately $V_P/2$	note 3	V_O	–	6,8	–	V
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	100	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,0	–	6,4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	*	2	mV
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	100	mV
Stand-by condition		V_{sb}	0	–	2	V
D.C. current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

* Value to be fixed.

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application	note 1					
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
	notes 4 and 5;					
	THD = 10%	P_o	6	7	–	W
Output power at	note 4;					
R_L = 2 Ω	THD = 0,5%	P_o	7.5	8,5	–	W
	THD = 10%	P_o	10	11	–	W
	notes 4 and 5;					
	THD = 10%	P_o	10,5	12,0	–	W
Low frequency roll-off	note 6;					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	19	20	21	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	50	60	75	kΩ
Noise output voltage:	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	50	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	70	100	μV
mute	note 9	$V_{no(rms)}$	–	50	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		G_v	–	–	1	dB

A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application	note 10					
Output power	THD =0,5%	P_o	15,5	17,0	–	W
	THD = 10%	P_o	20	22	–	W
	note 5; THD = 10%	P_o	21	24	–	W
Output power at V_P = 13,2 V	THD = 0,5%	P_o	–	13,5	–	W
	THD = 10%	P_o	–	17	–	W
	note 5; THD = 10%	P_o	–	19	–	W
Power bandwidth	THD = 0,5% P_o = 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 6; –3 dB	f_L	–	25	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	25	30	38	kΩ
Noise output voltage	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	70	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	100	200	μV
mute	note 9	$V_{no(rms)}$	–	60	–	μV

Notes to the characteristics

1. All characteristics, for stereo application are measured using the circuit shown in Fig. 3.
2. The circuit is d.c. adjusted at V_P = 6 V to 18 V and a.c. operating at V_P = 8,5 to 18 V.
3. At 18 V $< V_P <$ 30 V the d.c. output voltage $\leqslant V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. With bootstrap and a 100 kΩ resistor from pin 12 to the positive supply voltage (Vp), value of bootstrap capacitor is 47 μF.
6. Frequency response externally fixed.
7. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).
10. All characteristics, for BTL application are measured using the circuit shown in Fig. 4.

APPLICATION INFORMATION

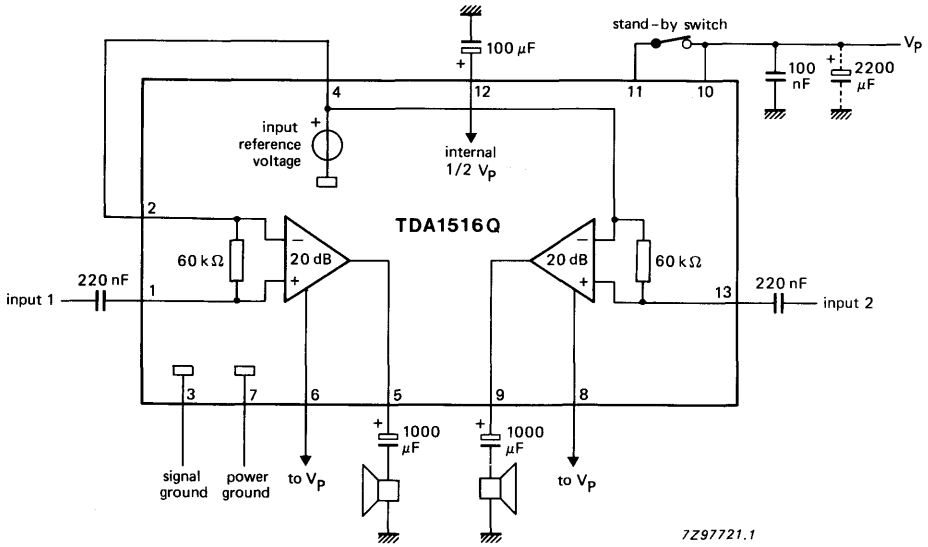


Fig. 3 Stereo application circuit diagram.

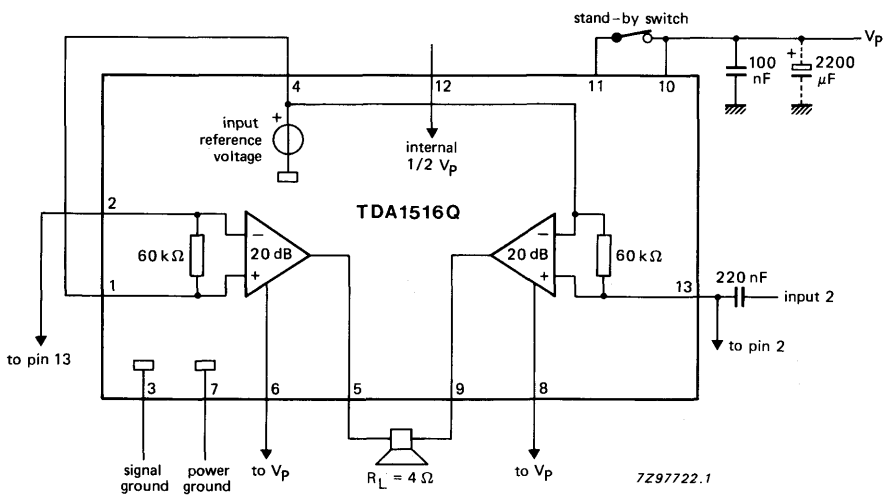


Fig. 4 BTL application circuit diagram (without bootstrapping).

DEVELOPMENT DATA

2 × 6 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1517 is an integrated class-B dual output amplifier in a 9-lead single-in-line (SIL) plastic medium power package. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- High output power
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and Vp
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Compatible with TDA1519 (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30,0	V
load dump protected		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	2,5	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance		$\|Z_I\|$	50	–	–	kΩ
Output power	THD = 0,5%; 4 Ω	P_O	–	5	–	W
	THD = 10%; 4 Ω	P_O	–	6	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	50	–	μV
Supply voltage ripple rejection	f = 100 Hz to 100 kHz	SVRR	48	–	–	dB
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

9-lead SIL-bent-to-DIL; plastic (SOT110B).

PINNING

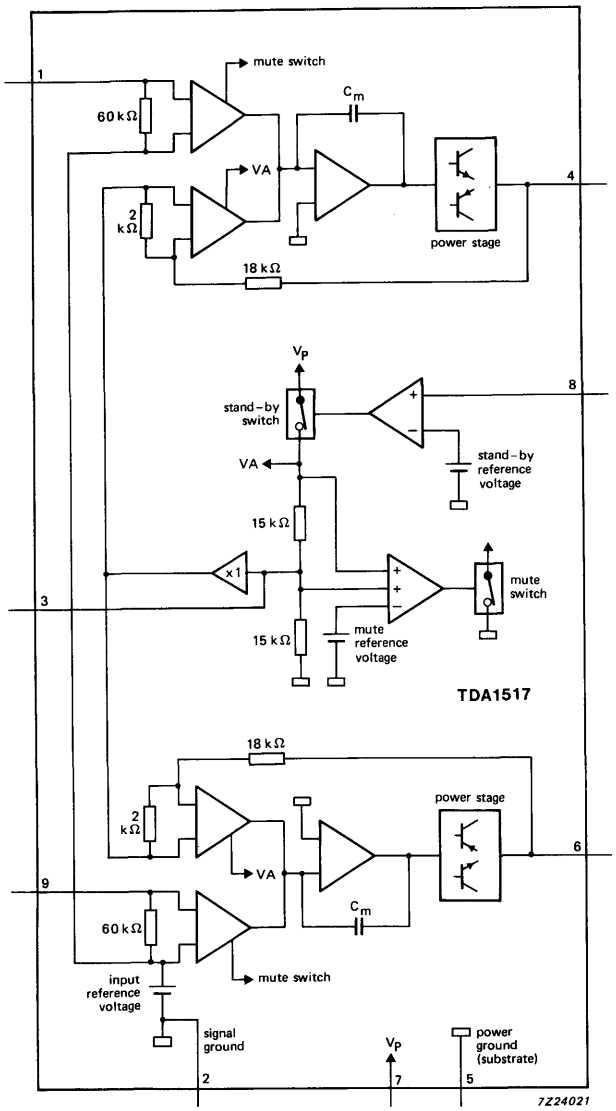


Fig. 1 Block diagram.

1	−INV1	non-inverting input 1
2	GND1	ground (signal)
3	SVRR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	supply voltage
8	M/SS	mute/stand-by switch
9	−INV2	non-interting input 2

FUNCTIONAL DESCRIPTION

The TDA1517 contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 20 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	4	A
Repetitive peak output current		I_{ORM}	–	2,5	A
Total power dissipation	see Fig. 2	P_{tot}	–	15	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	–65	+150	°C

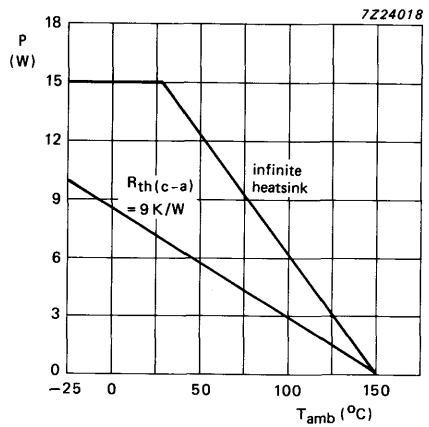


Fig. 2 Power derating curve.

DC CHARACTERISTICS (note 1)

V_P = 14,4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	40	80	mA
DC output voltage	note 3	V_O	–	6,95	–	V
Mute/stand-by switch	see Fig. 3					
Switch-on voltage level		V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,3	–	6,4	V
Output signal in mute position	V_I = 1 V (max); f = 20 Hz to 15 kHz	V_O	–	–	2	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

AC CHARACTERISTICS (note 1)

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0,1	–	%
Low frequency roll-off	note 5; –3 dB	f_L	–	45	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	19	20	21	dB
Supply voltage ripple rejection:	note 6					
ON		SVRR	48	–	–	dB
mute		SVRR	48	–	–	dB
stand-by		SVRR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage:	note 7;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	50	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	70	100	μV
mute	note 8	$V_{no(rms)}$	–	50	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		$\|\Delta G_v\|$	–	0,1	1	dB

DEVELOPMENT DATA

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig. 4.
2. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8,5 V to 18 V.
3. At 18 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. Frequency response externally fixed.
6. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
7. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
8. Noise output voltage independent of R_S (V_I = 0 V).

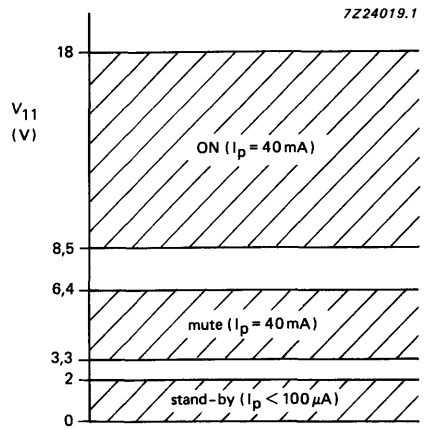


Fig. 3 Stand-by, mute and ON conditions.

APPLICATION INFORMATION

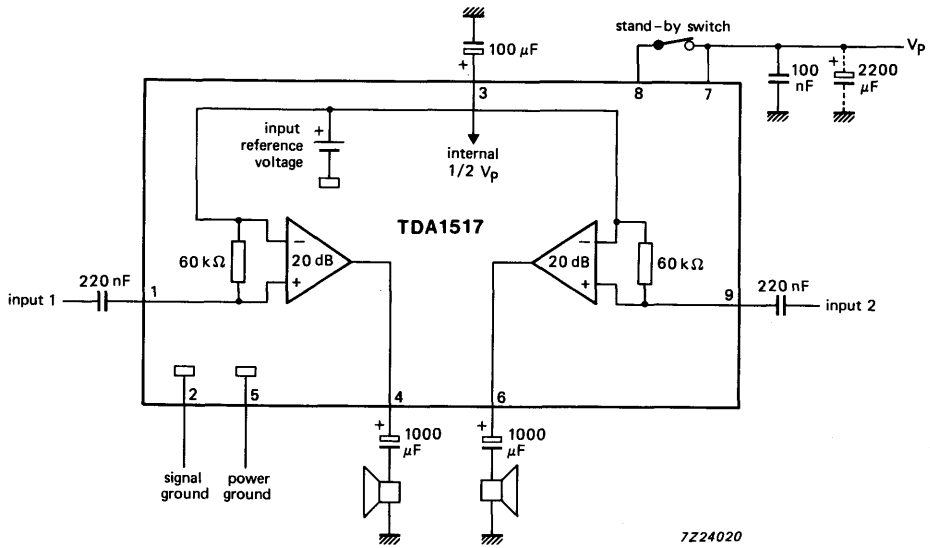


Fig. 4 Application circuit diagram.

DEVELOPMENT DATA

22 W BTL OR 2 × 11 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1518Q is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The device is primarily developed for car radio applications.

FEATURES

- Requires very few external components
- Flexibility in use – stereo as well as mono BTL
- High output power (without bootstrap)
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- A.C. and d.c. short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1516Q (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30,0	V
load dump		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	30	–	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 10%; 4 Ω	P_o	–	6	–	W
	THD = 10%; 2 Ω	P_o	–	11	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
BTL application						
Output power	THD = 10%; 4 Ω	P_o	–	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	RR	48	–	–	dB
D.C. output offset voltage		$\|\Delta V_O\|$	–	–	250	mV

PACKAGE OUTLINE

13-lead SIL-bent-to-DIL; plastic power (SOT141C).

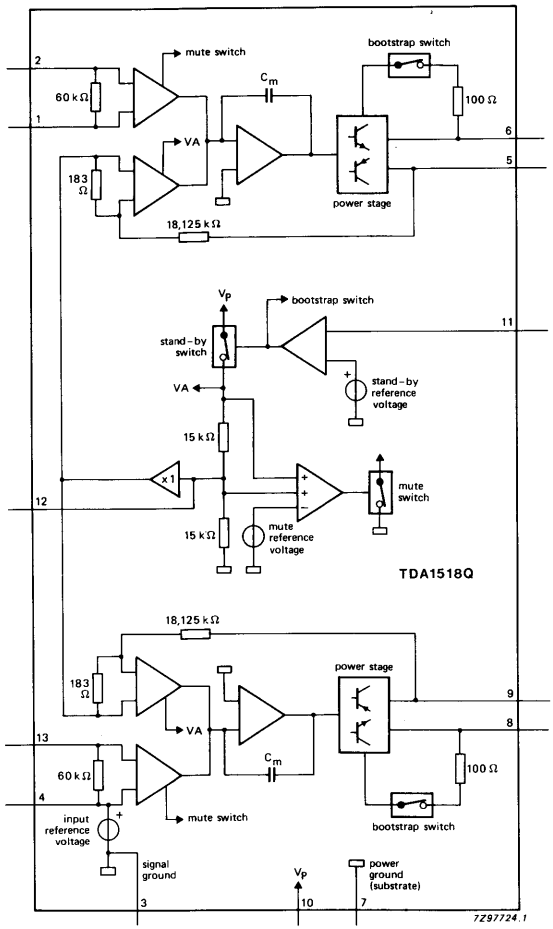


Fig. 1 Block diagram.

PINNING

1	−INV1	non-inverting input 1
2	INV	inverting input
3	GND1	ground (signal)
4	V_{ref}	reference voltage
5	OUT1	output 1
6	BS1	bootstrap 1
7	GND2	ground (substrate)
8	BS2	bootstrap 2
9	OUT2	output 2
10	V_P	supply voltage
11	M/SS	mute/stand-by switch
12	RR	supply voltage ripple rejection
13	−INV2	non-inverting input 2

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA1518Q contains two identical amplifiers with differential input stages. This device can be used for stereo or bridge applications. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
A.C. and d.c. short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}	–	15	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	–65	+150	°C

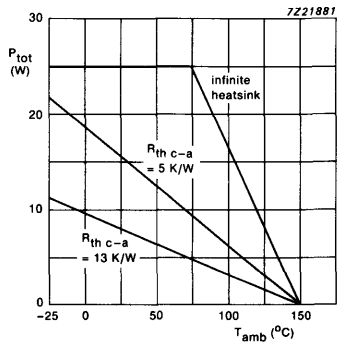


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS (note 1)

V_P = 14.4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	30	*	mA
D.C. output voltage at approximately $V_P/2$	note 3	V_O	–	6,8	–	V
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	200	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,0	–	6,4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	*	20	mV
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	250	mV
Stand-by condition		V_{sb}	0	–	2	V
D.C. current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

* Value to be fixed.

A.C. CHARACTERISTICS

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application	note 1					
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
	notes 4 and 5;					
	THD = 10%	P_o	6	7	–	W
Output power at	note 4;					
R_L = 2 Ω	THD = 0,5%	P_o	7,75	8,5	–	W
	THD = 10%	P_o	10	11	–	W
	notes 4 and 5;					
	THD = 10%	P_o	10,5	12,0	–	W
Low frequency roll-off	note 6;					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	50	60	75	kΩ
Noise output voltage:	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 9	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		G_v	–	0.1	1	dB

DEVELOPMENT DATA

A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application	note 10					
Output power	THD = 0,5%	P_o	15,5	17,0	–	W
	THD = 10%	P_o	20	22	–	W
	note 5; THD = 10%	P_o	21	24	–	W
Output power at V_P = 13,2 V	THD = 0,5%	P_o	–	13.5	–	W
	THD = 10%	P_o	–	17	–	W
	note 5; THD = 10%	P_o	–	19	–	W
Power bandwidth	THD = 0,5% P_o = 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 6; –3 dB	f_L	–	45	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	45	46	47	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	25	30	38	kΩ
Noise output voltage:	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	200	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	350	700	μV
mute	note 9	$V_{no(rms)}$	–	120	–	μV
Switch-on/switch-off behaviour		dV/dt	–	–	*	V/ms

Notes to the characteristics

1. All characteristics, for stereo application are measured using the circuit shown in Fig. 3.
2. The circuit is d.c. adjusted at V_P = 6 V to 18 V and a.c. operating at V_P = 8,1 V to 18 V.
3. At 18 V < V_P < 30 V the d.c. output voltage ≤ $V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. With bootstrap and a 100 kΩ resistor from pin 12 to the positive supply voltage (V_P), value of bootstrap capacitor is 47 μF.
6. Frequency response externally fixed.
7. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 1 kHz and 0 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).
10. All characteristics, for BTL application are measured using the circuit shown in Fig. 4.

* Value to be fixed.

APPLICATION INFORMATION

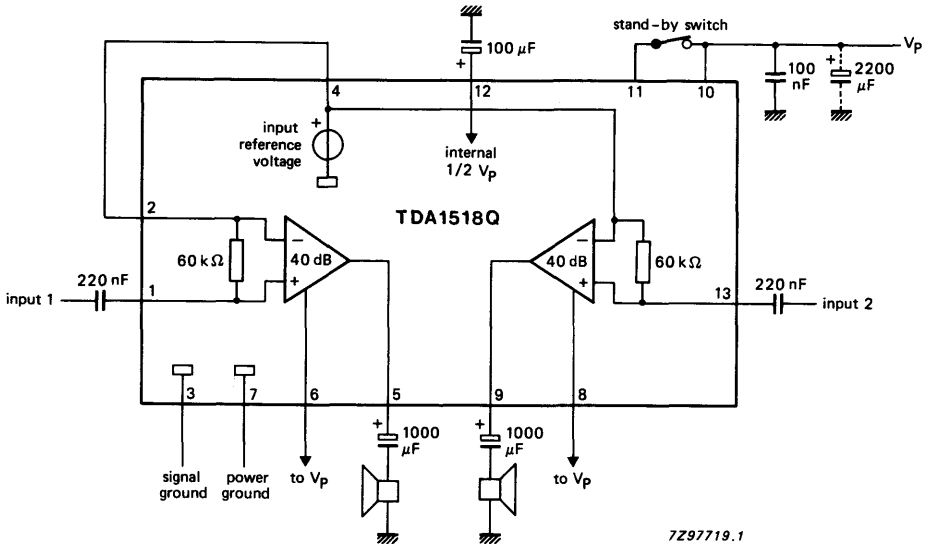


Fig. 3 Stereo application circuit diagram.

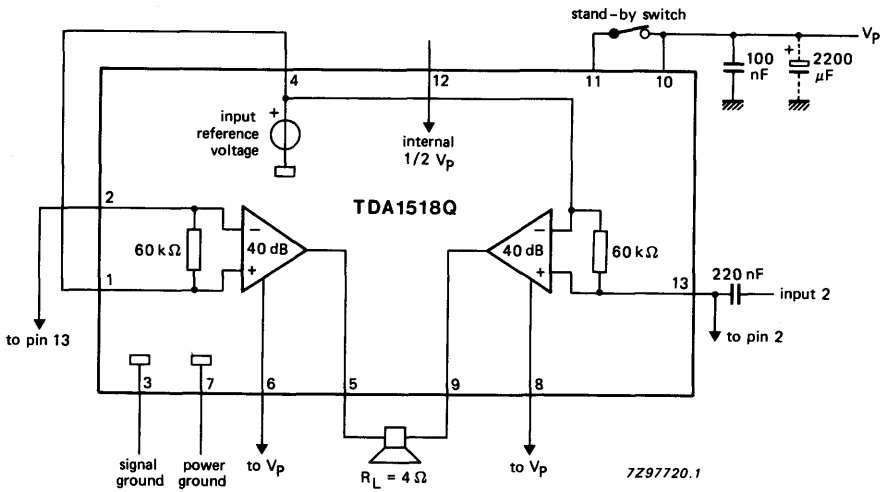


Fig. 4 BTL application circuit diagram (without bootstrapping).

DEVELOPMENT DATA

2 × 6 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1519 is an integrated class-B dual output amplifier in a 9-lead single in-line (SIL) plastic medium power package. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- High output power
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Compatible with TDA1517 (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	2,5	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance		$\|Z_I\|$	50	–	–	kΩ
Output power	THD = 0,5%; 4 Ω	P_o	–	5	–	W
	THD = 10%; 4 Ω	P_o	–	6	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
Supply voltage ripple rejection	f = 100 Hz	SVRR	40	–	–	dB
	f = 1 kHz to 10 kHz	SVRR	48	–	–	dB
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

9-lead SIL-bent-to-DIL; plastic (SOT110B).

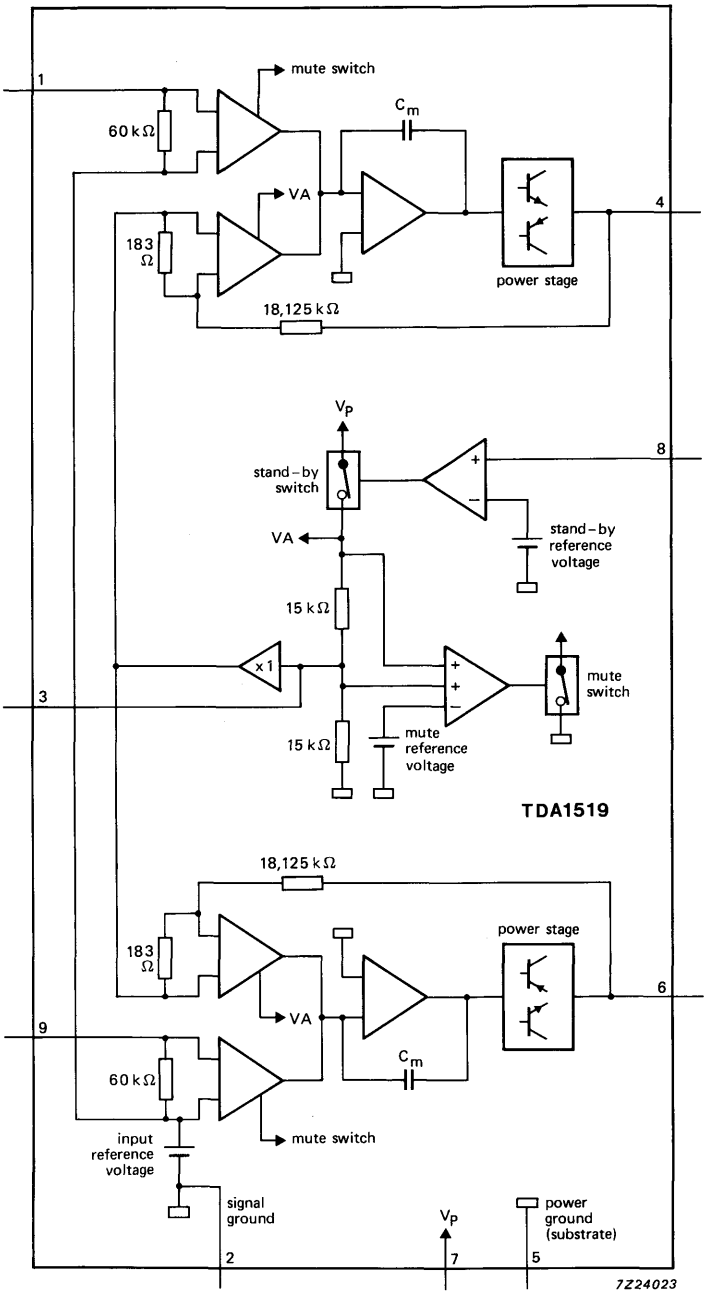


Fig. 1 Block diagram.

PINNING

1	INV1	non-inverting input 1
2	GND1	ground (signal)
3	SVRR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	supply voltage
8	M/SS	mute/stand-by switch
9	−INV2	non-inverting input 2

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA1519 contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	4	A
Repetitive peak output current		I_{ORM}	–	2,5	A
Total power dissipation	see Fig. 2	P_{tot}	–	15	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	−65	+ 150	°C

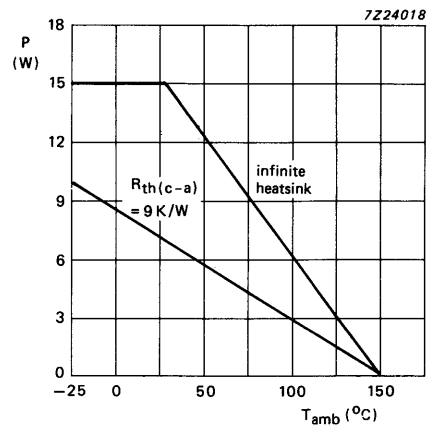


Fig. 2 Power derating curve.

DC CHARACTERISTICS (note 1)

V_P = 14,4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	40	80	mA
DC output voltage	note 3	V_O	–	6,95	–	V
Mute/stand-by switch						
Switch-on voltage level	see Fig. 3	V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,3	–	6,4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	–	20	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

DEVELOPMENT DATA

AC CHARACTERISTICS (note 1)

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0,1	–	%
Low frequency roll-off	note 5;					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection	note 6					
ON	f = 100 Hz	SVRR	40	–	–	dB
ON	f = 10 Hz to 10 kHz	SVRR	48	–	–	dB
mute		SVRR	48	–	–	dB
stand-by		SVRR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage	note 7;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 8	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		$\|\Delta G_v\|$	–	0,1	1	dB

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig. 4.
2. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8,5 V to 18 V.
3. At 18 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. Frequency response externally fixed.
6. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
7. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
8. Noise output voltage independent of R_S (V_I = 0 V).

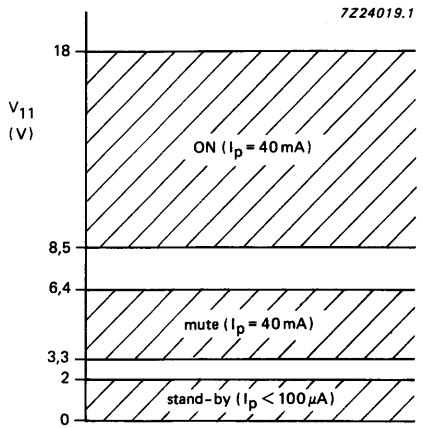


Fig. 3 Stand-by, mute and ON conditions.

APPLICATION INFORMATION

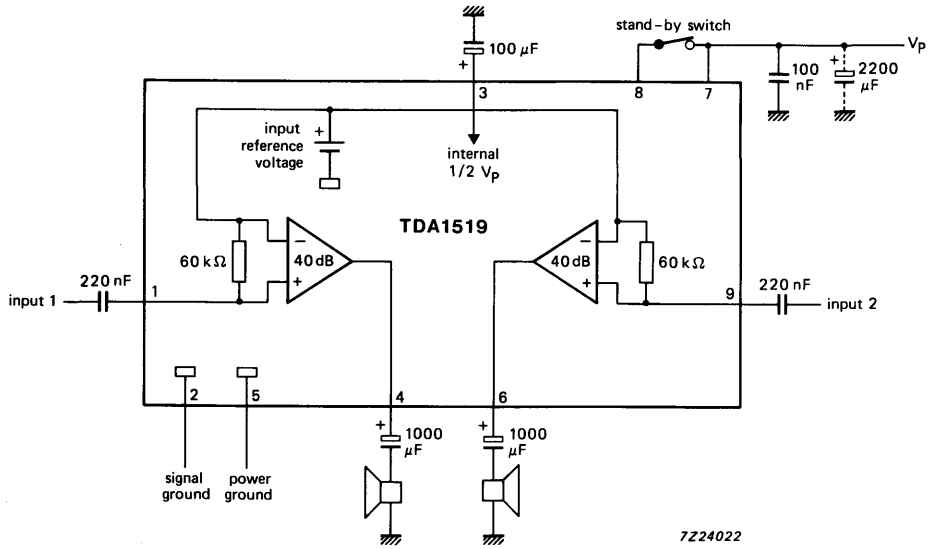


Fig. 4 Application circuit diagram.

DEVELOPMENT DATA

22 W BTL OR 2 × 11 WATT STEREO CAR RADIO POWER AMLIFIER

GENERAL DESCRIPTION

The TDA1519A is an integrated class-B dual output amplifier in a 9-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications.

Features

- Requires very few external components for Bridge Tied Load (BTL)
- Stereo or BTL application
- High output power
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1519B (except output power)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6.0	14.4	18.0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 10%; 4 Ω	P_o	–	6	–	W
	THD = 10%; 2 Ω	P_o	–	11	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
BTL application						
Output power	THD = 10%; 4 Ω	P_o	–	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω					
	f = 100 Hz	RR	34	–	–	dB
	f = 1 kHz to 10 kHz	RR	48	–	–	dB
DC output offset voltage		$\|\Delta V_O\|$	–	–	250	mV
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINES

9-lead SIL; plastic power (SOT131).
9-lead SIL-bent-to-DIL; plastic power (SOT157).

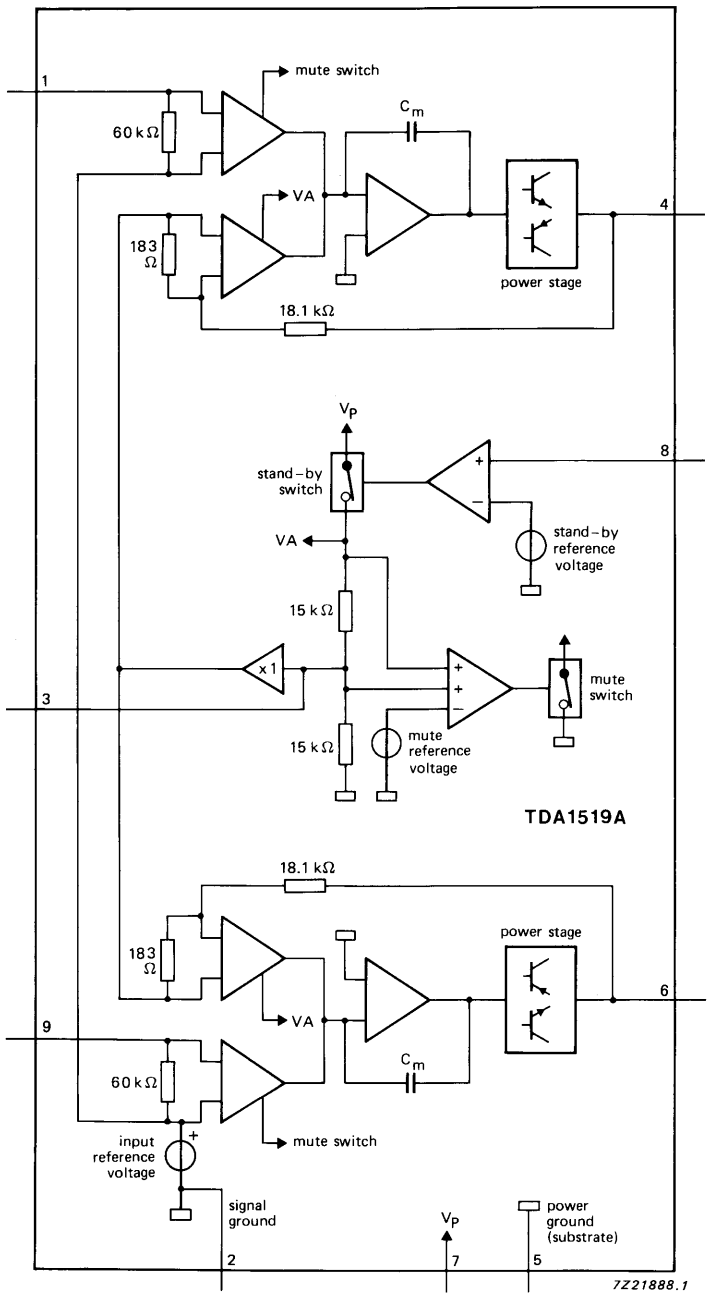


Fig.1 Block diagram.

PINNING

1	NINV	non-inverting input
2	GND1	ground (signal)
3	RR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	positive supply voltage
8	M/SS	mute/stand-by switch
9	INV	inverting input

FUNCTIONAL DESCRIPTION

The TDA1519A contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- Low stand-by current ($< 100\ \mu A$)
- Low mute/stand-by switching current (low cost supply switch)
- Mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Total power dissipation	see Fig.2	P_{tot}	–	25	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	−65	+150	°C

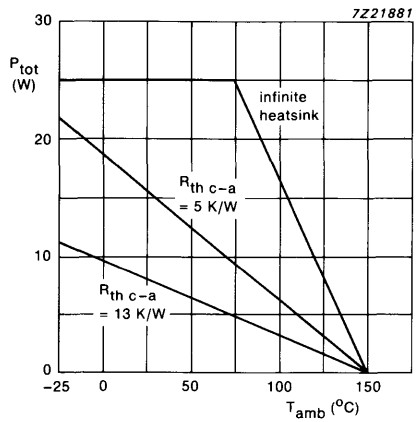


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	40	80	mA
DC output voltage	note 2	V_O	–	6.95	–	V
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	–	20	mV
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

DEVELOPMENT DATA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application						
Output power	note 3					
	THD = 0.5%	P_o	4	5	–	W
	THD = 10%	P_o	5.5	6.0	–	W
Output power at R_L = 2 Ω	note 3					
	THD = 0.5%	P_o	7.5	8.5	–	W
	THD = 10%	P_o	10	11	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Low frequency roll-off	note 4					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	40	–	–	dB
ON	notes 5 and 7	RR	45	–	–	dB
mute	notes 5, 6 and 7	RR	45	–	–	dB
stand-by	notes 5, 6 and 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)	note 8					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 9	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	0.1	1	dB

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.4; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application						
Output power	note 3					
	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	note 3					
	THD = 0.5%	P_o	–	13	–	W
	THD = 10%	P_o	–	17.5	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5%; P_o = −1 dB; w.r.t. 15 W	B_W	–	35 to 15 000	–	Hz
Low frequency roll-off	note 4					
	−1 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	45	46	47	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	34	–	–	dB
ON	notes 5 and 7	RR	48	–	–	dB
mute	notes 5, 6 and 7	RR	48	–	–	dB
stand-by	notes 5, 6 and 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	25	30	38	kΩ
Noise output voltage (RMS value)	note 8					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	200	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	350	700	μV
mute	note 9	$V_{no(rms)}$	–	180	–	μV

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ≤ $V_P/2$.
3. Output power is measured directly at the output pins of the IC.
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
6. Frequency f = 100 Hz.
7. Frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).

DEVELOPMENT DATA

APPLICATION INFORMATION

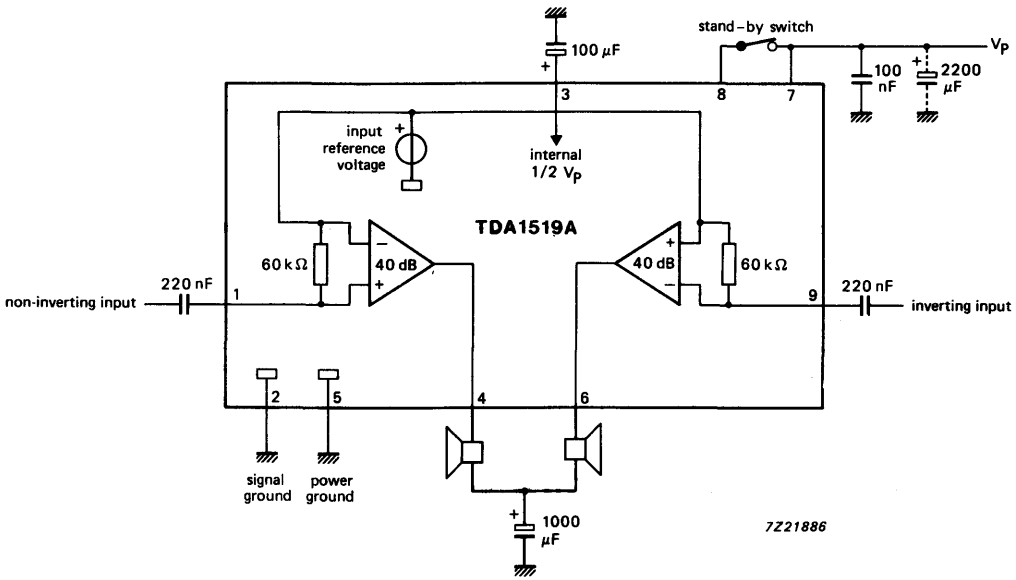


Fig.3 Stereo application circuit diagram.

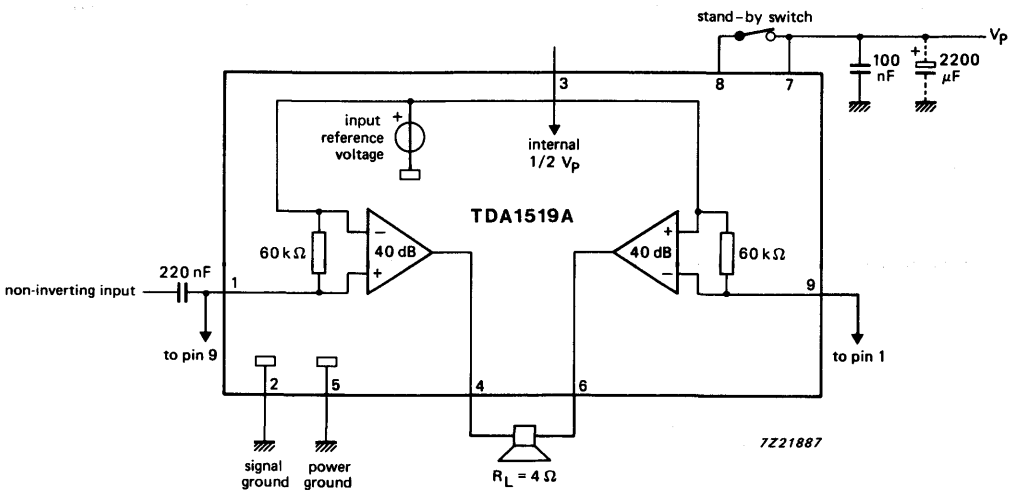


Fig.4 BTL application circuit diagram.

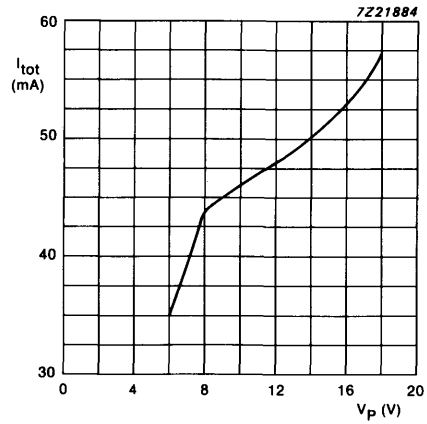


Fig.5 Total quiescent current (I_{tot}) as a function of supply voltage (V_P).

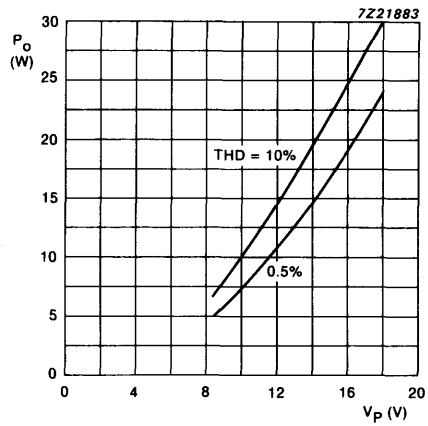


Fig.6 Output power (P_o) as a function of supply voltage (V_P) for BTL application at $R_L = 4\ \Omega$; f = 1 kHz.

DEVELOPMENT DATA

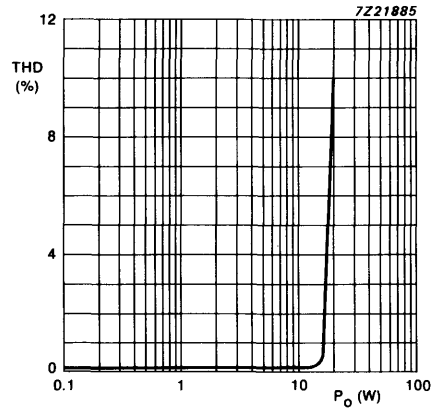


Fig.7 Total harmonic distortion (THD) as a function of output power (P_o) for BTL application at $R_L = 4\ \Omega$; f = 1 kHz.

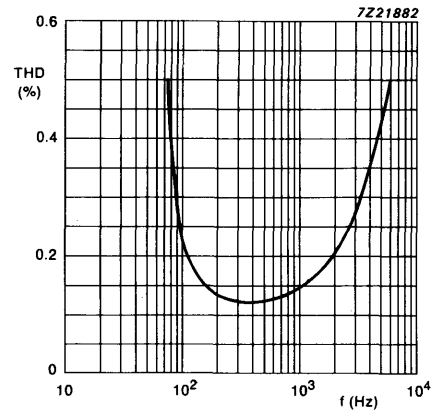


Fig.8 Total harmonic distortion (THD) as a function of operating frequency (f) for BTL application at $R_L = 4\ \Omega$; $P_o = 1$ W.

12 W BTL OR 2 × 6 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1519B is an integrated class-B dual output amplifier in a 9-lead single in-line (SIL) plastic medium power package. The device is primarily developed for car radio applications.

Features

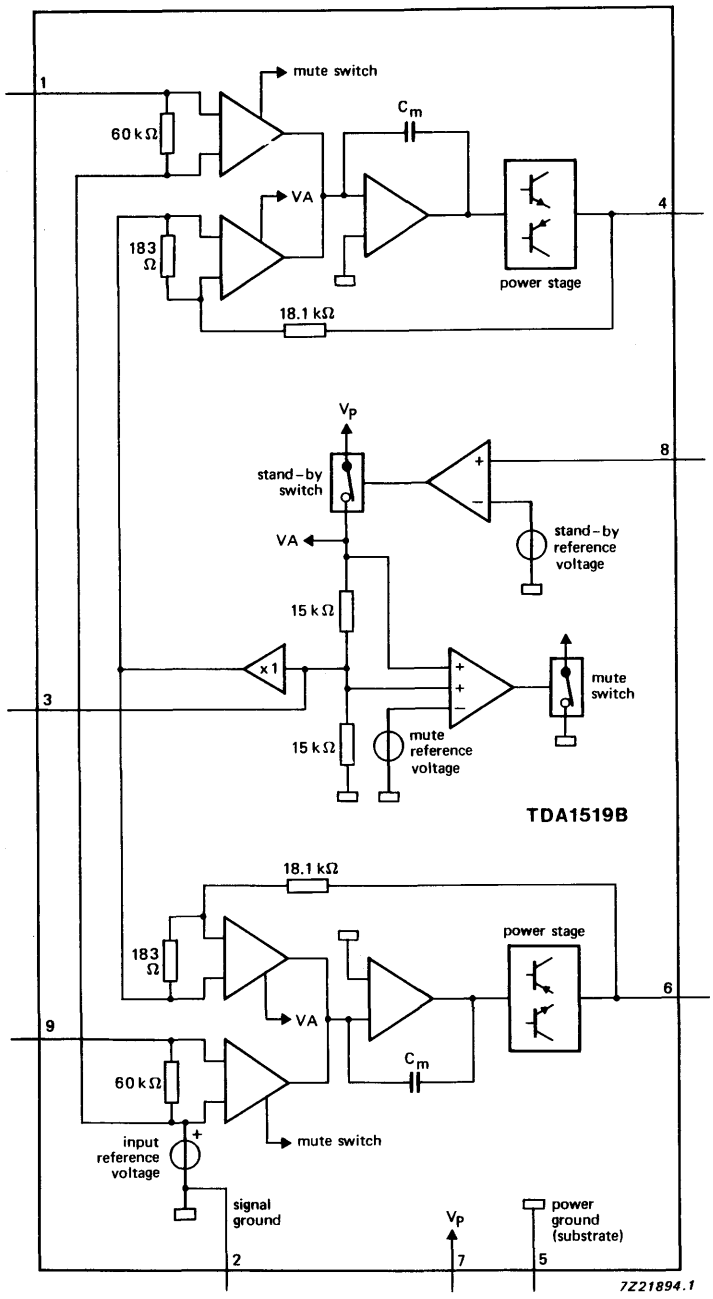
- Requires very few external components for Bridge Tied Load (BTL)
- Stereo or BTL application
- High output power
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1519A (except output power)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6.0	14.4	18.0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	2.5	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 5%; 4 Ω	P_o	–	5	–	W
	THD = 10%; 4 Ω	P_o	–	6	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
BTL application						
Output power	THD = 10%; 8 Ω	P_o	–	12	–	W
Supply voltage ripple rejection	R_S = 0 Ω					
	f = 100 Hz	RR	34	–	–	dB
	f = 1 kHz to 10 kHz	RR	48	–	–	dB
DC output offset voltage		$\|\Delta V_O\|$	–	–	250	mV
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).



PINNING

1	NINV	non-inverting input
2	GND1	ground (signal)
3	RR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	positive supply voltage
8	M/SS	mute/stand-by switch
9	INV	inverting input

Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The TDA1519B contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- Low stand-by current ($< 100\ \mu A$)
- Low mute/stand-by switching current (low cost supply switch)
- Mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	4	A
Repetitive peak output current		I_{ORM}	–	2.5	A
Total power dissipation	see Fig.2	P_{tot}	–	15	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	−65	+150	°C

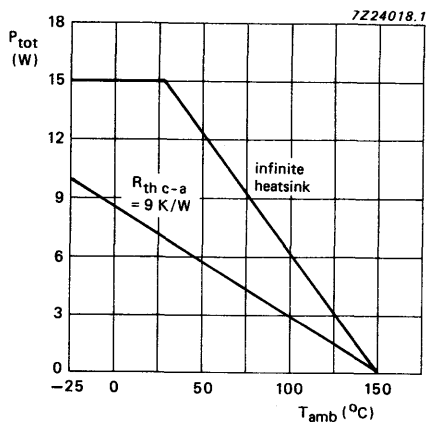


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	40	80	mA
DC output voltage	note 2	V_O	–	6.95	–	V
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	–	20	mV
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application						
Output power	note 3					
	THD = 0.5%	P_o	4	5	–	W
	THD = 10%	P_o	5.5	6.0	–	W
Output power at V_P = 13.2 V	note 3					
	THD = 0.5%	P_o	–	3.5	–	W
	THD = 10%	P_o	–	4.8	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Low frequency roll-off	note 4					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	40	–	–	dB
ON	notes 5 and 7	RR	45	–	–	dB
mute	notes 5, 6 and 7	RR	45	–	–	dB
stand-by	notes 5, 6 and 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)	note 8					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 9	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	0.1	1	dB

DEVELOPMENT DATA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.4; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application						
Output power	note 3					
	THD = 0.5%	P_o	8	10	–	W
	THD = 10%	P_o	11	12	–	W
Output power at V_P = 13.2 V	note 3					
	THD = 0.5%	P_o	–	7.5	–	W
	THD = 10%	P_o	–	10	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5%; P_o = −1 dB; w.r.t. 15 W	B_W	–	35 to 15 000	–	Hz
Low frequency roll-off	note 4					
	−1 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	45	46	47	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	34	–	–	dB
ON	notes 5 and 7	RR	48	–	–	dB
mute	notes 5, 6 and 7	RR	48	–	–	dB
stand-by	notes 5, 6 and 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	25	30	38	kΩ
Noise output voltage (RMS value)	note 8					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	200	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	350	700	μV
mute	note 9	$V_{no(rms)}$	–	180	–	μV

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
3. Output power is measured directly at the output pins of the IC.
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
6. Frequency f = 100 Hz.
7. Frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).

APPLICATION INFORMATION

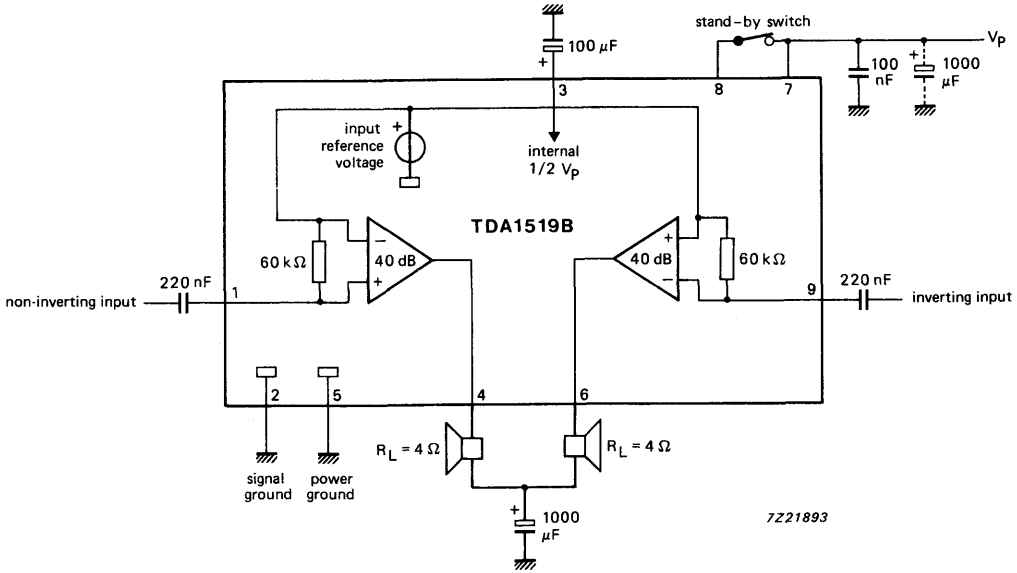


Fig.3 Stereo application circuit diagram.

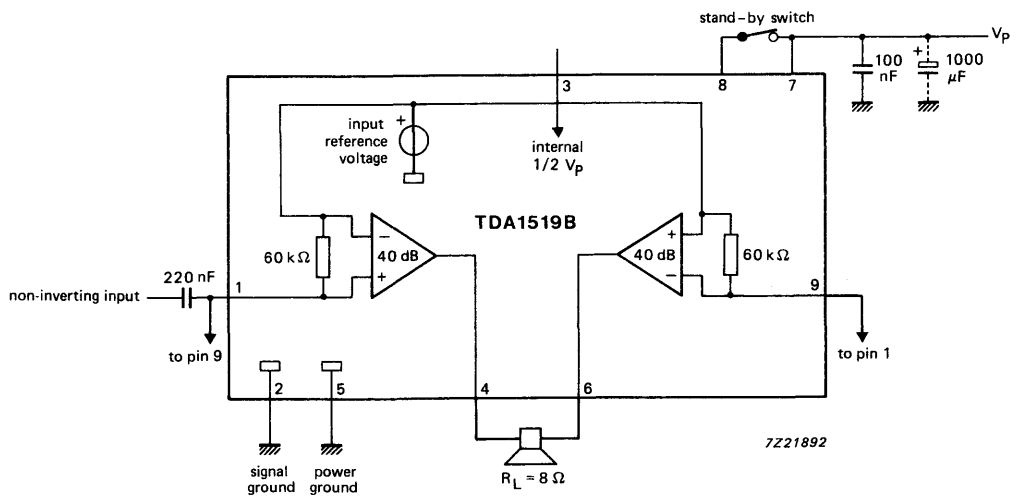


Fig.4 BTL application circuit diagram.

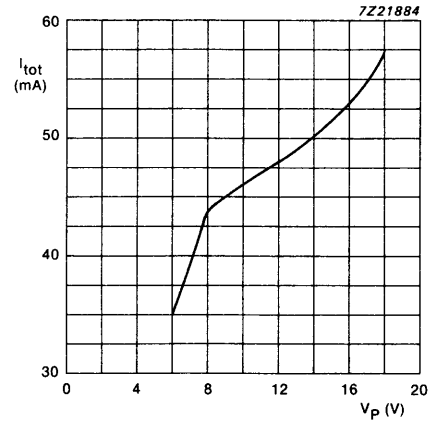


Fig.5 Total quiescent current (I_{tot}) as a function of supply voltage (V_P).

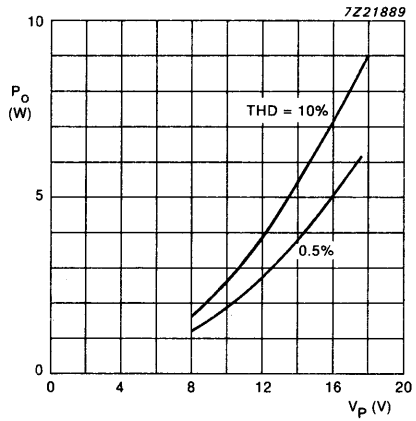


Fig.6 Output power (P_o) as a function of supply voltage (V_P) for stereo application at $R_L = 4\ \Omega$, f = 1 kHz.

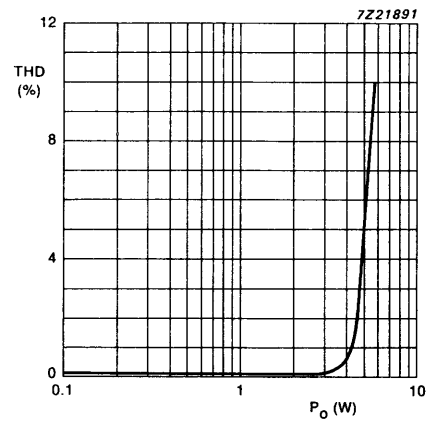


Fig.7 Total harmonic distortion (THD) as a function of output power (P_o) for stereo application at $R_L = 4\ \Omega$, f = 1 kHz.

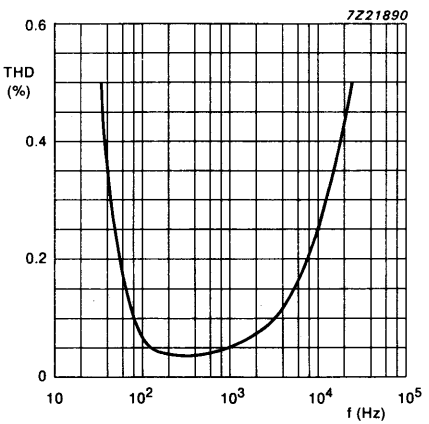


Fig.8 Total harmonic distortion (THD) as a function of operating frequency (f) for stereo application at $R_L = 4\ \Omega$, $P_o = 1$ W.

DEVELOPMENT DATA

20 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1520B is an integrated hi-fi audio power amplifier designed for use with non-stabilized symmetrical or stabilized asymmetrical power supplies in mains-fed applications (e.g. stereo radio, stereo TV sound and cassette recorder).

Features

- Low offset voltage at output (suitable for BTL application)
- Low cross-over and secondary cross-over distortion
- Low intermodulation and transient intermodulation distortion
- Low harmonic distortion
- Good hum suppression
- High slew rate
- No switch-on/switch-off plop
- Thermal protection

QUICK REFERENCE DATA (note 1)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	15	–	50	V
Total quiescent current		I_{tot}	22	60	105	mA
Output power at THD = 0,5%		P_o	20	22	–	W
Input impedance		Z_I	1000	–	–	kΩ
Signal plus noise to noise ratio at P_O = 50 mW	note 2	(S+N)/N	70	75	–	dB
Supply voltage ripple rejection at R_S = 0 Ω	f = 100 Hz	SVRR	45	60	–	dB
	f = 10 kHz	SVRR	45	80	–	dB

Notes to the Quick Reference Data

1. All values measured from test circuit Fig.6; V_P = 33 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.
2. Bandwidth is 20 Hz to 20 kHz; R_S = 2 kΩ (RMS value).

PACKAGE OUTLINES

TDA1520B: 9-lead SIL; plastic power (SOT131).
TDA1520BQ: 9-lead SIL-bent-to-DIL; plastic power (SOT157).

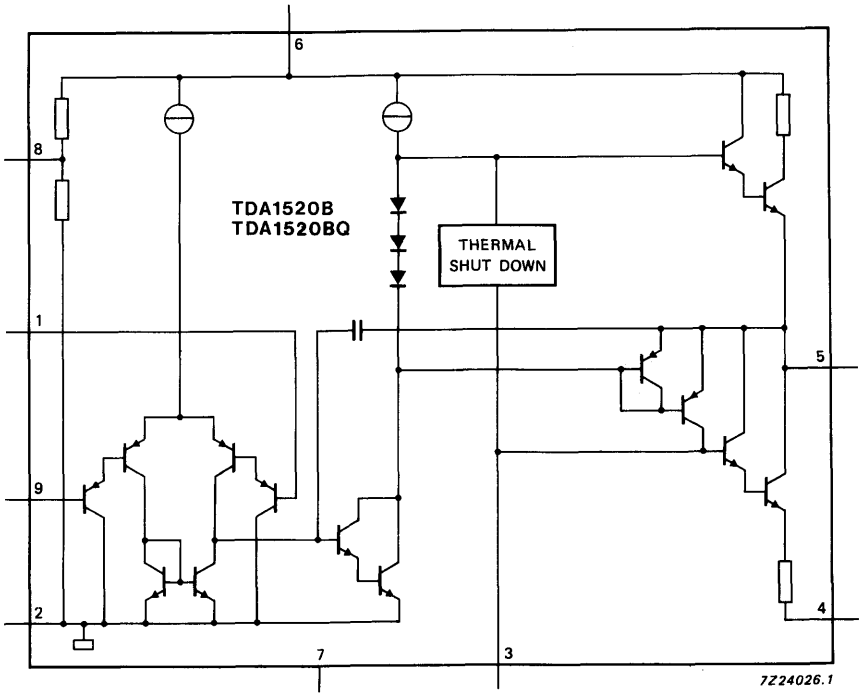


Fig. 1 Block diagram.

PINNING

1 Non-inverting input
2 Input ground (substrate)
3 Compensation
4 Negative supply (ground)
5 Output
6 Positive supply (V_P)
7 Not connected
8 Supply voltage ripple rejection
9 Inverting input (feedback)

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	note 1	V_P	–	50	V
Input voltage					
pins 1 to 2		V_I	–	25	V
pins 9 to 2		V_I	–	25	V
Repetitive peak output current		I_{ORM}	–	4	A
Non-repetitive peak output current	note 2	I_{OSM}	–	5	A
Total power dissipation		P_{tot}	see Fig.2		
AC short-circuit time of the load impedance during signal drive at					
$V_P = \pm 20$ V	symmetrical supply; $R_S = 2\ \Omega$; $f = \geqslant 20$ Hz	T_{sc}	–	1	hour
$V_P = 30$ V	asymmetrical supply; $R_S = 4\ \Omega$	T_s	–	1	hour
Operating ambient temperature range		T_{amb}	see Fig.2		
Storage temperature range		T_{stg}	–65	+ 150	°C

Notes to the Ratings

1. Minimum rise time of the supply must be $\geqslant 20$ ms.
2. Maximum peak current is defined by the internal protection circuits.

POWER DISSIPATION AND HEATSINK INFORMATION

The maximum theoretical power dissipation with a stabilized power supply is ($V_P = 33$ V and $R_L = 4\ \Omega$):

$$\frac{V_P^2}{2\pi^2 R_L} = 13.8\ \text{W}.$$

Worst case power dissipation with a non-stabilized power supply is (regulation factor of 15%; over voltage of 10% and R_L min. = 0.8 x R_L typ.; V_{PL} is the loaded supply voltage):

$$\frac{(1.1 \times V_{PL})^2}{2\pi^2 R_{L\,\text{min.}}} = 23.4\ \text{W}.$$

With a maximum ambient temperature of 50 °C and a maximum crystal temperature of 150 °C, the required thermal resistance is:

$$R_{th\,j\text{-}a} = \frac{150 - 50}{23.4} = 4.3\ \text{K/W}.$$

The thermal resistance of the encapsulation is $\leqslant 2.5$ K/W, therefore the thermal resistance of the heatsink must be < 1.8 K/W.

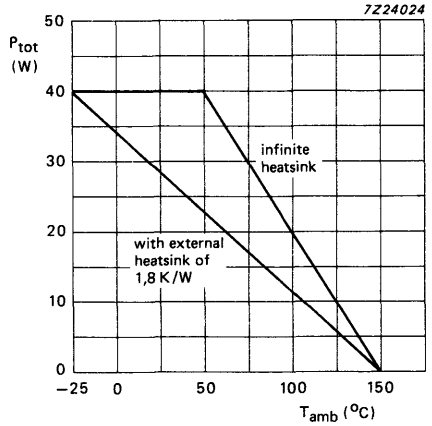


Fig.2 Power derating curve.

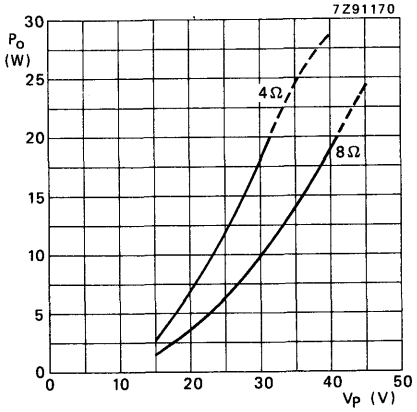


Fig.3 Output power (P_O) versus supply voltage (V_P); f = 1 kHz; d_{tot} = 0.5%; G_V = 30 dB.

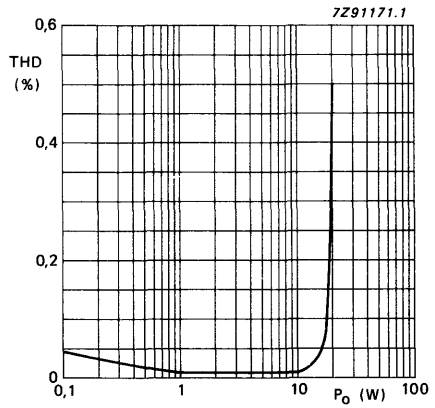


Fig.4 Total harmonic distortion (THD) versus output power (P_O); V_P = 33 V; R_L = 4 Ω; f = 1 kHz.

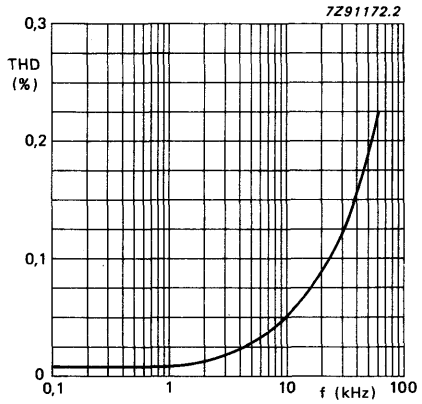


Fig.5 Total harmonic distortion (THD) versus operating frequency (f); V_P = 33 V; R_L = 4 Ω; P_O = 10 W (constant).

CHARACTERISTICS

V_P = 33 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified; measured from test circuit, Fig. 6.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	15	–	50	V
Total quiescent current		I_P	22	60	105	mA
Peak output current		I_{OM}	–	–	3,2	A
Power output at THD = 0.5%	note 1	P_O	20	22	–	W
Total harmonic distortion at P_O = 12 W	note 1	THD	–	0.01	0.1	%
Power bandwidth at THD = 0.5%	P_O = 50 mW to 10 W	B	–	20 to 20 000	–	Hz
Input voltage at P_O = 20 W	note 2	V_I	225	290	325	mV
Input impedance	note 3	Z_I	1000	–	–	kΩ
Signal plus noise to noise ratio at P_O at 50 mW	note 4	(S+N)/N	70	75	–	dB
Offset voltage		$\lvert V_{5-8} \rvert$	0	± 10	± 100	mV
Input offset current		I_{os}	–	0	1	μA
Output impedance		Z_O	–	–	0.1	Ω
Supply voltage ripple rejection at R_S = 0 Ω	f = 100 Hz	SVRR	45	60	–	dB
	f = 10 kHz	SVRR	45	80	–	dB
Intermodulation distortion at P_O = 10 W		d_{IM}	–	0.02	–	%
Transient intermodulation distortion	note 5	d_{TIM}	–	0.01	–	%
Slew rate		SR	–	6	–	V/μs

Notes to the Characteristics

1. Output power is measured directly at the output pin.
2. The closed-loop gain is determined by external resistors and is variable between 20 to 40 dB.
3. Input impedance in the test circuit is determined by the bias resistor R.
4. Unweighted noise measured in a bandwidth of 20 Hz to 20 kHz at R_S = 2 kΩ.
5. The transient intermodulation distortion is measured at P_O = 10 W. The input signal is a 3.18 kHz square-wave signal mixed with a 15 kHz sine-wave signal and a peak-to-peak voltage ratio of 4:1.

DEVELOPMENT DATA

APPLICATION INFORMATION

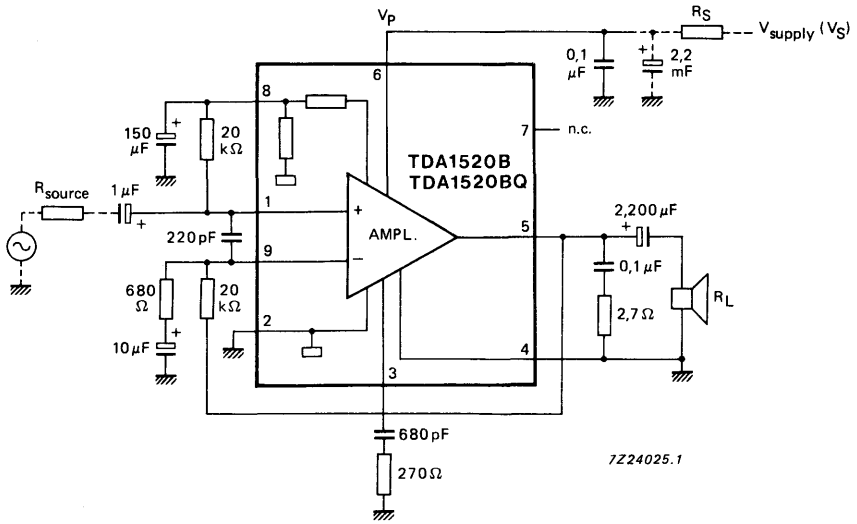


Fig. 6 Test and application diagram.

2 x 12 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521/TDA1521Q is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications			
Supply voltage range	V_P	± 7,5 to ± 20,0	V
Output power at THD = 0,5%, V_P = ± 16 V	P_o	typ. 12	W
Voltage gain	G_v	typ. 30	dB
Gain balance between channels	ΔG_v	typ. 0,2	dB
Ripple rejection	SVRR	typ. 60	dB
Channel separation	α	typ. 70	dB
Noise output voltage	$V_{no(rms)}$	typ. 70	μV

PACKAGE OUTLINES

TDA1521: 9-lead single in-line; plastic power (SOT131).
TDA1521Q: 9-lead SIL-bent-to-DIL; plastic power (SOT157).

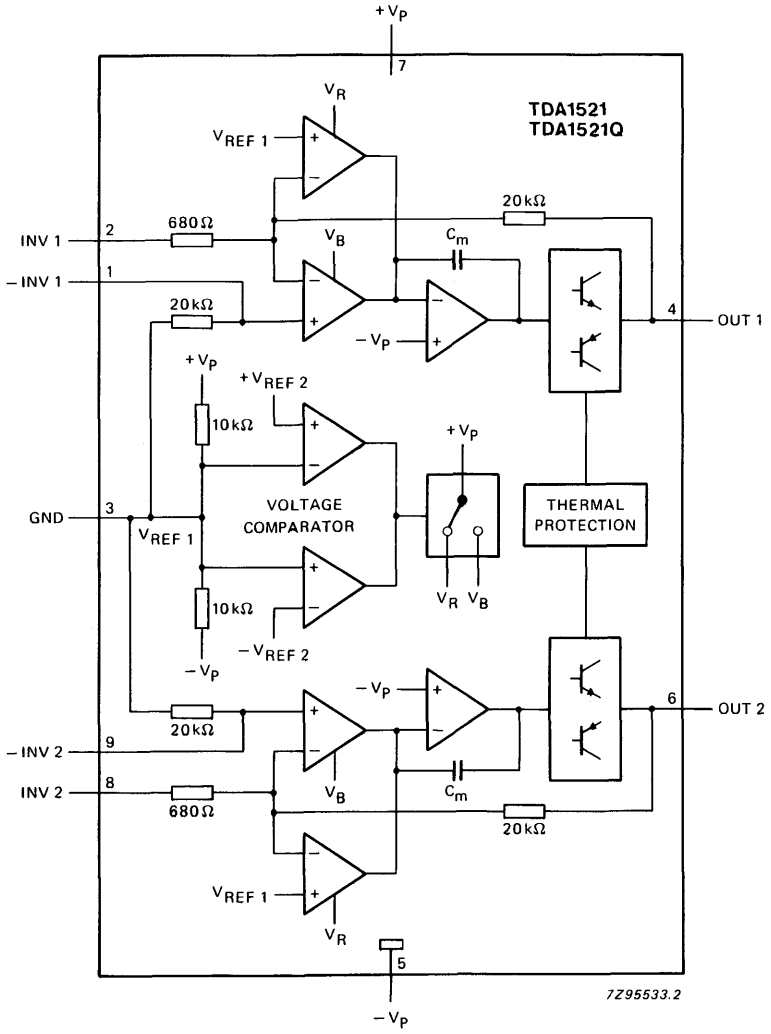


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) / ½ V_P (asymmetrical)
4	OUT1	output 1
5	$-V_P$	negative supply (symmetrical) / ground (asymmetrical)
6	OUT2	output 2
7	$+V_P$	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

This hi-fi stereo power amplifier is designed for mains fed applications. The circuit is designed for both symmetrical and asymmetrical power supply systems. An output power of 2 x 12 watts (THD = 0,5%) can be delivered into an 8 Ω load with a symmetrical power supply of ± 16 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread and very good balance between the amplifiers (0,2 dB).

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 13, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifiers remain in their DC operating mode but are isolated from the non-inverting inputs on pins 1 and 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 7	$V_P = V_{7-3}$	–	+ 20	V
	pin 5	$-V_P = V_{5-3}$	–	−20	V
Non-repetitive peak output current	pins 4 and 6	I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	−65	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note				
	symmetrical power supply	t_{sc}	–	1	hour
	asymmetrical power supply; $V_P < 32$ V (unloaded); $R_i \geqslant 4\ \Omega$	t_{sc}	–	1	hour

Note

For asymmetrical power supplies (at short circuiting of the load) the maximum supply voltage is limited to V_P = 28 V. If the total internal resistance of the supply (R_i) > 4 Ω, the maximum unloaded supply voltage is increased to 32 V.

DEVELOPMENT DATA

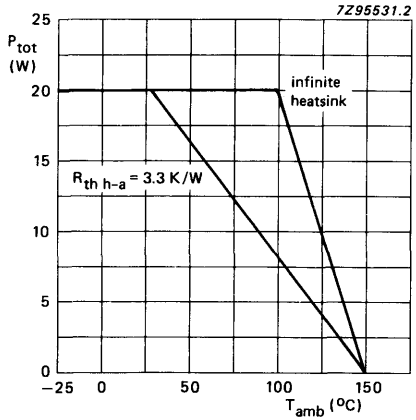


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j\text{-}c} = 2{,}5$ K/W

HEATSINK DESIGN EXAMPLE

With derating of 2,5 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = \pm 16$ V, the measured maximum dissipation is 14,6 W; then, for a maximum ambient temperature of 65 °C, the required thermal resistance of the heatsink is

$$R_{th\ h\text{-}a} = \frac{150 - 65}{14{,}6} - 2{,}5 = 3{,}3\ \text{K/W}$$

Note: The internal metal block (heatsink) has the same potential as pin 5 ($-V_P$)

DEVELOPMENT DATA

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	± 7,5	± 16,0	± 20,0	V
input mute mode		V_P	± 2,0	–	± 5,5	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: symmetrical power supply; test circuit as per Fig. 12; V_P = ± 16 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	10	12	–	W
	THD = 10%	P_o	12	15	–	W
Total harmonic distortion	P_o = 6 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5% note 1	B		20 to 20k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection	note 2	SVRR	40	60	–	dB
Channel separation	R_S = 0 Ω	α	46	70	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to ground	V_{OFF}	–	30	200	mV
Input mute mode: symmetrical power supply; test circuit as per Fig. 12; V_P = ± 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	9	30	40	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to ground	V_{OFF}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: asymmetrical power supply; test circuit as per Fig. 13; V_S = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B		40 to 20k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection		SVRR	40	50	–	dB
Channel separation	R_S = 0 Ω	α	–	45	–	dB

Notes to the characteristics

1. Power bandwidth at $P_{o\,max}$ −3 dB.
2. Ripple rejection at R_S = 0 Ω, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting inputs (pins 1 and 9) are disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 3).

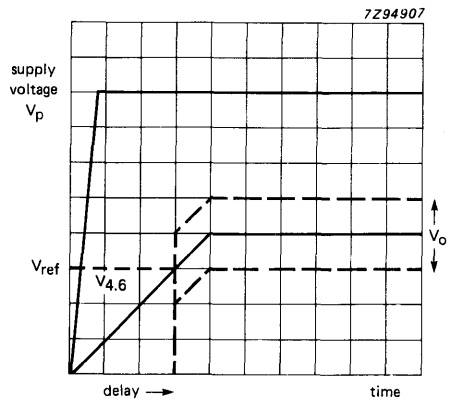


Fig. 3 Input mute circuit; time delay.

APPLICATION INFORMATION (continued)

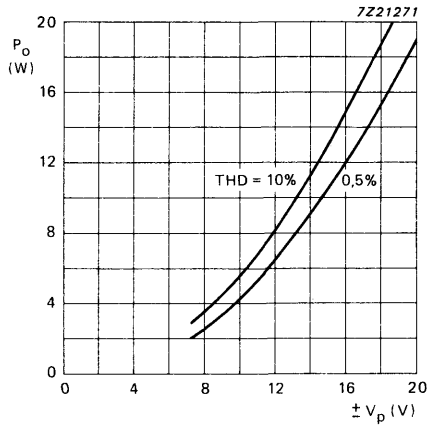


Fig. 4 Output power as a function of supply voltage, symmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

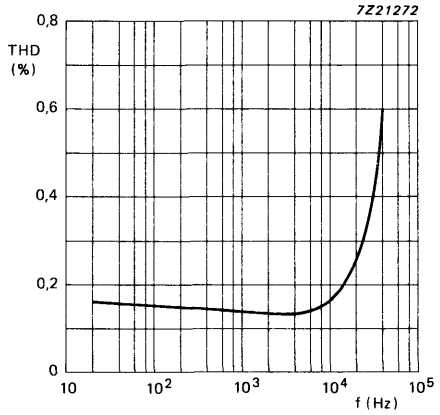


Fig. 5 Distortion as a function of frequency; symmetrical supply; $V_P = \pm 16$ V; $R_L = 8\ \Omega$; $P_o = 6$ W.

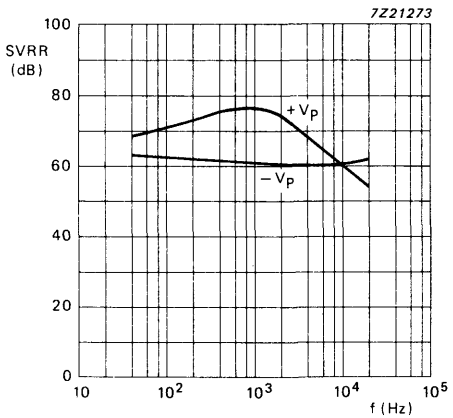


Fig. 6 Supply voltage ripple rejection; symmetrical supply; $V_P = \pm 16$ V; $V_{RR} = 200$ mV.

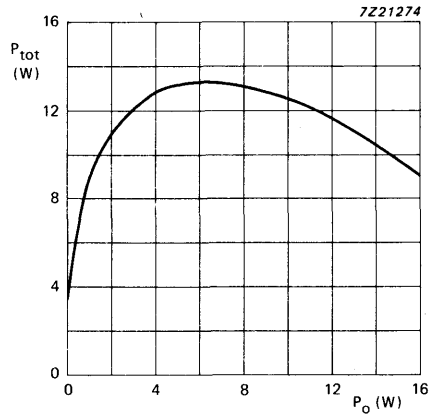


Fig. 7 Power dissipation as a function of output power; symmetrical supply; $V_P = \pm 16$ V; $R_L = 8\ \Omega$; f = 1 kHz.

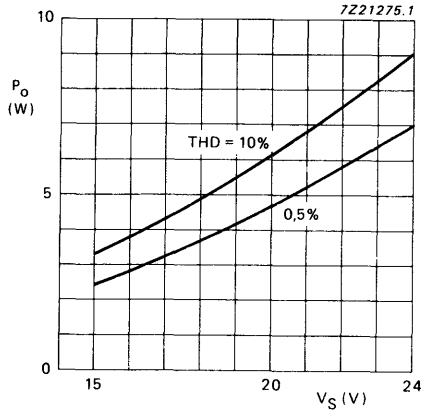


Fig. 8 Output power as a function of supply voltage; asymmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

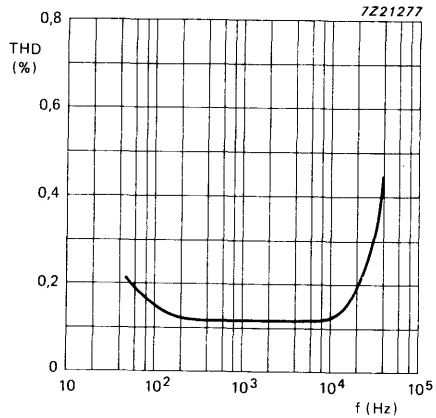


Fig. 9 Distortion as a function of frequency; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; $P_o = 4$ W.

DEVELOPMENT DATA

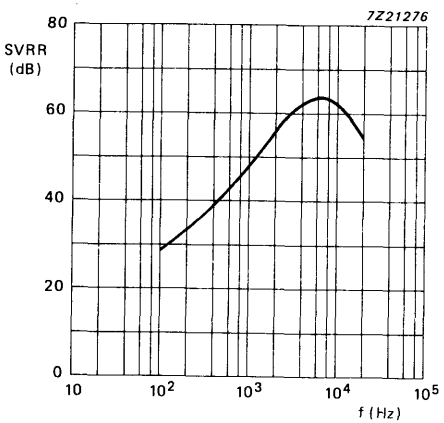


Fig. 10 Supply voltage ripple rejection; asymmetrical supply; $V_S = 24$ V; $V_{RR} = 200$ mV.

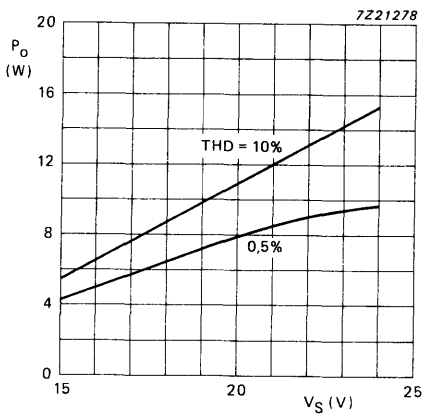
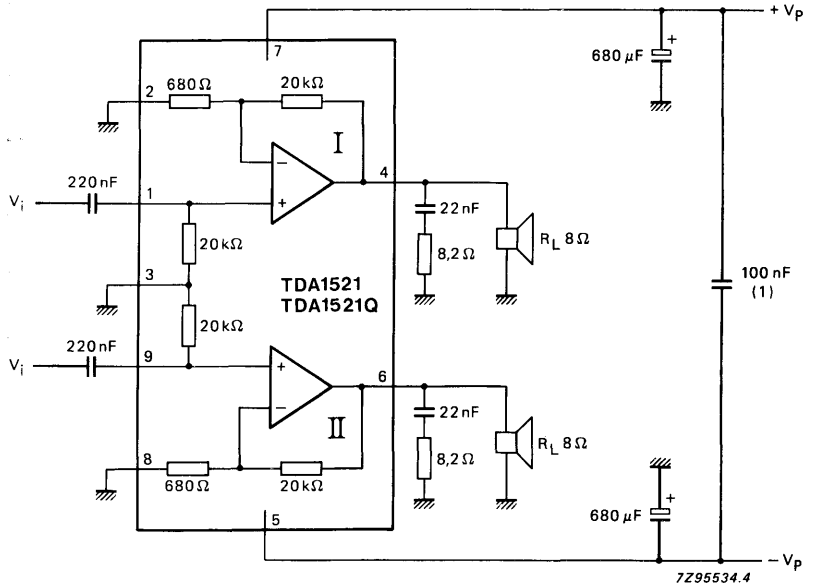
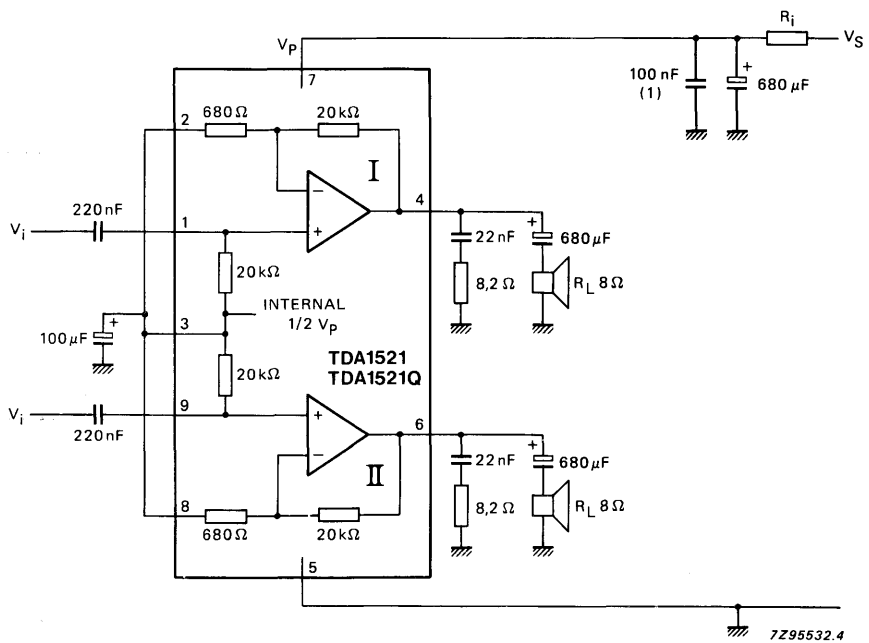


Fig. 11 Output power as a function of supply voltage; asymmetrical supply; $R_L = 4\ \Omega$; f = 1 kHz.



1 To be connected as close as possible to the IC

Fig. 12 Test and application circuit; symmetrical power supply.



1 To be connected as close as possible to the IC

Fig. 13 Test and application circuit; asymmetrical power supply.

2 x 6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521A is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications				
Supply voltage range	V_P		± 7,5 to ± 20,0	V
Output power at THD = 0,5%, V_P = ± 12 V	P_o	typ.	6	W
Voltage gain	G_v	typ.	30	dB
Gain balance between channels	ΔG_v	typ.	0,2	dB
Ripple rejection	SVRR	typ.	60	dB
Channel separation	α	typ.	70	dB
Noise output voltage	$V_{no(rms)}$	typ.	70	μV

PACKAGE OUTLINE

TDA1521A: 9-lead single in-line; plastic power (SOT 110B).

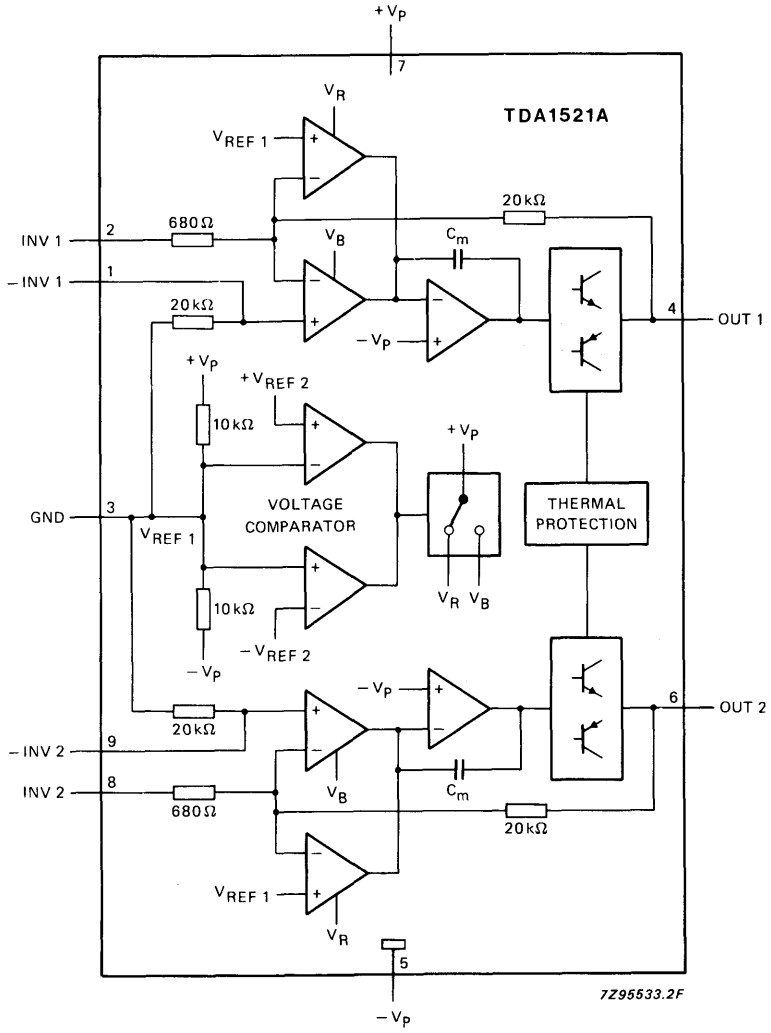


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) / ½ VP (asymmetrical)
4	OUT1	output 1
5	–VP	negative supply (symmetrical) / ground (asymmetrical)
6	OUT2	output 2
7	+ VP	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

This hi-fi stereo power amplifier is designed for mains fed applications. The circuit is designed for both symmetrical and asymmetrical power supply systems. An output power of 2 x 6 watts (THD = 0,5%) can be delivered into an 8 Ω load with a symmetrical power supply of ± 12 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread and very good balance between the amplifiers (0,2 dB).

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 12, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifiers remain in their DC operating mode but are isolated from the non-inverting inputs on pins 1 and 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 7	$V_P = V_{7-3}$	–	+ 20	V
	pin 5	$-V_P = V_{5-3}$	–	−20	V
Non-repetitive peak output current	pins 4 and 6	I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	−65	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note				
	symmetrical power supply	t_{sc}	–	1	hour
	asymmetrical power supply	t_{sc}	–	1	hour

Note

For asymmetrical power supplies (at short circuiting of the load) the maximum supply voltage is limited to V_P = 28 V.

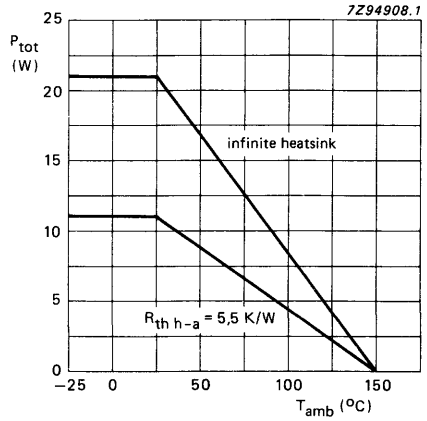


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j-c} = 6$ K/W

HEATSINK DESIGN EXAMPLE

With derating of 6 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = \pm 12$ V, the measured maximum dissipation is 7,8 W; then, for a maximum ambient temperature of 60 °C, the required thermal resistance of the heatsink is

$$R_{th\ h-a} = \frac{150 - 60}{7,8} - 6 = 5,5\ \text{K/W}$$

Note: The metal tab (heatsink) has the same potential as pin 5 ($-V_P$).

DEVELOPMENT DATA

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	± 7,5	± 12,0	± 20,0	V
input mute mode		V_P	± 2,0	–	± 5,5	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: symmetrical power supply; test circuit as per Fig. 11; V_P = ± 12 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8,0	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5% note 1	B		20 to 16 k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection	note 2	SVRR	40	60	–	dB
Channel separation	R_S = 0 Ω	α	46	70	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to ground	V_{OFF}	–	30	200	mV
Input mute mode: symmetrical power supply; test circuit as per Fig. 11; V_P = ± 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	9	30	40	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to ground	V_{OFF}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: asymmetrical power supply; test circuit as per Fig. 12; V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B		40 to 16 k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection		SVRR	40	50	–	dB
Channel separation	R_S = 0 Ω	α	–	45	–	dB

Notes to the characteristics

1. Power bandwidth at $P_{o\,max}$ −3 dB.
2. Ripple rejection at R_S = 0 Ω, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting inputs (pins 1 and 9) are disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 3).

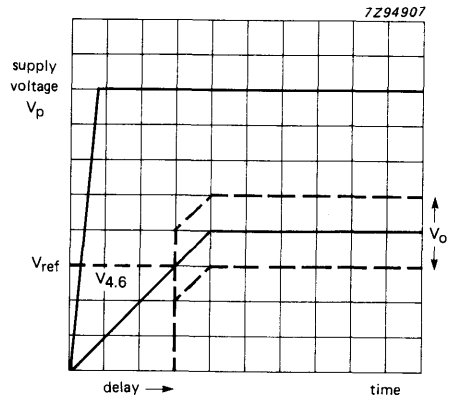


Fig. 3 Input mute circuit; time delay.

APPLICATION INFORMATION (continued)

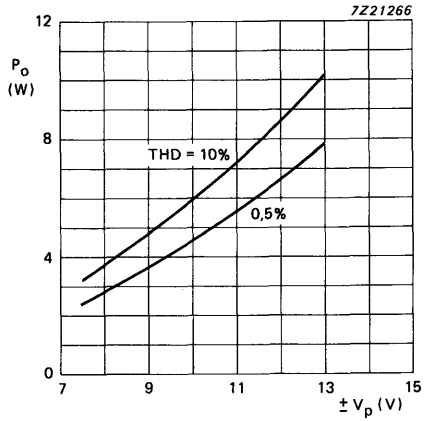


Fig. 4 Output power as a function of supply voltage; symmetrical supply; R_L = 8 Ω; f = 1 kHz.

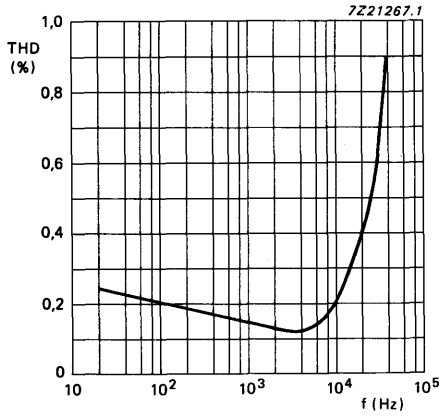


Fig. 5 Distortion as a function of frequency; symmetrical supply; V_p = ± 12 V; R_L = 8 Ω; P_o = 3 W.

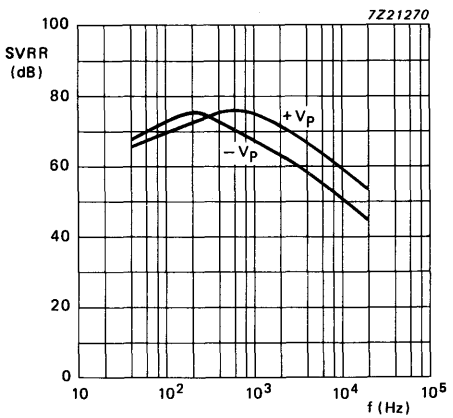


Fig. 6 Supply voltage ripple rejection; symmetrical supply, V_P = ± 12 V; V_{RR} = 200 mV.

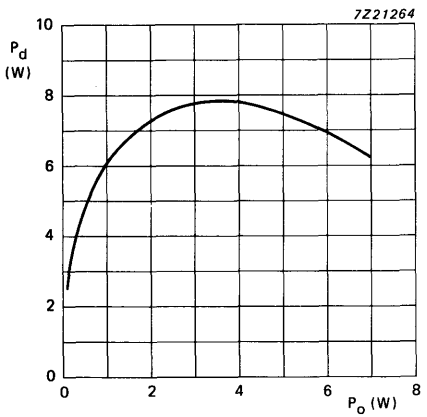


Fig. 7 Power dissipation as a function of output power; asymmetrical supply; V_S = 24 V; R_L = 8 Ω; f = 1 kHz.

APPLICATION INFORMATION (continued)

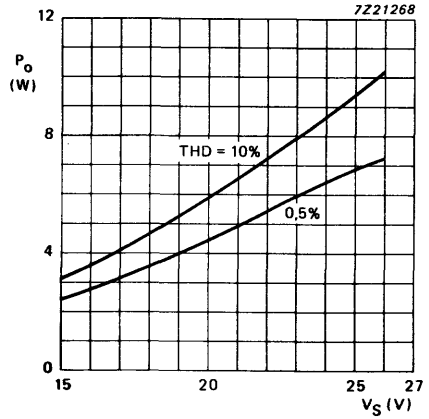


Fig. 8 Output power as a function of supply voltage; asymmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

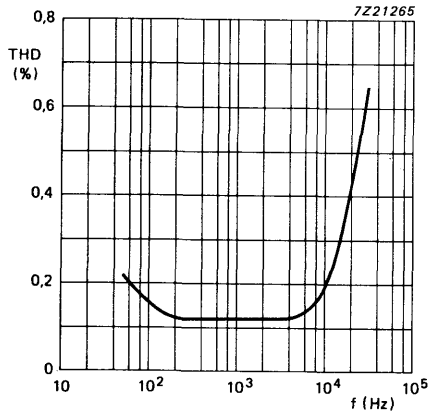


Fig. 9 Distortion as a function of frequency; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; $P_o = 3$ W.

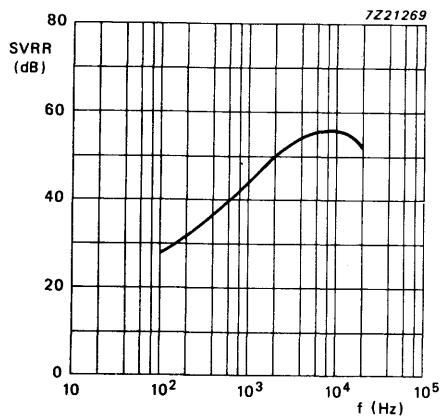
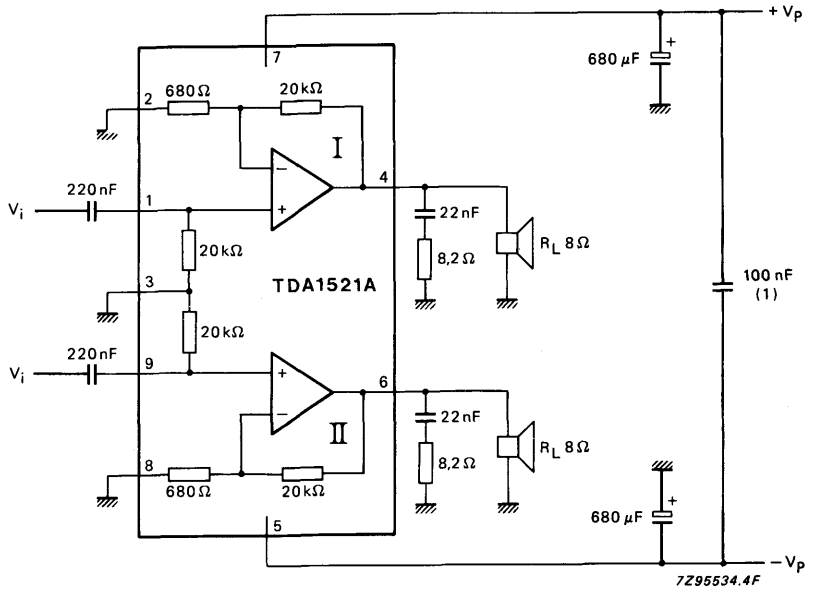


Fig. 10 Supply voltage ripple rejection; asymmetrical supply; $V_S = 24$ V; $V_{RR} = 200$ mW.

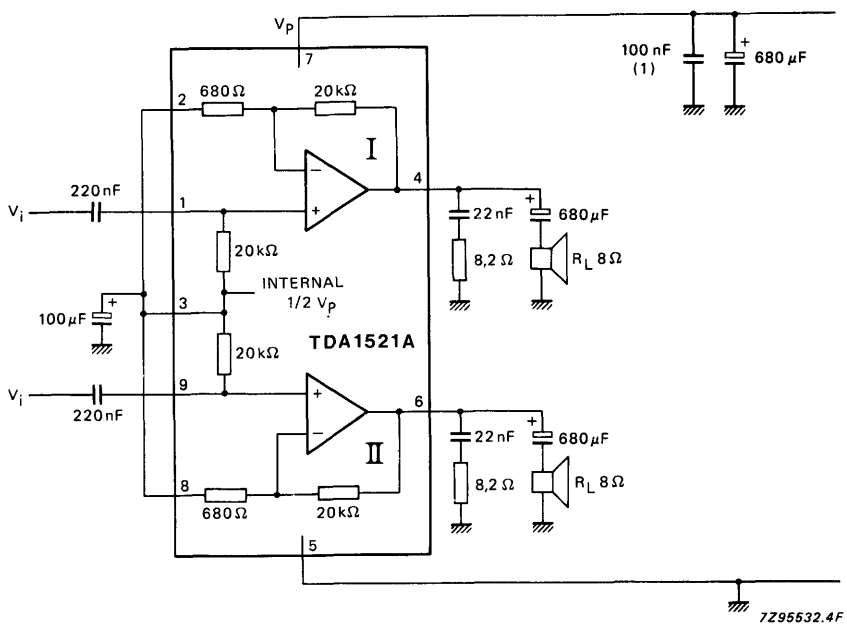
DEVELOPMENT DATA

APPLICATION INFORMATION (continued)



(1) To be connected as close as possible to the I.C.

Fig. 11 Test and application circuit; symmetrical power supply.



(1) To be connected as close as possible to the I.C.

Fig. 12 Test and application circuit; asymmetrical power supply.

STEREO CASSETTE HEAD PREAMPLIFIER AND EQUALIZER

GENERAL DESCRIPTION

The TDA1522 is a playback amplifier for car radio/cassette players.

Features

- Two independent amplifiers with open loop gain of typ. 90 dB
- Internal d.c. feedback via a 140 kΩ resistor from output to feedback point
- A.C. characteristics that can be determined externally by an RC network
- Electronic on/off switching with transient suppression for switch on
- Head input at d.c. ground that eliminates the input coupling capacitor
- Minimal external component requirement
- Stability down to a gain of 30 dB
- Low input noise
- Low distortion
- D.C. input current $< 2\ \mu A$
- Wide supply voltage range

QUICK REFERENCE DATA

Supply voltage range (pin 8)	V_P	7,5 to 23	V
Supply current (pin 8)	I_P	typ. 5	mA
Operating ambient temperature range	T_{amb}	−30 to +85	°C
Total harmonic distortion	THD	typ. 0,05	%
Channel separation at $R_S = 10\ k\Omega$; $L_S = 0$	α	min. 45	dB

PACKAGE OUTLINE

9-lead SIL; plastic (SOT142).

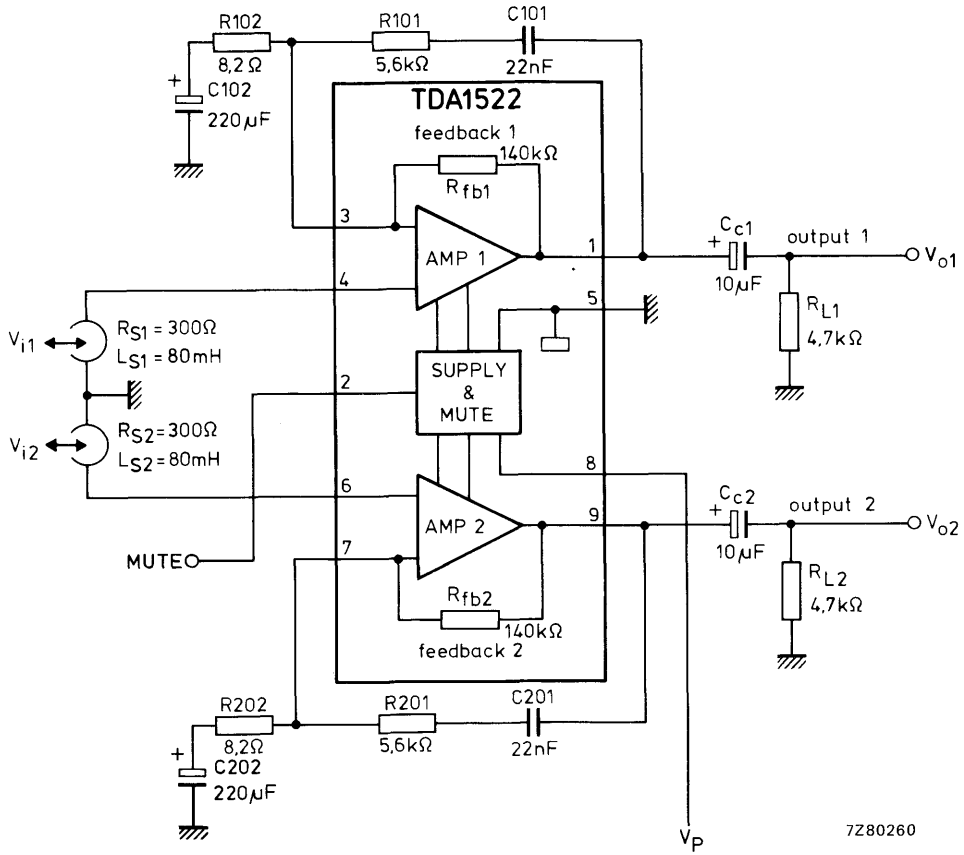


Fig. 1 Block diagram with external components; also used as test circuit.

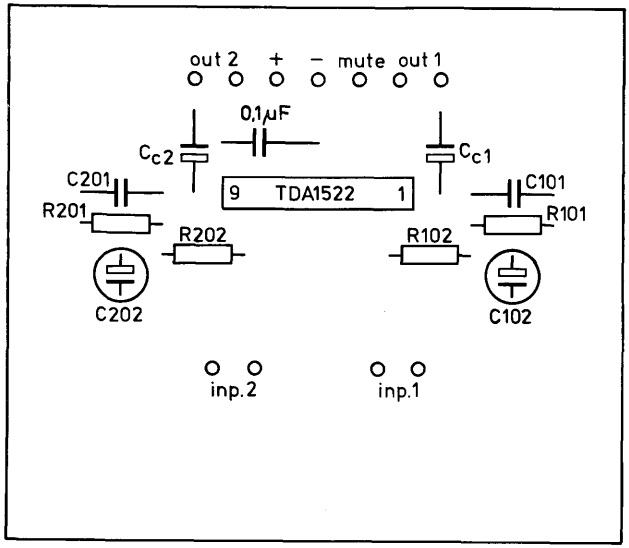


Fig. 2 Printed-circuit board component side, showing component layout for circuit of Figure 1.

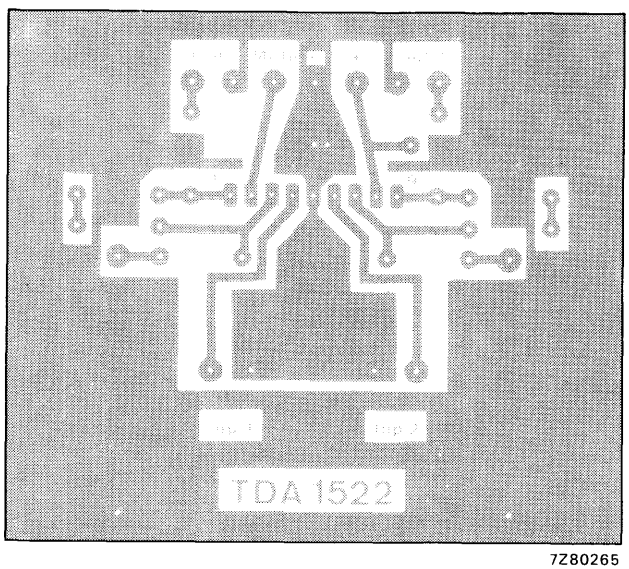


Fig. 3 Printed-circuit board, showing track side. Dimensions 75 mm x 65 mm.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_P		7,5 to 23	V
Power dissipation	P_{tot}	max.	800	mW
Feedback current (pins 3 and 7)	I_{fb}	max.	10	mA
Storage temperature range	T_{stg}		−55 to +150	°C
Operating ambient temperature range	T_{amb}		−30 to +85	°C

Note

All pins except 3 and 7 (feedback) can be connected to V_P (pin 8) or ground, (pin 5).

CHARACTERISTICS

$V_P = 8{,}5$ V; $T_{amb} = 25$ °C; test circuit Fig. 1 unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage range	V_P	7,5	–	23	V
Supply current	I_P	–	5	–	mA
Inputs (pin 4 or 6)					
Noise input voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz*	$V_{n(rms)}$	–	1,6	–	μV
Noise input voltage at $R_S = 0$; f = 1 kHz*, **	V_n	–	5	–	$nV/\sqrt{Hz}$
Noise input current at f = 1 kHz*, ▲	I_n	–	1,2	–	$pA/\sqrt{Hz}$
D.C. input current at pins 4 and 6	$-I_4; -I_6$	–	–	2	μA
Outputs (pin 1 or 9)					
Output voltage at $V_i = 0{,}3$ mV; f = 315 Hz	V_o	–	0,72	–	V
at THD = 1%; f = 1 kHz	V_o	1,0	–	–	V
Output source current at $V_{2\text{-}5} \geqslant 7{,}5$ V; mute OFF	$-I_o$	5	10	–	mA
D.C. output voltage	V_o	–	3,7	–	V
Noise output voltage (weighted) at $R_S = 300\ \Omega$; $L_S = 80$ mH					
as DIN A (r.m.s. value)	$V_{n(rms)}$	–	700	–	μV
as CCITT (peak value)	$V_{n(m)}$	–	1200	–	μV
as CCIR (peak value)	$V_{n(m)}$	–	1600	–	μV
Noise output voltage (unweighted) at $R_S = 300\ \Omega$; $L_S = 80$ mH					
as DIN 45405 (peak value)	$V_{n(m)}$	–	1800	–	μV

* Measured in Fig. 4. ** See also Fig. 6. ▲ See also Fig. 7.

parameter	symbol	min.	typ.	max.	unit
Mute on/off characteristics (pin 2)*					
Mute ON voltage at mute switch closed	V_m	0	–	1	V
Mute ON current at mute switch closed or $V_{2-5} = 0$ V	I_m	–	2,7	–	μA
Mute OFF voltage at mute switch open	V_m	7,5	–	V_P	V
Impedance					
Input impedance** at f = 1 kHz	$\|Z_i\|$	200	–	–	kΩ
Output impedance** at f = 1 kHz	$\|Z_o\|$	–	–	1	kΩ
General					
Internal feedback resistor**	R_{fb}	100	140	180	kΩ
Open-loop voltage gain** at f = 315 Hz	G_v	–	90	–	dB
Channel separation at $R_S = 10$ kΩ; $L_S = 0$; (note 1)	α	45	–	–	dB
Power supply ripple rejection at $V_{P(rms)} = 0{,}1$ V; f = 100 Hz (note 2)	RR	90	95	–	dB
Total harmonic distortion at f = 1 kHz; $V_o = 0{,}72$ V (note 3)	THD	–	0,05	–	%

Notes

1. Frequency range 300 Hz to 20 kHz.
2. Referred to the input.
3. Measured selective.

* See also Fig. 5.
** Applies to each amplifier.

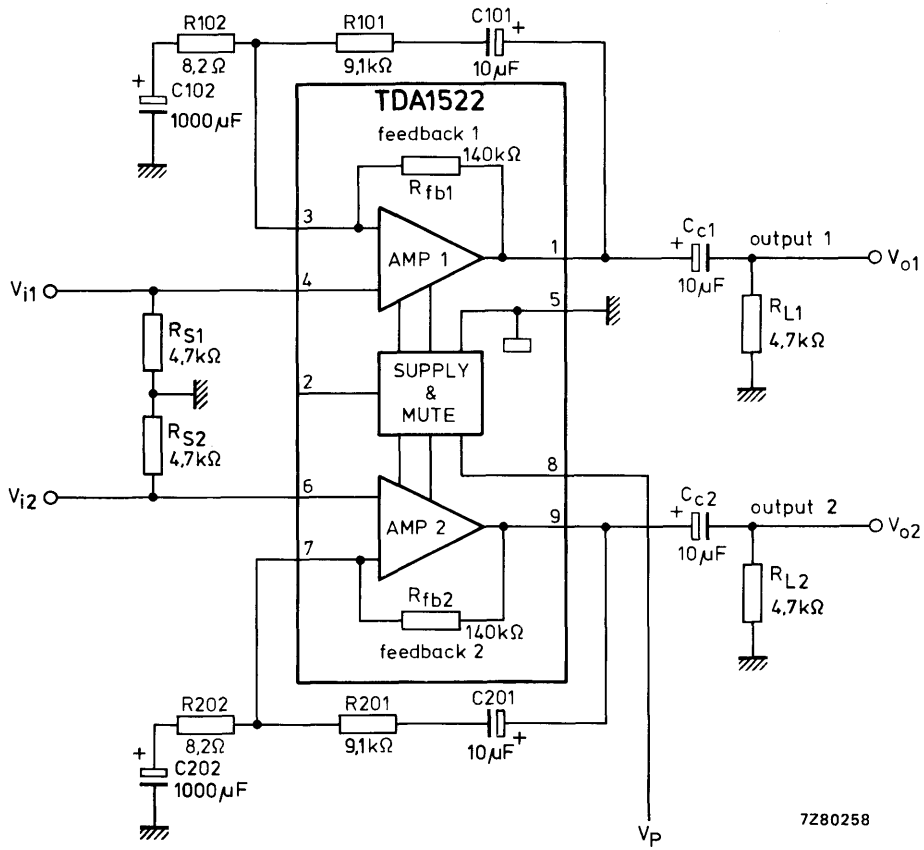


Fig. 4 Test circuit for noise measurement.

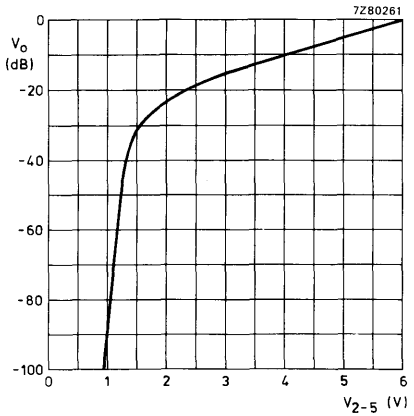


Fig. 5 Muting depth as a function of control voltage at pin 2.

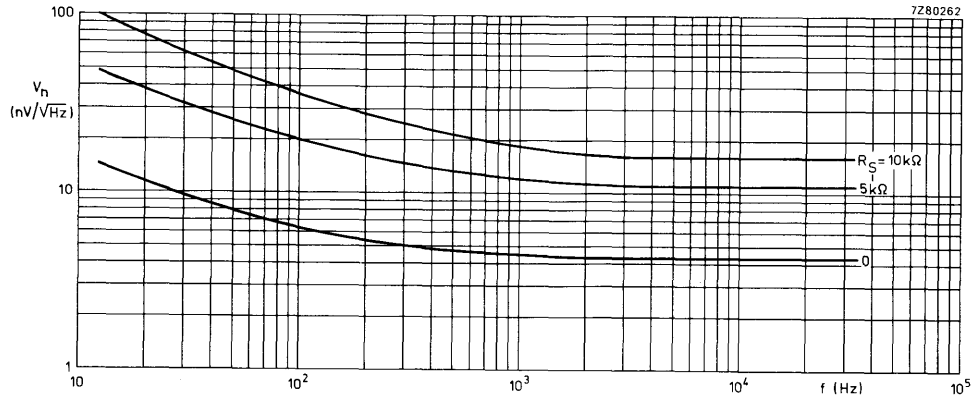


Fig. 6 Noise input voltage as a function of frequency.

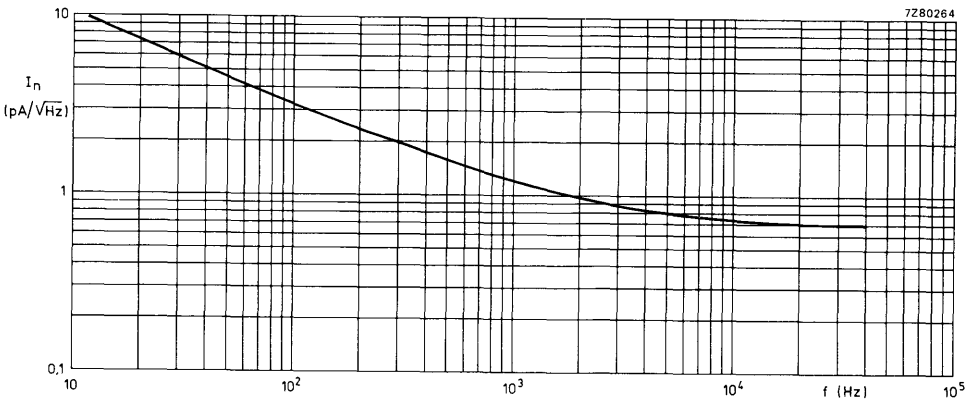


Fig. 7 Noise input current as a function of frequency.

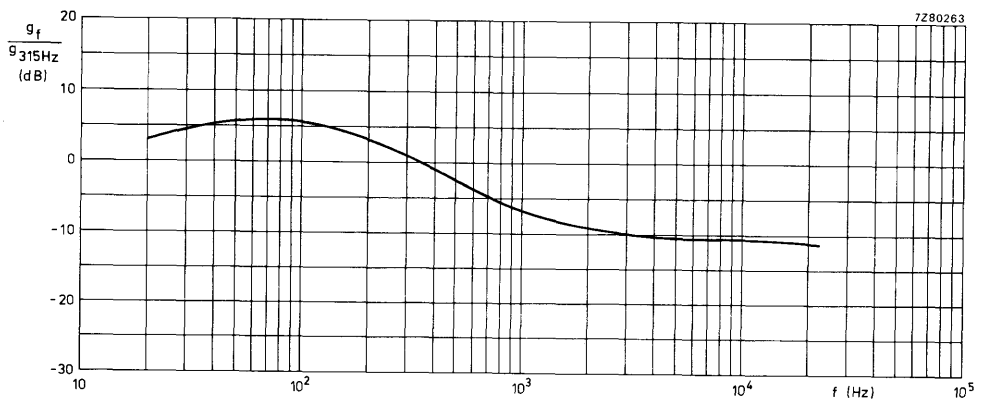


Fig. 8 Frequency response curve for the circuit in Figure 1.

APPLICATION INFORMATION

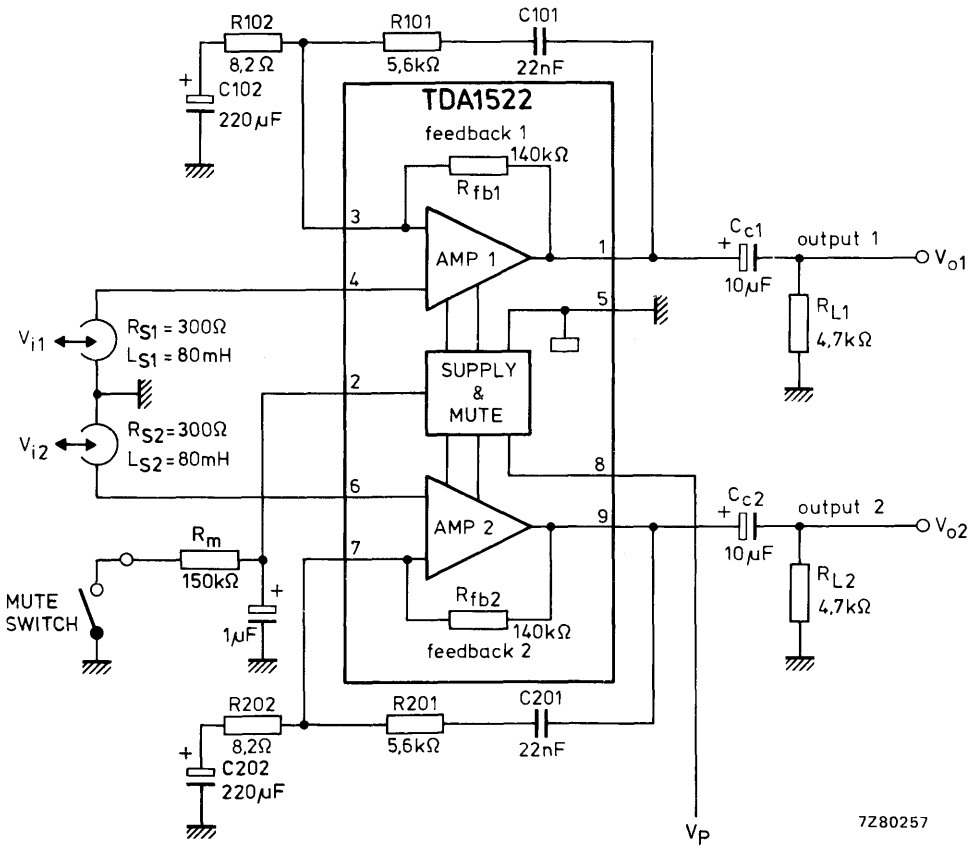


Fig. 9 Simple mute application.

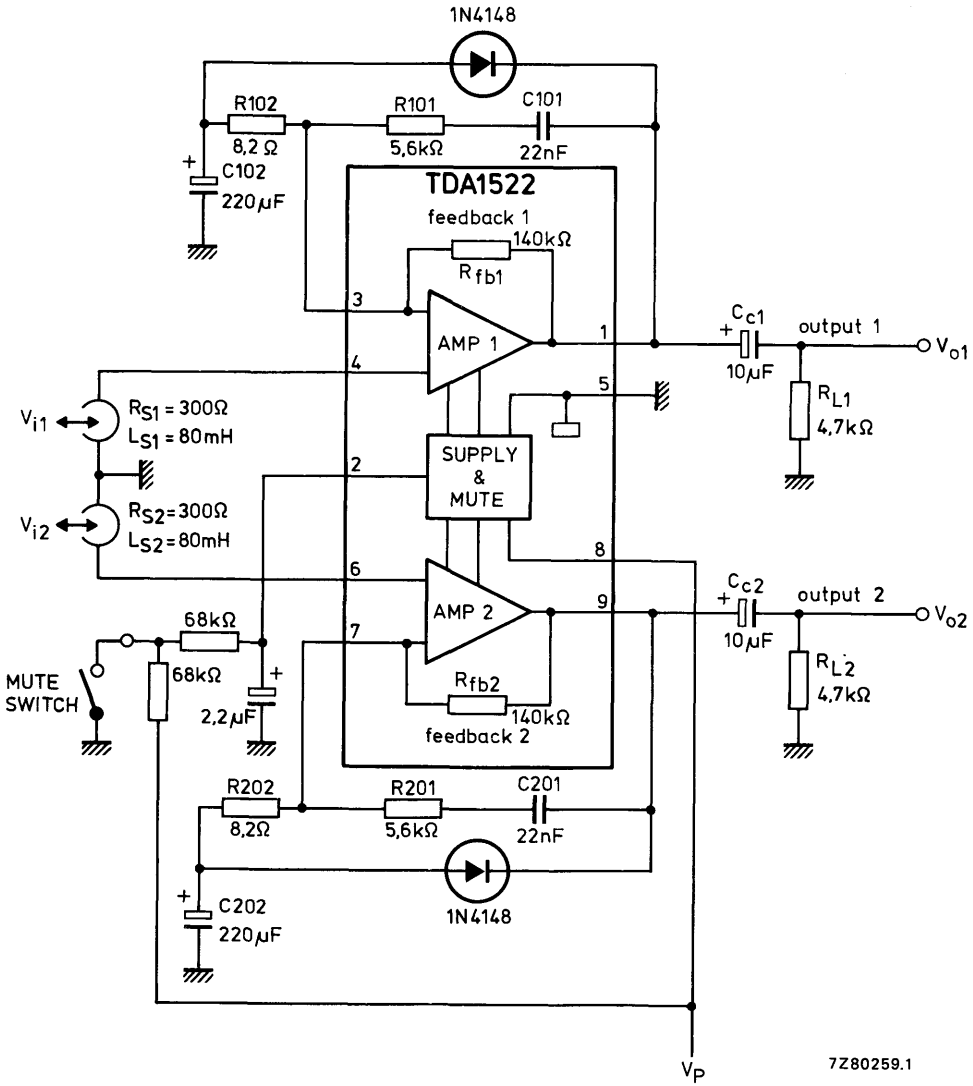


Fig. 10 Application for plop-free muting.

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

Features

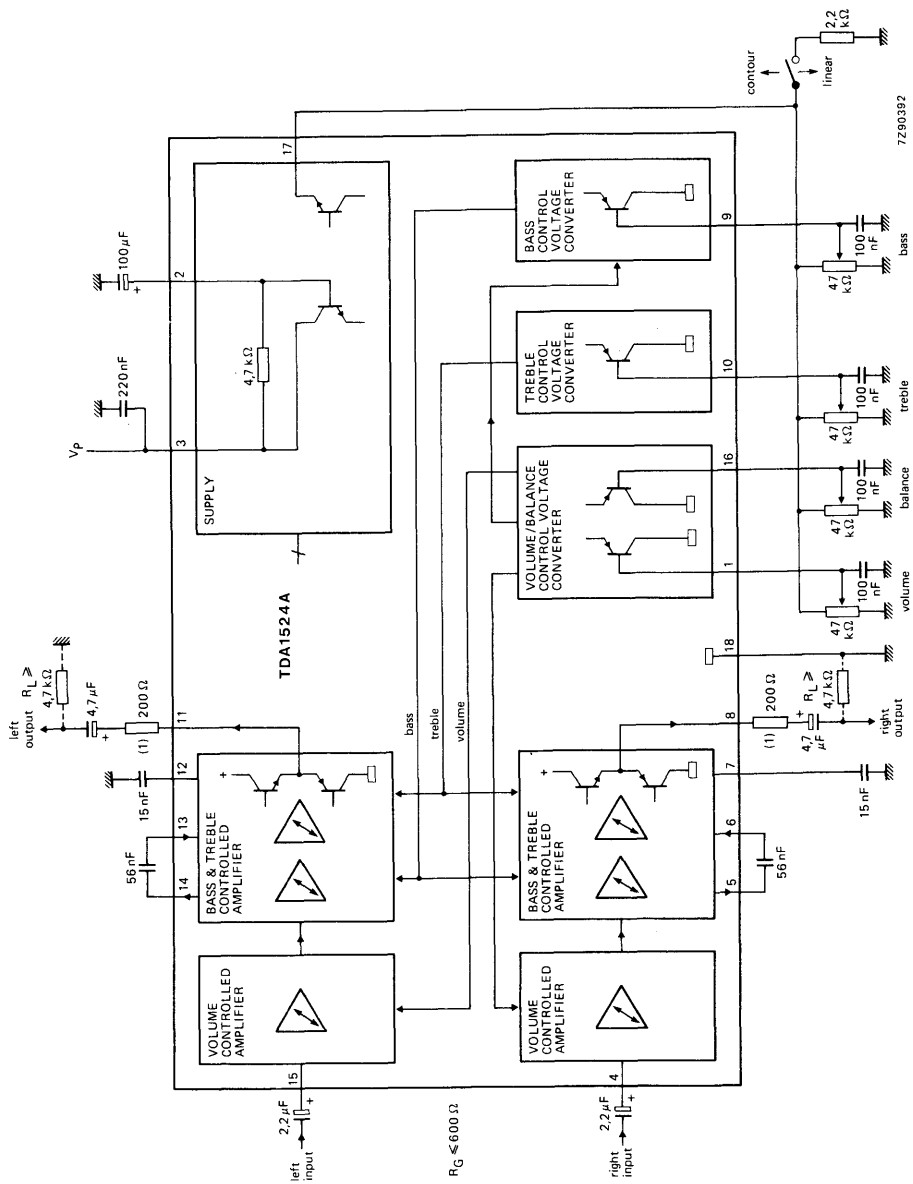
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

QUICK REFERENCE DATA

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	typ.	12 V
Supply current (pin 3)	$I_P = I_3$	typ.	35 mA
Maximum input signal with d.c. feedback (r.m.s. value)	$V_{i(rms)}$	typ.	2,5 V
Maximum output signal with d.c. feedback (r.m.s. value)	$V_{o(rms)}$	typ.	3 V
Volume control range	G_V	−80 to + 21,5	dB
Bass control range at 40 Hz	ΔG_V	−19 to + 17	dB
Treble control range at 16 kHz	ΔG_V	typ. ± 15	dB
Total harmonic distortion	THD	typ. 0,3	%
Output noise voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz; V_P = 12 V;			
for max. voltage gain	$V_{no(rms)}$	typ. 310	μV
for voltage gain G_V = −40 dB	$V_{no(rms)}$	typ. 100	μV
Channel separation at G_V = −20 to + 21,5 dB	α_{cs}	typ. 60	dB
Tracking between channels at G_V = −20 to + 26 dB	ΔG_V	max. 2,5	dB
Ripple rejection at 100 Hz	RR	typ. 50	dB
Supply voltage range (pin 3)	$V_P = V_{3\text{-}18}$	7,5 to 16,5	V
Operating ambient temperature range	T_{amb}	−30 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.

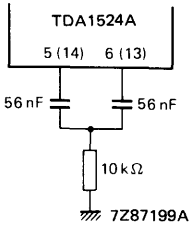


Fig. 2 Double-pole low-pass filter for improved bass-boost.

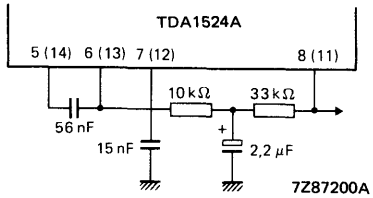


Fig. 3 D.C. feedback with filter network for improved signal handling.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	max.	20 V
Total power dissipation	P_{tot}	max.	1200 mW
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

D.C. CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7,5	–	16,5	V
Supply current					
at $V_P = 8{,}5$ V	$I_P = I_3$	19	27	35	mA
at $V_P = 12$ V	$I_P = I_3$	25	35	45	mA
at $V_P = 15$ V	$I_P = I_3$	30	43	56	mA
D.C. input levels (pins 4 and 15)					
at $V_P = 8{,}5$ V	$V_{4,15-18}$	3,8	4,25	4,7	V
at $V_P = 12$ V	$V_{4,15-18}$	5,3	5,9	6,6	V
at $V_P = 15$ V	$V_{4,15-18}$	6,5	7,3	8,2	V
D.C. output levels (pins 8 and 11) under all control voltage conditions with d.c. feedback (Fig. 3)					
at $V_P = 8{,}5$ V	$V_{8,11-18}$	3,3	4,25	5,2	V
at $V_P = 12$ V	$V_{8,11-18}$	4,6	6,0	7,4	V
at $V_P = 15$ V	$V_{8,11-18}$	5,7	7,5	9,3	V
Pin 17					
Internal potentiometer supply voltage at $V_P = 8{,}5$ V	V_{17-18}	3,5	3,75	4,0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0,5	mA
linear (switch closed)	$-I_{17}$	1,5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10{,}8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4,5	–	$V_P/2 - V_{BE}$	V
D.C. control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at $V_{17-18} = 5$ V	$V_{1,9,10,16}$	1,0	–	4,25	V
using internal supply	$V_{1,9,10,16}$	0,25	–	3,8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

A.C. CHARACTERISTICS

$V_P = V_{3-18} = 8{,}5$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Max. gain of volume (Fig. 5)	$G_{V\,max}$	20,5	21,5	23	dB
Volume control range; $G_{V\,max}/G_{V\,min}$	ΔG_V	90	100	–	dB
Balance control range; $G_V = 0$ dB (Fig. 6)	ΔG_V	–	−40	–	dB
Bass control range at 40 Hz (Fig. 7)	ΔG_V	–	−19 to + 17 ± 3		dB
Treble control range at 16 kHz (Fig. 8)	ΔG_V	–	± 15 ± 3	–	dB
Contour characteristics		see Figs 9 and 10			
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1) at gain of volume control: $G_V = 20$ dB	$R_{i4,15}$	10	–	–	kΩ
$G_V = -40$ dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; $G_V = 0$ dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz) at $G_V = -20$ to + 21,5 dB	α_{cs}	46	60	–	dB
Spread of volume control with constant control voltage $V_{1-18} = 0{,}5\ V_{17-18}$	ΔG_V	–	–	± 3	dB
Gain tolerance between left and right channel $V_{16-18} = V_{1-18} = 0{,}5\ V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1,5	dB
Tracking between channels for $G_V = 21{,}5$ to −26 dB f = 250 Hz to 6,3 kHz; balance adjusted at $G_V = 10$ dB	ΔG_V	–	–	2,5	dB

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with d.c. feedback (Fig. 3)					
Input signal handling					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 8,5 V; THD = 0,7%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,8	2,4	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 12 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 15 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
Output signal handling (note 2 and note 3)					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	1,8	2,0	–	V
at V_P = 8,5 V; THD = 10%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	–	2,2	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	2,5	3,0	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	–	3,5	–	V
Noise performance (V_P = 8,5 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	260	–	μV
for G_V = −3 dB (note 4)	$V_{no(rms)}$	–	70	140	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	890	–	μV
for maximum emphasis of bass and treble (contour off; G_V = −40 dB)	$V_{no(m)}$	–	360	–	μV
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	310	–	μV
for G_V = −16 dB (note 4)	$V_{no(rms)}$	–	100	200	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	940	–	μV
for maximum emphasis of bass and treble (contour off; G_V = −40 dB)	$V_{no(m)}$	–	400	–	μV

parameter	symbol	min.	typ.	max.	unit
Noise performance (V_P = 15 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	350	–	μV
for G_V = 16 dB (note 4)	$V_{no(rms)}$	–	110	220	μV
Output noise voltage; weighted as DIN 45405					
of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	980	–	μV
for maximum emphasis of bass and treble					
(contour off; G_V = −40 dB)	$V_{no(m)}$	–	420	–	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 4)

$$R_i = \frac{160\ k\Omega}{1 + G_V}\ ;\ G_{V\ max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. Linear frequency response.
5. For peak values add 4,5 dB to r.m.s. values.

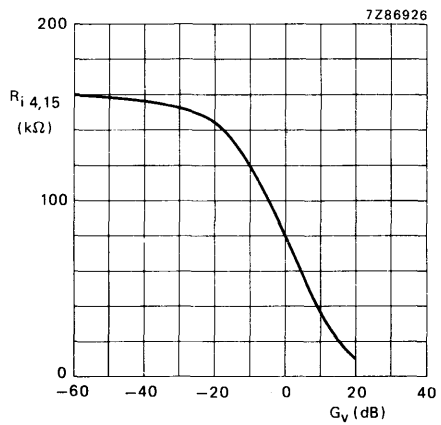


Fig. 4 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig. 1.

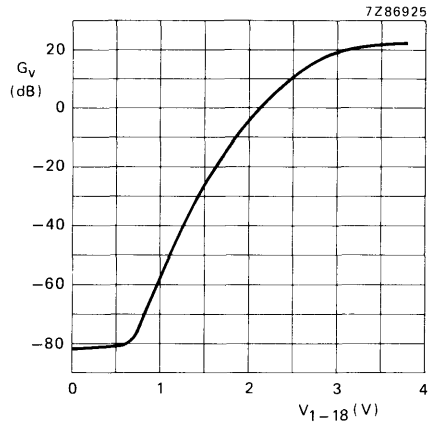


Fig. 5 Volume control curve; voltage gain (G_v) as a function of control voltage (V_{1-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 1 kHz.

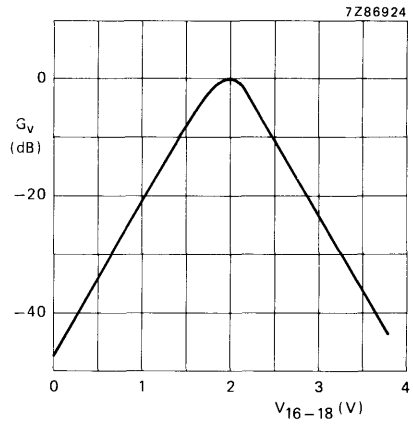


Fig. 6 Balance control curve; voltage gain (G_v) as a function of control voltage (V_{16-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V.

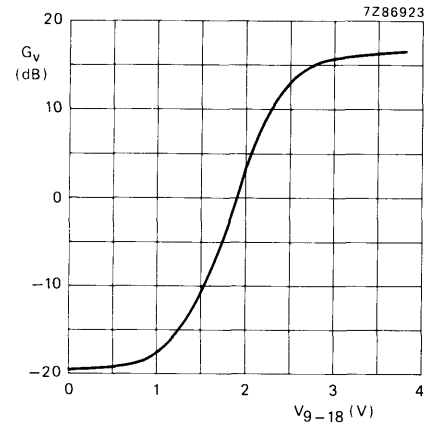


Fig. 7 Bass control curve; voltage gain (G_v) as a function of control voltage (V_{9-18}). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 40 Hz.

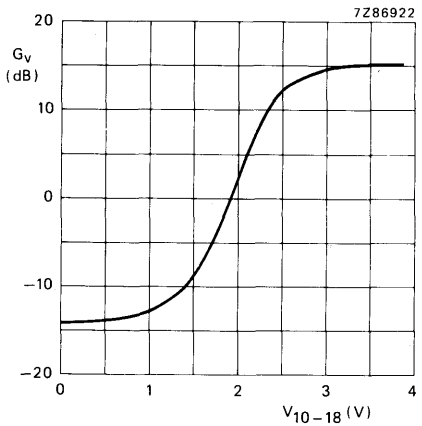


Fig. 8 Treble control curve; voltage gain (G_v) as a function of control voltage (V_{10-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 16 kHz.

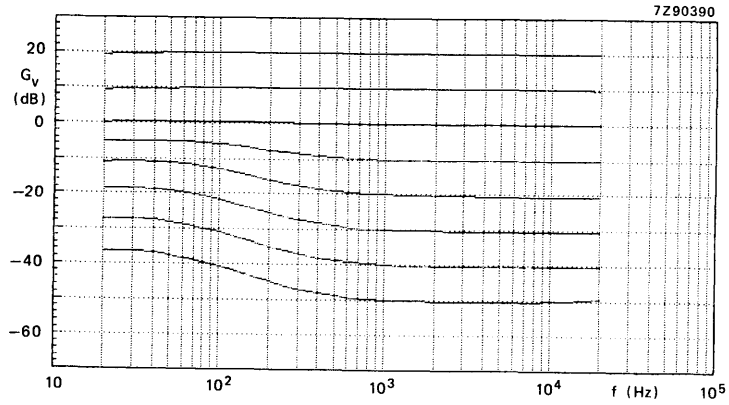


Fig. 9 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

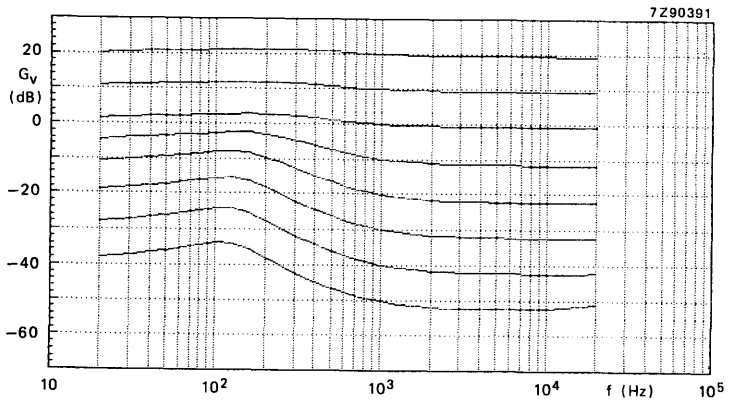


Fig. 10 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

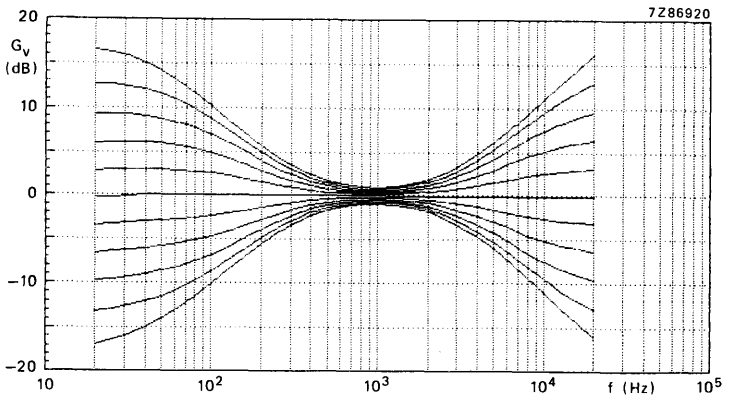


Fig. 11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

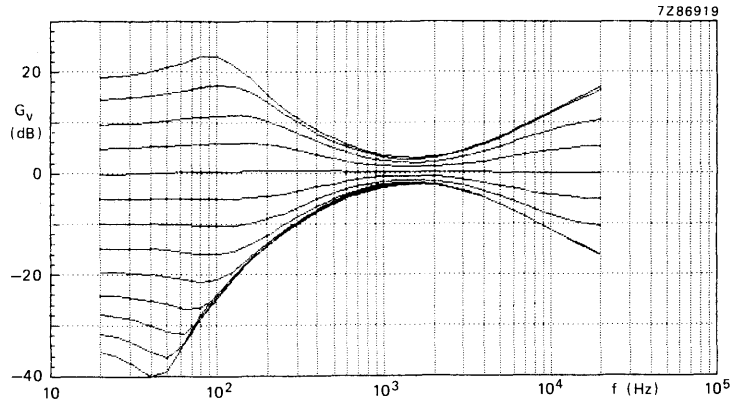


Fig. 12 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

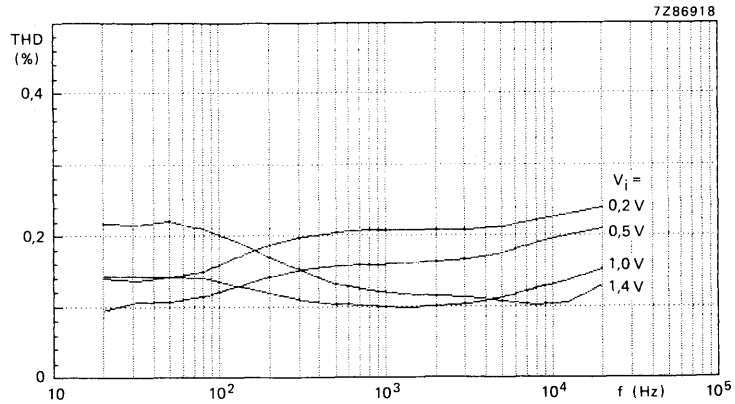


Fig. 13 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig. 1; V_P = 8,5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

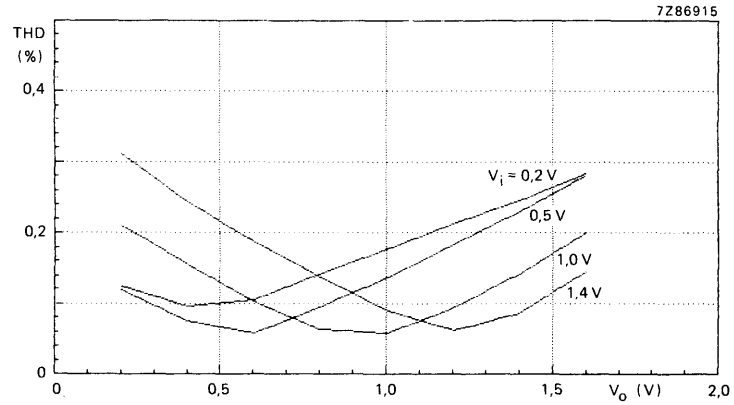
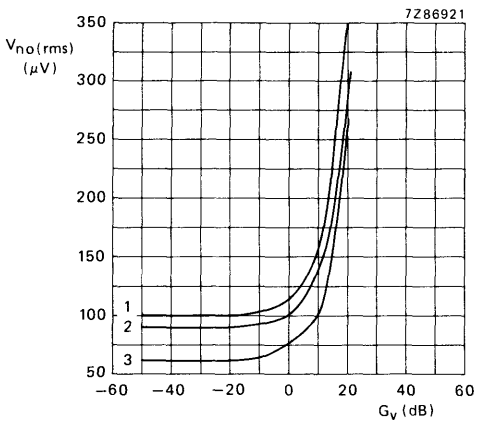


Fig. 14 Total harmonic distortion (THD); as a function of output voltage (V_O). Measured in Fig. 1; V_P = 8,5 V; f_i = 1 kHz.



(1) V_P = 15 V.
(2) V_P = 12 V.
(3) V_P = 8,5 V.

Fig. 15 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_V). Measured in Fig. 1; f = 20 Hz to 20 kHz.

STEREO TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The TDA1525 is an active stereo tone/volume control for car radios, television receivers and mains-fed audio equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by DC voltages or by single linear potentiometers.

Features

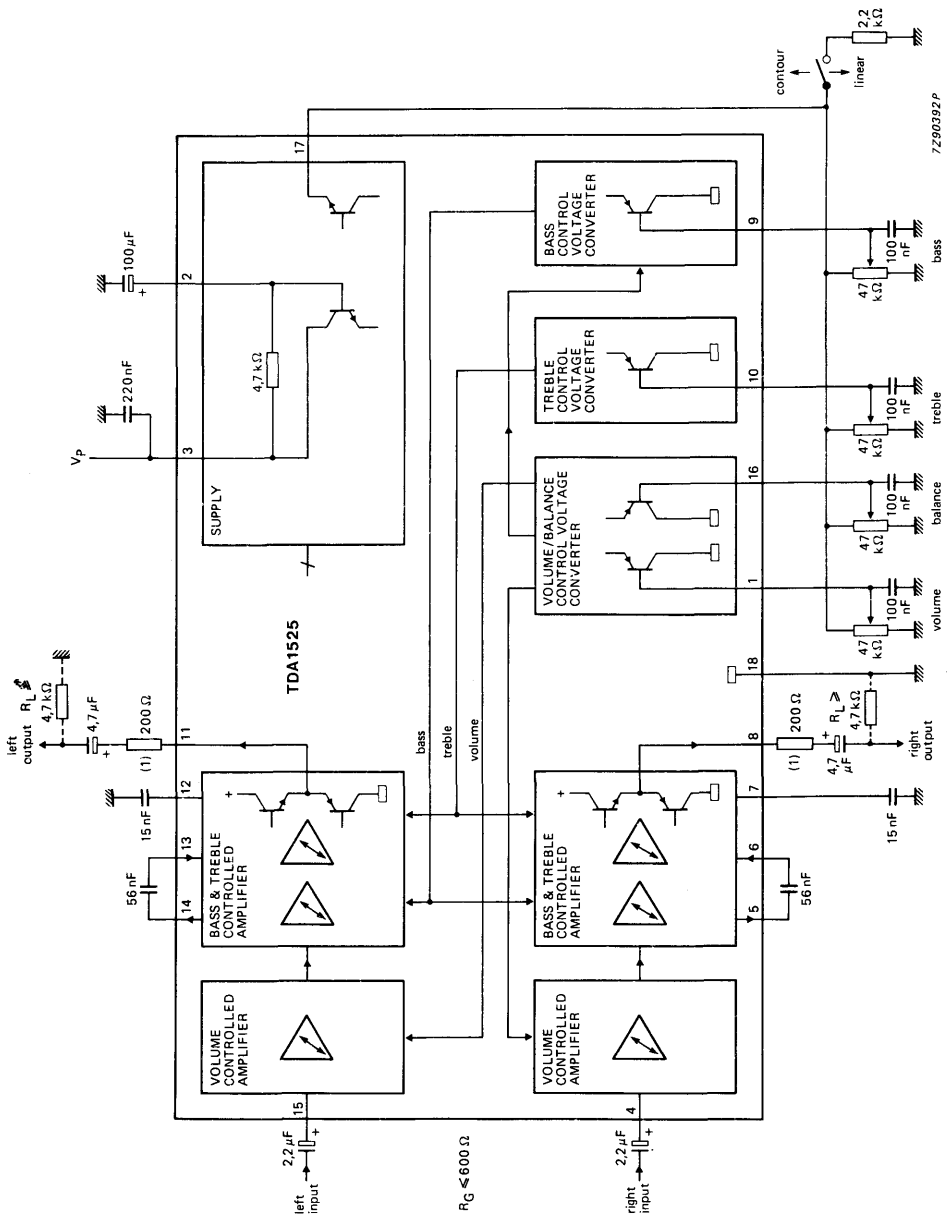
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		$V_P = V_{3-18}$	7.5	12	16.5	V
Supply current		I_3	–	35	–	mA
Maximum input signal with DC feedback (RMS value)		$V_{i(rms)}$	–	2.5	–	V
Maximum output signal with DC feedback (RMS value)		$V_{o(rms)}$	–	3.0	–	V
Volume control range		ΔG_v	–80	–	+ 21.5	dB
Bass control range	at 40 Hz	ΔG_v	–	– 19 to + 17	–	dB
Treble control range	at 16 kHz	ΔG_v	–	± 15	–	dB
Total harmonic distortion		THD	–	0.3	–	%
Output noise voltage (RMS value)	unweighted; f = 20 Hz to 20 kHz; V_P = 12 V					
for maximum voltage gain		$V_{no(rms)}$	–	310	–	μV
for voltage gain = –40 dB		$V_{no(rms)}$	–	100	–	μV
Channel separation	G_v = –20 to + 21.5 dB	α_{cs}	–	60	–	dB
Tracking between channels	G_v = –20 to + 26 dB	ΔG_v	–	–	2.5	dB
Ripple rejection	f = 100 Hz	RR	–	50	–	dB
Operating ambient temperature range		T_{amb}	–40	–	+ 85	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.

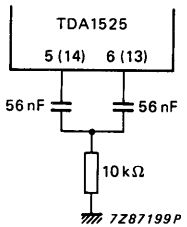


Fig.2 Double-pole low-pass filter for improved bass-boost.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 3)		$V_P = V_{3-18}$	–	18	V
Total power dissipation		P_{tot}	–	1200	mW
Storage temperature range		T_{stg}	−55	+ 150	°C
Operating ambient temperature range		T_{amb}	−40	+ 85	°C

DEVELOPMENT DATA

DC CHARACTERISTICS

$V_P = V_{3\text{-}18} = 12$ V; $T_{amb} = 25$ °C; all voltages are with reference to pin 18; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L > 4.7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_P = V_3$	7.5	12	16.5	V
Supply current	V_P = 8.5 V	I_3	19	27	35	mA
	V_P = 9.7 V	I_3	–	–	40	mA
	V_P = 12.0 V	I_3	25	35	45	mA
	V_P = 15.0 V	I_3	30	43	56	mA
DC input levels (pins 4 and 15)	V_P = 8.5 V	$V_{4,15}$	3.8	4.25	4.7	V
	V_P = 12.0 V	$V_{4,15}$	5.3	5.9	6.6	V
	V_P = 15.0 V	$V_{4,15}$	6.5	7.3	8.2	V
DC output levels (pins 8 and 11)	all control voltage conditions					
	V_P = 8.5 V	$V_{8,11}$	3.3	4.25	5.2	V
	V_P = 12.0 V	$V_{8,11}$	4.6	6.0	7.4	V
	V_P = 15.0 V	$V_{8,11}$	5.7	7.5	9.3	V
Potentiometer supply voltage output (pin 17)	V_P = 8.5 V	V_{17}	3.25	3.6	3.85	V
Contour on/off switch (control by I_{17})						
contour	switch open	$-I_{17}$	–	–	0.5	mA
linear	switch closed	$-I_{17}$	1.5	–	10.0	mA
Application without potentiometer supply from pin 17 (contour cannot be switched off); voltage range forced to pin 17	$V_P \geqslant 10.8$ V	V_{17}	4.5	–	$\frac{V_P}{2} - V_{BE}$	V
DC voltage range for volume, bass, treble and balance controls (pins 1, 9, 10 and 16 respectively)	V_{17} = 5.0 V	$V_{1,9,10,16}$	1.0	–	4.25	V
	using supply from pin 17	$V_{1,9,10,16}$	0.25	–	3.8	V
Input current to pins 1, 9, 10 and 16		$-I_{1,9,10,16}$	–	–	5.0	μA

DEVELOPMENT DATA

AC CHARACTERISTICS

$V_P = V_{3-18} = 8.5$ V; $T_{amb} = 25$ °C; all voltages are with reference to pin 18; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Control range						
Max. gain (volume)	see Fig. 4	$G_{v\,max}$	20.5	21.5	23.0	dB
Volume control range	$G_{v\,max}/G_{v\,min}$	ΔG_v	90	100	–	dB
Balance control range	G_v = 0 dB; see Fig. 5	ΔG_v	–	–40	–	dB
Bass control range	f = 40 Hz; see Fig. 6	ΔG_v	± 12	–19 to +17	–	dB
Treble control range	f = 16 kHz; see Fig. 7	ΔG_v	± 12	± 15	–	dB
Contour characteristics			see Figs 8 and 9			
Input signals (pins 4 and 15)						
Input resistance with volume control gain	note 1					
at 20 dB	G_v = 20 dB	$R_{i4,\,15}$	10	–	–	kΩ
at –40 dB	G_v = –40 dB	$R_{i4,\,15}$	–	160	–	kΩ
Output signals (pins 8 and 11)						
Output resistance		$R_{o8,\,11}$	–	–	300	Ω
Signal processing						
Power supply ripple rejection	$V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; G_v = 0 dB	RR	35	50	–	dB
Channel separation	250 Hz to 10 kHz; G_v = –20 to + 21.5 dB	α_{cs}	46	60	–	dB
Spread of volume control with constant control voltage	$V_1 = V_{17}/2$	ΔG_v	–	–	± 3	dB
Gain tolerance between left and right channels	$V_1 = V_{16} = V_{17}/2$	$\Delta G_{vL\text{-}R}$	–	–	1.5	dB
Tracking between channels	G_v = 21.5 to –26 dB; f = 250 Hz to 6.3 kHz; balance adjusted for G_v = 10 dB	ΔG_v	–	–	2.5	dB

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Signal handling						
Input signal handling (RMS value)	V_P = 8.5 V; THD = 0.5%; f = 1 kHz	$V_{i(rms)}$	1.4	–	–	V
	V_P = 8.5 V; THD = 0.7%; f = 1 kHz	$V_{i(rms)}$	1.8	2.4	–	V
	V_P = 12 V; THD = 0.5%; f = 40 Hz to 16 kHz	$V_{i(rms)}$	1.4	–	–	V
	V_P = 12 V; THD = 0.7%; f = 40 Hz to 16 kHz	$V_{i(rms)}$	2.0	3.2	–	V
	V_P = 15 V; THD = 0.5%; f = 40 Hz to 16 kHz	$V_{i(rms)}$	1.4	–	–	V
	V_P = 15 V; THD = 0.7%; f = 40 Hz to 16 kHz	$V_{i(rms)}$	2.0	3.2	–	V
Output signal handling (RMS value)	notes 2 and 3; V_P = 8.5 V; THD = 0.5%; f = 1 kHz	$V_{o(rms)}$	1.8	2.0	–	V
	V_P = 8.5 V; THD = 10%; f = 1 kHz	$V_{o(rms)}$	–	2.2	–	V
	V_P = 12 V; THD = 0.5%; f = 40 Hz to 16 kHz	$V_{o(rms)}$	2.5	3.0	–	V
	V_P = 15 V; THD = 0.5%; f = 40 Hz to 16 kHz	$V_{o(rms)}$	–	3.5	–	V

parameter	conditions	symbol	min.	typ.	max.	unit
Noise performance (V_P = 8.5 V)						
Output noise voltage; unweighted (RMS value)	see Fig. 14; f = 20 Hz to 20 kHz					
for max. voltage gain	note 4	$V_{no(rms)}$	–	260	–	μV
for G_V = −3 dB	note 4	$V_{no(rms)}$	–	70	140	μV
Output noise voltage; weighted as DIN45405 of 1981, CCIR recommendation 468-2 (peak value)						
for max. voltage gain for max. emphasis of bass and treble	note 4	$V_{no(m)}$	–	890	–	μV
	contour off; G_V = −40 dB	$V_{no(m)}$	–	360	–	μV
Noise performance (V_P = 12 V)						
Output noise voltage; unweighted (RMS value)	see Fig. 14; f = 20 Hz to 20 kHz; note 5					
for max. voltage gain	note 4	$V_{no(rms)}$	–	310	–	μV
for G_V = −16 dB	note 4	$V_{no(rms)}$	–	100	200	μV
Output noise voltage; weighted as DIN45405 of 1981, CCIR recommendation 468-2 (peak value)						
for max. voltage gain for max. emphasis of bass and treble	note 4	$V_{no(m)}$	–	940	–	μV
	contour off; G_V = −40 dB	$V_{no(m)}$	–	400	–	μV

DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Noise performance (V_P = 15 V)						
Output noise voltage; unweighted (RMS value)	see Fig. 14; f = 20 Hz to 20 kHz; note 5					
for max. voltage gain	note 4	$V_{no(rms)}$	–	350	–	μV
for G_v = −16 dB	note 4	$V_{no(rms)}$	–	110	220	μV
Output noise voltage; weighted as DIN45405 of 1981, CCIR recommendation 468-2 (peak value)						
for max. voltage gain for max. emphasis of bass and treble	note 4	$V_{no(m)}$	–	980	–	μV
	contour off; G_v = −40 dB	$V_{no(m)}$	–	420	–	μV

Notes to the characteristics

1. Equation for input resistance (see also Fig. 3)

$$R_i = \frac{160\ k\Omega}{1 + G_v};\ G_{v\,max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. Linear frequency response.
5. For peak values add 4.5 dB to RMS values.

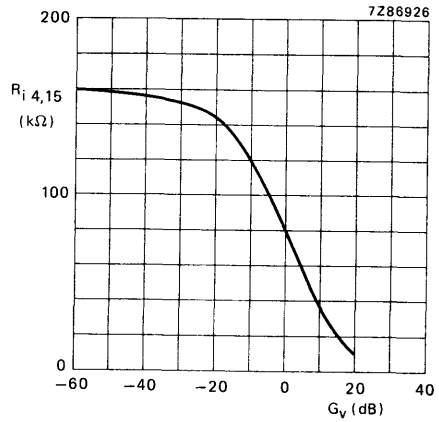


Fig. 3 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig. 1.

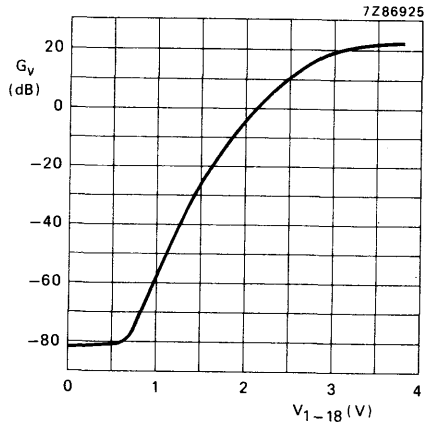


Fig. 4 Volume control curve; voltage gain (G_V) as a function of control voltage (V_{1-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 1 kHz.

DEVELOPMENT DATA

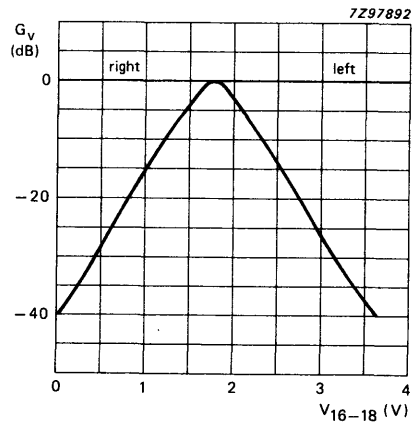


Fig. 5 Balance control curve; voltage gain (G_V) as a function of control voltage (V_{16-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V.

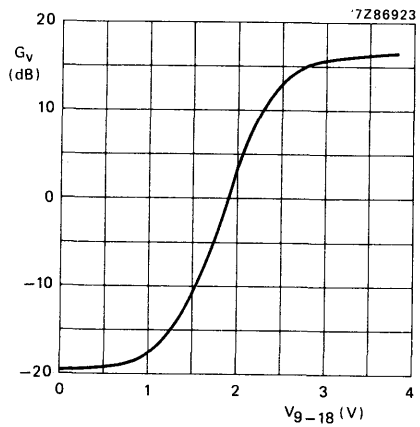


Fig. 6 Bass control curve; voltage gain (G_V) as a function of control voltage (V_{9-18}). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 40 Hz.

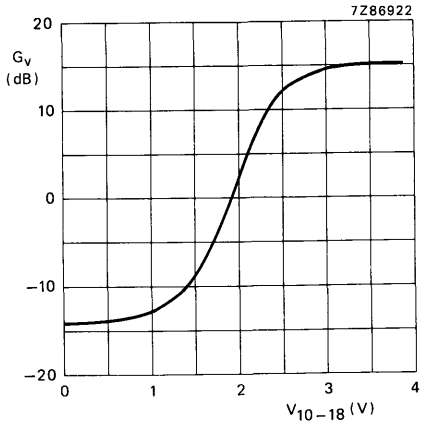


Fig. 7 Treble control curve; voltage gain (G_v) as a function of control voltage (V_{10-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 16 kHz.

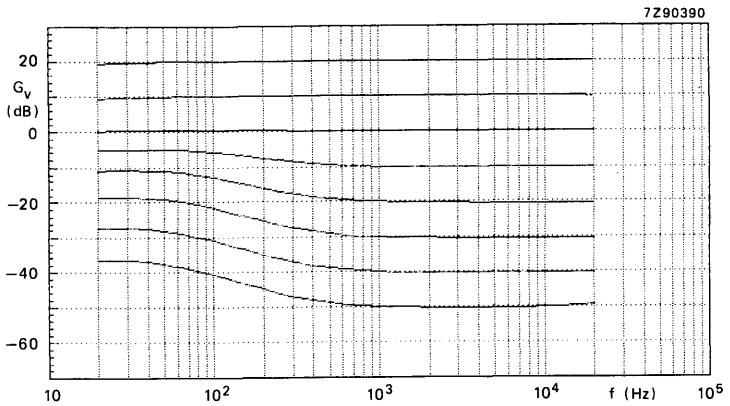


Fig. 8 Contour frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8.5 V.

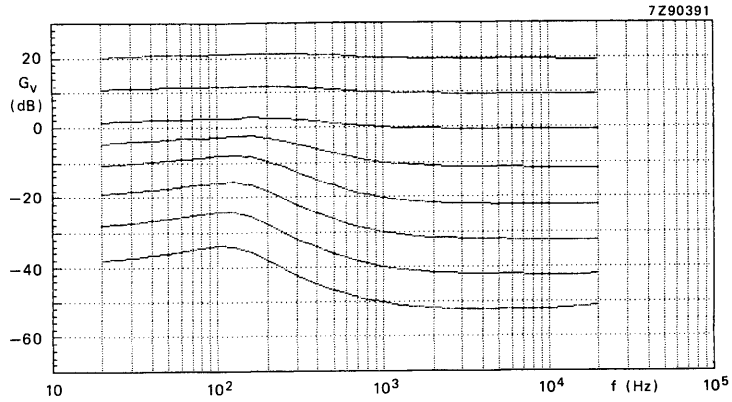


Fig. 9 Contour frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8.5 V.

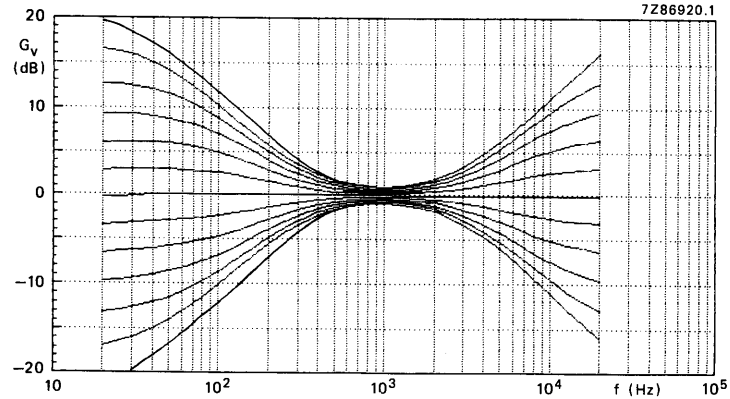


Fig. 10 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8.5 V.

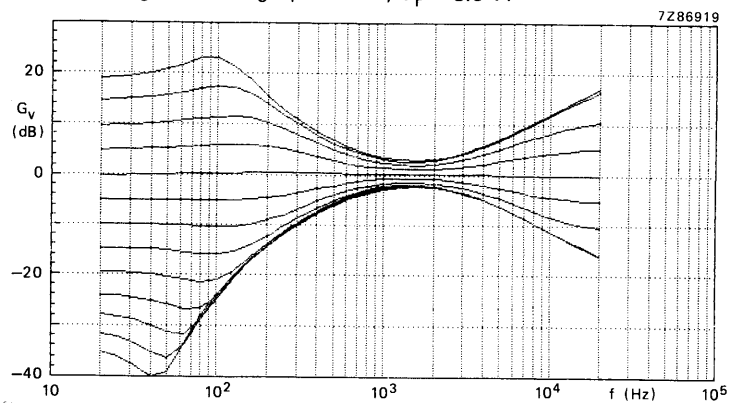


Fig. 11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8.5 V.

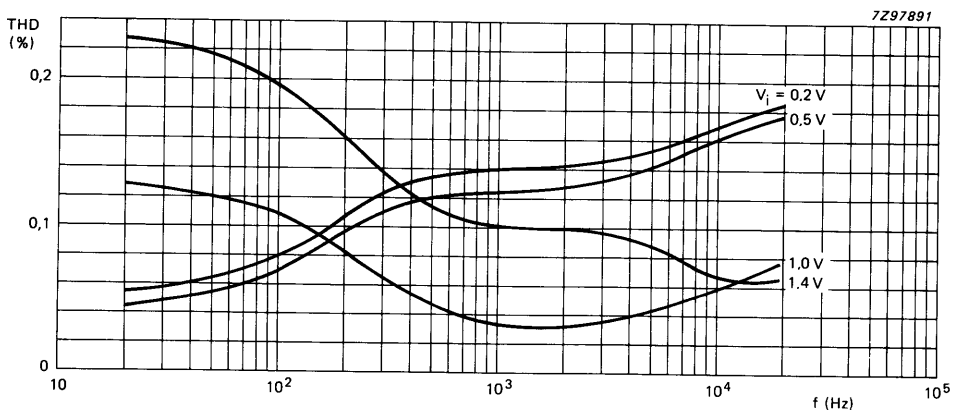


Fig. 12 Total harmonic distortion (THD) as a function of audio input frequency. Measured in Fig. 1; V_P = 8.5 V; volume control voltage gain at $G_V = 20 \log \frac{V_o}{V_i} = 0$ dB.

DEVELOPMENT DATA

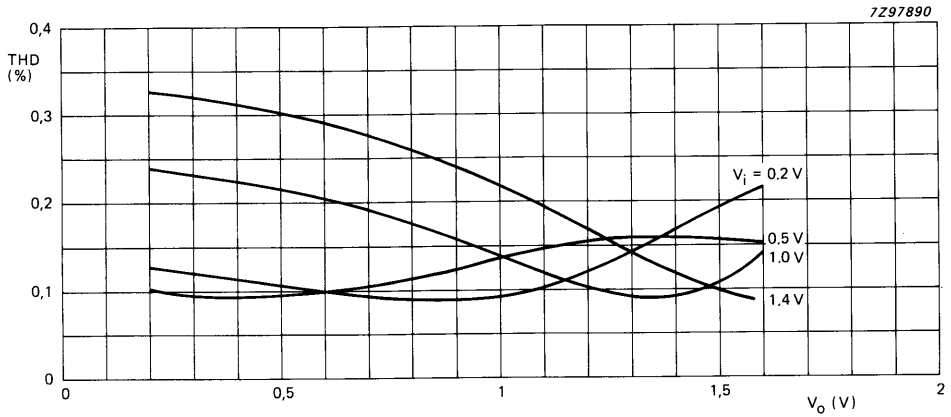
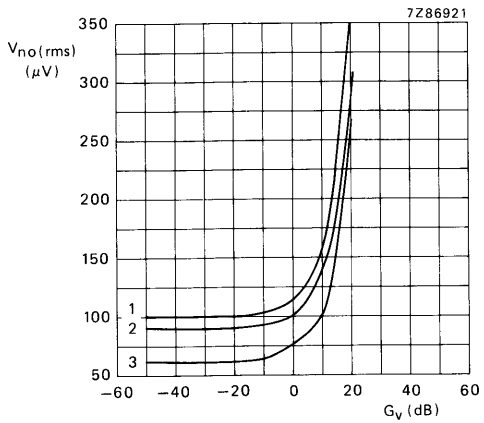


Fig. 13 Total harmonic distortion (THD) as a function of output voltage (V_O). Measured in Fig. 1; V_P = 8.5 V; f = 1 kHz.



(1) V_P = 15 V.
(2) V_P = 12 V.
(3) V_P = 8.5 V.

Fig. 14 Noise output voltage ($V_{no(rms)}$; unweighted) as a function of voltage gain (G_V). Measured in Fig. 1; f = 20 Hz to 20 kHz.

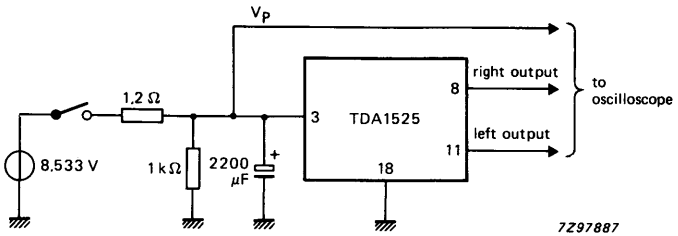


Fig. 15 Test circuit for power-on and power-off response measurements.

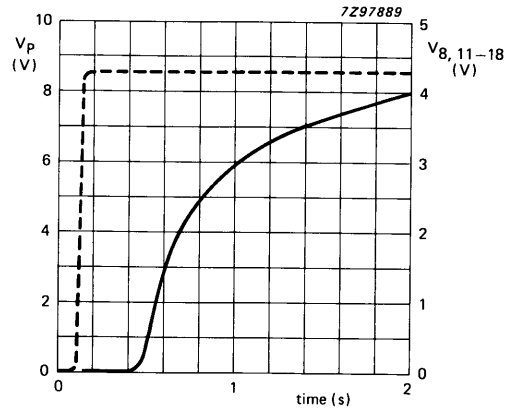


Fig. 16 Response at power-on. Measured in circuit of Fig. 15.

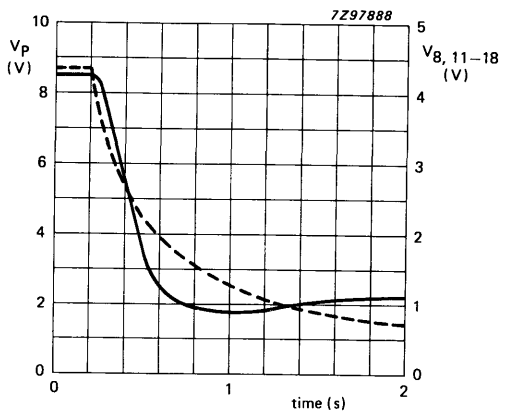


Fig. 17 Response at power-off. Measured in circuit of Fig. 15.

14-BIT ANALOGUE TO DIGITAL CONVERTER (ADC)

An integrated 14-bit analogue to digital converter (ADC) which uses the successive approximation conversion technique and includes the comparator, reference source and clock on the same chip.
The high linearity makes it very suitable for signal processing while the accurate, temperature-compensated reference source makes it applicable for instrumentation purposes.
The ADC accepts unipolar or bipolar input signals.
Digital output data is in serial form.
All digital outputs are fully TTL compatible.

QUICK REFERENCE DATA

Positive supply voltage (pin 5)	V_P	typ.	5 V
Negative supplu voltage 1 (pin 6)	$-V_{N1}$	typ.	5 V
Negative supply voltage 2 (pin 9)	$-V_{N2}$	typ.	17 V
Signal-to-noise ratio	S/N	typ.	84 dB
Linearity error		typ.	± ½ LSB
Total power dissipation	P_{tot}	typ.	500 mW
Operating ambient temperature range	T_{amb}	−20 to	+ 70 °C
Storage temperature range	T_{stg}	−55 to	+ 150 °C
Resolution			14 bits
Full scale input current	I_{FS}	typ.	4 mA

PACKAGE OUTLINE

28-lead dual in-line; plastic (with internal heat spreader) (SOT117).

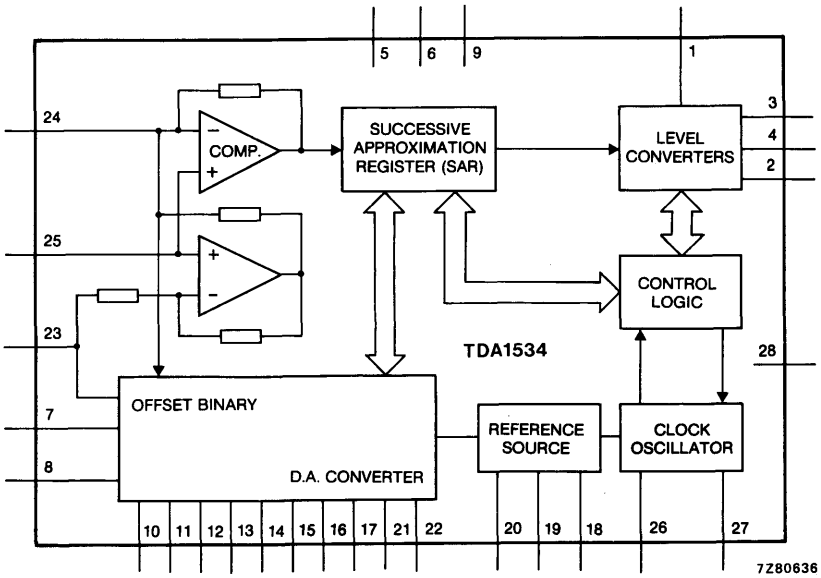


Fig. 1 Block diagram.

PIN DESIGNATION

1	start conversion
2	status out
3	data out
4	data strobe
5	positive supply voltage
6	negative supply voltage 1
7	oscillator input
8	oscillator input
9	negative supply voltage 2
10	decoupling binary weighted current sources
11	
12	
13	
14	
15	decoupling binary weighted current sources
16	
17	
18	I_{ref1}
19	I_{ref2}
20	I_{ref3}
21	decoupling binary weighted current sources
22	
23	offset binary input
24	analogue signal input
25	analogue ground
26	oscillator
27	oscillator
28	digital ground

FUNCTIONAL DESCRIPTION

The circuit consists of the following parts:

14-bit D/A converter

Using "dynamic element matching", which results in high accuracy, linearity and longterm stability, without the need of trimming. The main parts of the DAC are the binary wieghted current sources and the bit switches. The DAC also delivers an offset binary current for bipolar operation of the ADC.

Fast settling comparator/substractor

Consisting of a high speed, clamped operational amplifier with special frequency compensation system.

Successive approximation register (SAR)

This register is an array of fourteen addressable latches, with the outputs connected to the bit switches of the D/A converter.

Logic-level converters

Converting the internally used current-mode-logic (CML) levels to TTL levels, for easy interface of the ADC with standard logic families.

Clock oscillator and control logic

Delivering the pulses and timing for the SAR and takes care of the communication with the peripheral circuits.

Reference source

Based on the bandgap voltage of silicon, with extra temperature compensation circuit.

For the timing of the output signals see Fig. 3. At the leading edge of the start conversion (SC) pulse the ADC starts converting the input voltage. During the conversion cycle the following signals appear at the output pins:

Status (pin 2)

This signal can be used to force the Sample-Hold-Circuit, in front of the ADC, in hold mode.

Data strobe (pin 4)

This signal is used to clock the data-out signal into the peripheral devices.

Data out (pin 3)

The 14 bits serial, binary, output code of the A/D converter starting with the most significant bit (MSB). The data must be considered valid at the trailing edge of the data-strobe signal.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive supply (pin 5)	V_P	0 to 7 V
Negative supply voltage (pin 6)	$-V_{N1}$	0 to 7 V
Negative supply voltage (pin 9)	$-V_{N2}$	0 to 20 V
Storage temperature	T_{stg}	−55 to + 150 °C
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Total power dissipation	P_{tot}	derating curve (Fig. 2)

CHARACTERISTICS (see application circuit Fig. 4)

$V_P = 5$ V; $-V_{N1} = 5$ V; $-V_{N2} = 17$ V; $T_{amb} = +25$ °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Positive supply voltage (pin 5)	V_P	4	5	6	V
Negative supply voltage 1 (pin 6)	$-V_{N1}$	–	5	–	V
Negative supply voltage 2 (pin 9)	$-V_{N2}$	16,5	17	18	V
Positive supply current	I_P	–	30	40	mA
Negative supply current	$-I_{N1}$	–	37	45	mA
Negative supply current	$-I_{N2}$	–	10	13	mA
Total power dissipation	P_{tot}	–	500	–	mW
Resolution		–	14	–	bits
Analogue input					
Full scale input current offset-binary current switched off	I_{FS}	3,8	4,0	4,2	mA
Temperature coefficient pin 23 short-circuited	TC	–	t.b.f.	–	10^{-6}/K
Zero-offset offset-binary current switched off					
Offset voltage	$-V_o$	10	20	30	mV
Temperature coefficient	TC	–	t.b.f.	–	μV/K
Offset current	I_o	–	500	–	nA
Temperature coefficient	TC	–	t.b.f.	–	nA/K
Linearity					
Linearity error		–	± ¼	–	LSB
Linearity from −20 to + 70 °C		–	± ½	–	LSB
Offset binary current	I_{BO}	$0,4_{\cdot} \cdot I_{FS}$	$0,50 \cdot I_{FS}$	$0,55 \cdot I_{FS}$	mA
Temperature coefficient	TC	–	t.b.f.	–	10^{-6}/K
Signal to noise ratio*	S/N	80	84	–	dB

parameter	symbol	min.	typ.	max.	unit
Start conversion (pin 1)					
Input current					
V_{IL} (< 0,8 V)	$-I_1$	–	–	1,6	mA
V_{IH} (> 2,0 V)	I_1	–	–	40	μA
Data, strobe, status (pins 3, 4 and 2)					
Output current					
V_{OL} (< 0,6 V)	$I_{3, 4, 2}$	6,4	16	–	mA
V_{OH} (> 2,4 V)	$-I_{3, 4, 2}$	160	400	–	μA
Conversion time					
$C_{26\text{-}27}$ = 220 pF ± 1%	t_C	–	8,5	–	μs
Signal width (pin 1)					
start conversion	t_{SC}	0,2	–	t_C	μs
Delay time (pin 2)					
status out	t_{SD}	–	60	–	ns
Set-up time (pin 3)					
data out	t_{DS}	–	25	–	ns
Pulse duration (pin 4)					
data strobe high	t_{DSH}	–	125	–	ns

* Signal-to-noise ratio within 10 Hz and 20 kHz bandwidth of a 1 kHz full scale sinewave, generated at a sample rate of 44 kHz.

DEVELOPMENT DATA

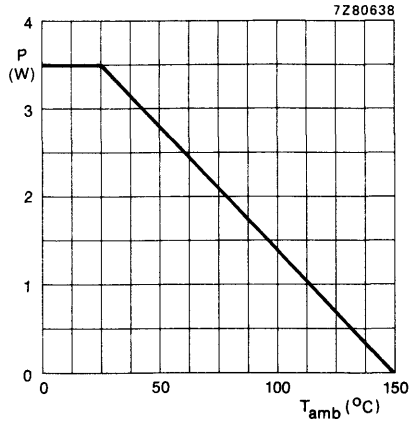


Fig. 2 Power derating curve.

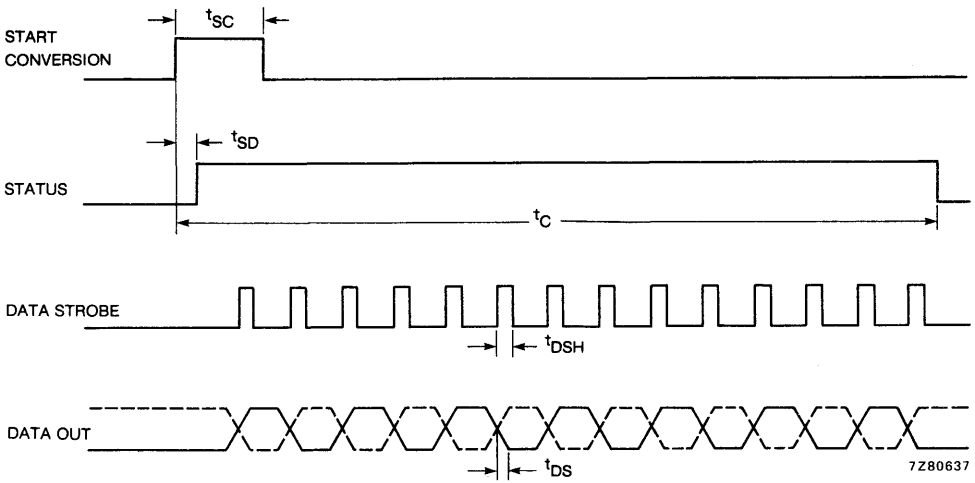


Fig. 3 Switching times waveforms.

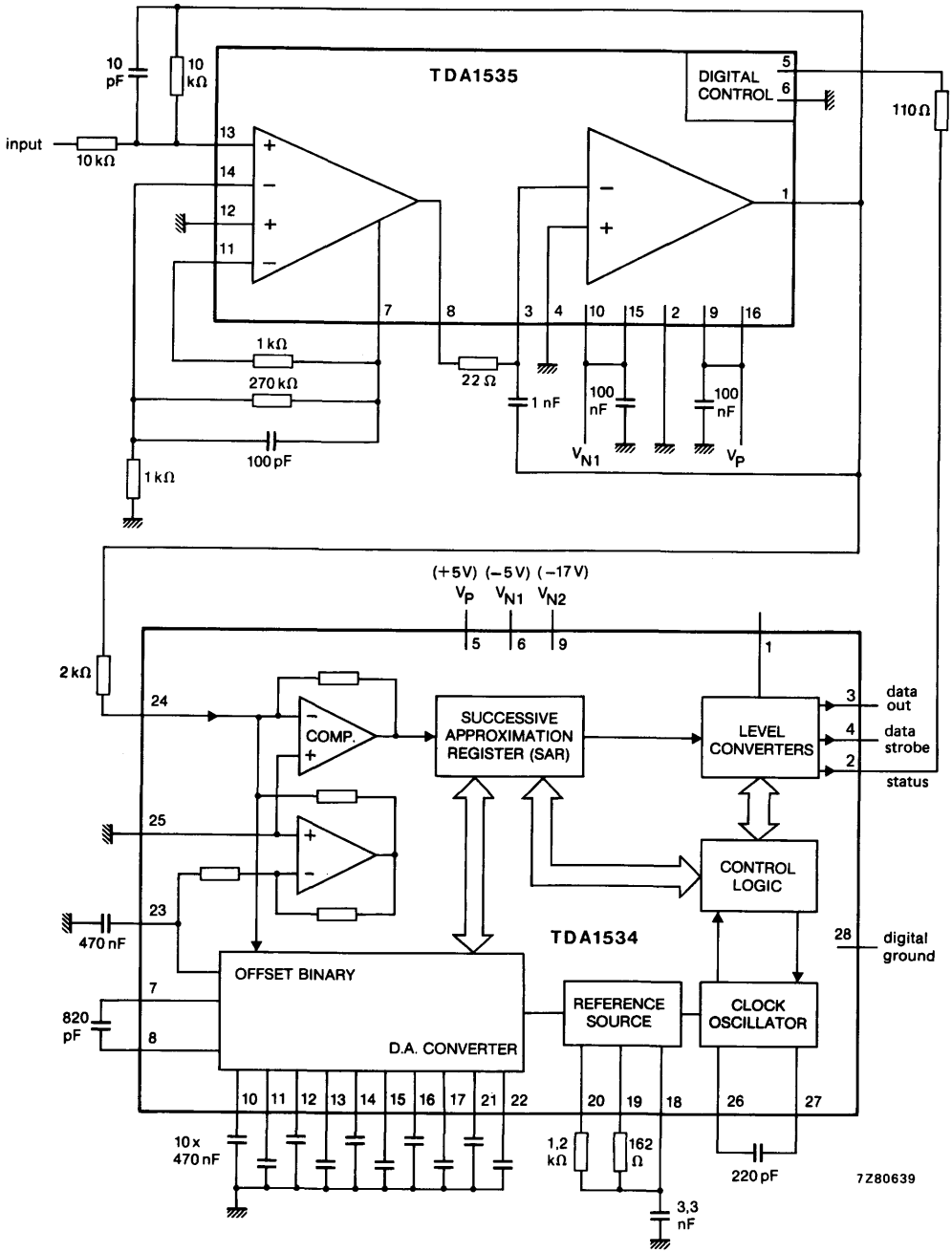


Fig. 4 Application and test circuit.

All earthed components connected to analogue ground (pin 25).

HIGH-SPEED SAMPLE AND HOLD AMPLIFIER

GENERAL DESCRIPTION

The TDA1535 is a high speed sample and hold amplifier with a total harmonic distortion of 0,001%, and a very high signal-to-noise ratio.

The excellent performance of the circuit makes it suitable for data acquisition systems with resolutions up to 16 bits, such as hi-fi digital audio equipment. The control input is TTL compatible.

Features

- High speed operational amplifier with two switchable inputs
- Wide band switchable class-B output stage
- High speed, low distortion operational amplifier with on chip JFET input stage
- Control circuit with TTL input

QUICK REFERENCE DATA

Positive supply voltage	V_P	typ.	5	V
Negative supply voltage	V_N	typ.	−5	V
Total harmonic distortion	THD	typ.	−100	dB
Signal-to-noise ratio	S/N	typ.	110	dB
Acquisition time to 0,001% (8 V step)	t_{AC}	typ.	2	μs
Small signal bandwidth	B	typ.	2	MHz
Droop rate	dV/dt	typ.	50	mV/s
Total power dissipation	P_{tot}	typ.	430	mW
Operating ambient temperature range	T_{amb}	−20 to	+ 70	°C
Storage temperature range	T_{stg}	−55 to	+ 150	°C

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT38).

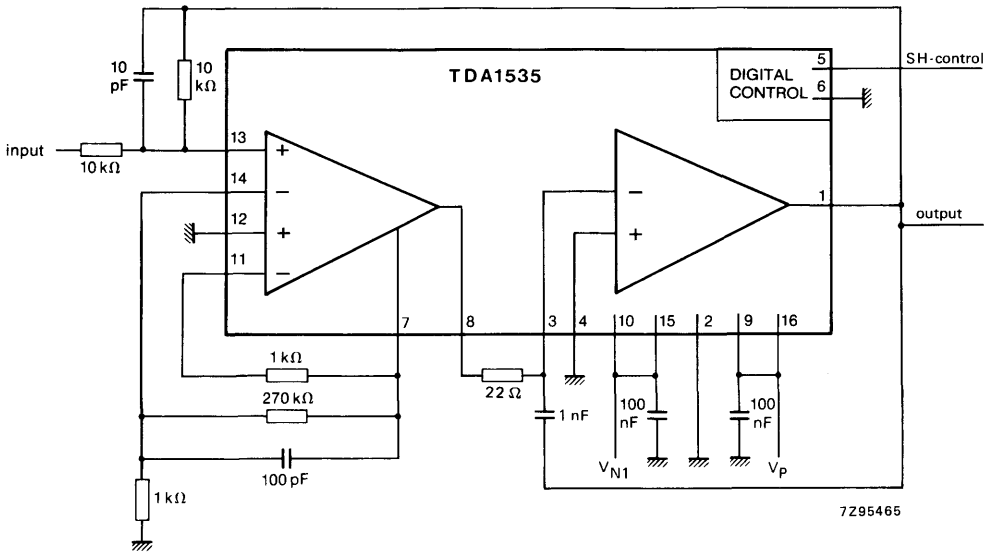


Fig. 1 Block and test diagram. All capacitors micro-poco.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

	symbol	min.	typ.	max.	unit
Positive supply voltage	V_P	0	–	10	V
Negative supply voltage	V_N	0	–	−10	V
Crystal temperature range	T_{cr}	−55	–	+ 150	°C
Storage temperature range	T_{stg}	−55	–	+ 150	°C
Operating ambient temperature range	T_{amb}	−20	–	+ 70	°C

CHARACTERISTICS

V_P = + 5 V; V_N = −5 V; T_{amb} = + 25 °C, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Positive supply voltage	V_P	4	5	8	V
Negative supply voltage	V_N	−4	−5	−8	V
Positive supply current	I_P	–	27	–	mA
Negative supply current	I_N	–	27	–	mA
Total power dissipation	P_{tot}	–	270	–	mW
Total harmonic distortion (notes 1, 2 and 3)	THD	–	−100	–	dB
Signal-to-noise ratio (notes 1, 2 and 3)	S/N	–	110	–	dB
Gain (note 2)	G	tbf	−1	–	V/V
Acquisition time to 0,001% (8 V step)	t_{AU}	–	2	–	μs
Aperture uncertainty	t_{SU}	–	tbd	0,5	ns
Small signal bandwidth	B	–	2	–	MHz
Droop rate	dV/dt	–	50	tbd	mV/s
Track to hold (pedestal) offset step	V_{SHO}	–	2	tbf	mV
Input voltage	V_i	–	–	± 4	V
Digital input voltage (logic "1")	V_{IH}	2	–	V_P	V
Digital input current, hold mode	I_{IH}	–	–	20	μA
Digital input voltage, track mode (logic "0")	V_{IL}	0	–	0,8	V
Digital input current, track mode	I_{IL}	–	–	−400	μA

DEVELOPMENT DATA

Notes to the characteristics

1. Over audio band (20 Hz to 20 kHz).
2. Tracking mode.
3. At maximum input signal.

DUAL 16-BIT DAC

GENERAL DESCRIPTION

The TDA1541A is a monolithic integrated dual 16-bit digital-to-analogue converter (DAC) designed for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders.

Features

- Selectable two-channel input format: offset binary or two's complement
- Internal timing and control circuit
- TTL compatible digital inputs
- High maximum input bit-rate and fast settling time
- No requirement for external deglitcher circuitry

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltages					
pin 28	V_{DD}	4,5	5,0	5,5	V
pin 26	$-V_{DD1}$	4,5	5,0	5,5	V
pin 15	$-V_{DD2}$	14,0	15,0	16,0	V
Supply currents					
pin 28	I_{DD}	–	27	40	mA
pin 26	$-I_{DD1}$	–	37	50	mA
pin 15	$-I_{DD2}$	–	25	35	mA
Signal-to-noise ratio (including THD) (full-scale sinewave) at analogue outputs (AOL; AOR)	S/(N + D)	90	95	–	dB
Non-linearity at T_{amb} = −20 to + 85 °C	NL	–	0,5	1,0	LSB
Current settling time to ± 1 LSB	t_{cs}	–	0,5	–	μs
Input bit rate at data input (pins 3 and 4)	BR	–	–	6,4	Mbits/s
Clock frequency at clock input (pin 2)	f_{BCK}	–	–	6,4	MHz
Full scale temperature coefficient at analogue outputs (AOL; AOR)	TC_{FS}	–	± 200 x 10^{-6}	–	K^{-1}
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C
Total power dissipation	P_{tot}	–	700	–	mW

PACKAGE OUTLINE

28-lead DIL; plastic with internal heat spreader (SOT117).

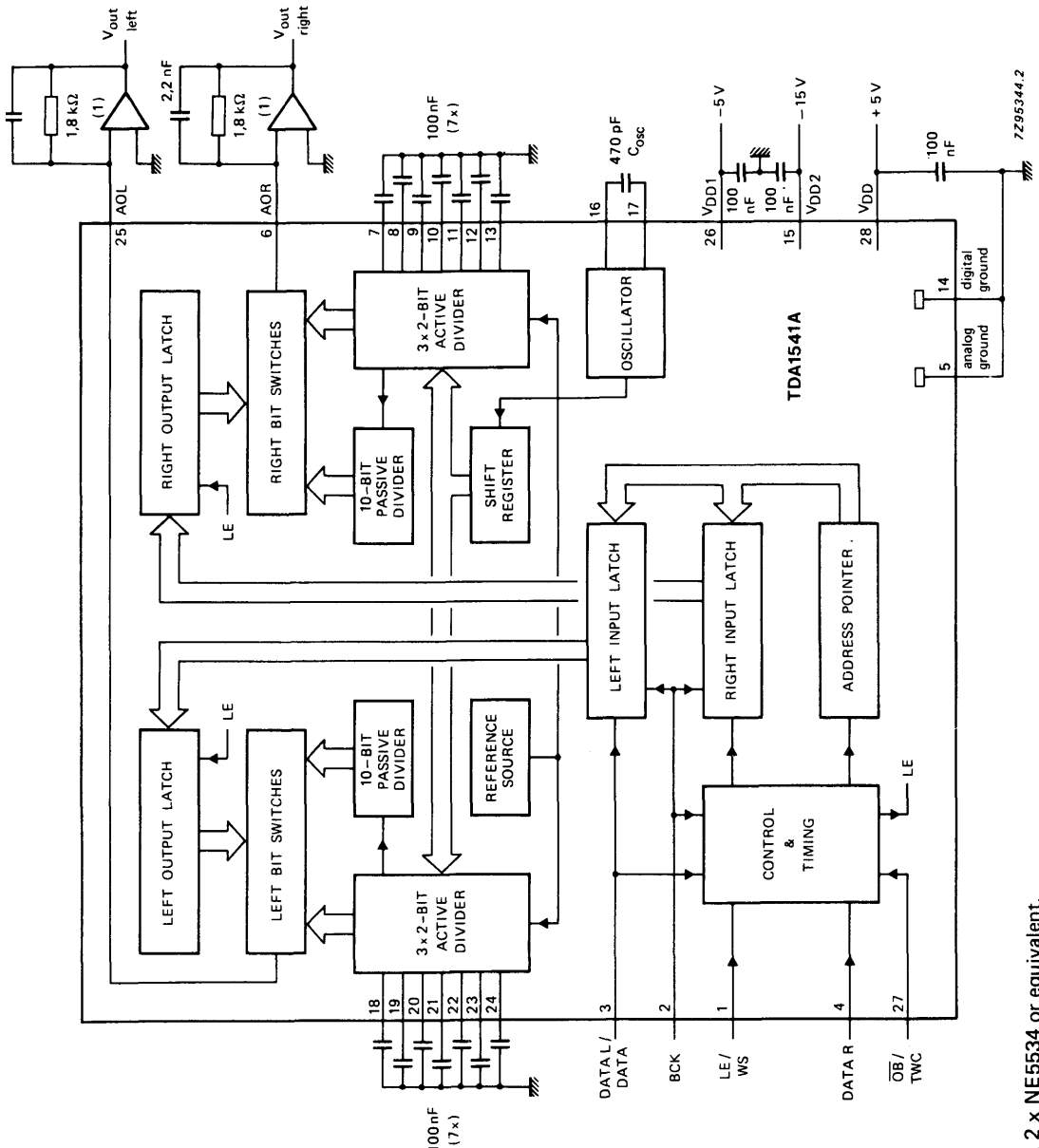


Fig. 1 Block diagram.

(1) TDA1542, 2 x NE5534 or equivalent.

DEVELOPMENT DATA

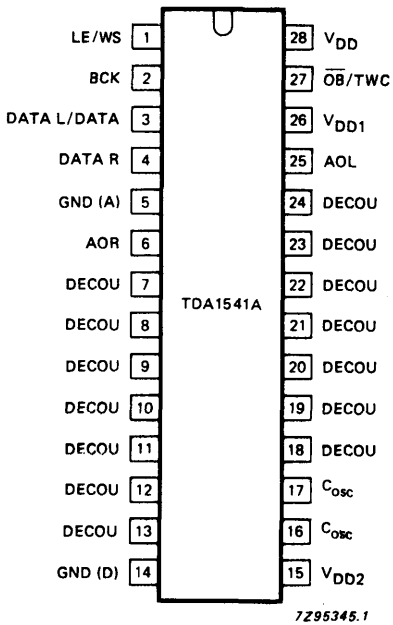


Fig. 2 Pinning diagram.

PINNING

1	LE/WS*	latch enable input word select input
2	BCK*	bit clock input
3	DATA L/DATA*	data left channel input data input (selected format)
4	DATA R*	data right channel input
5	GND (A)	analogue ground
6	AOR	right channel output
7	DECOU	decoupling
8	DECOU	
9	DECOU	
10	DECOU	
11	DECOU	
12	DECOU	
13	DECOU	
14	GND (D)	digital ground
15	V_{DD2}	−15 V supply voltage
16	COSC	oscillator
17	COSC	
18	DECOU	decoupling
19	DECOU	
20	DECOU	
21	DECOU	
22	DECOU	
23	DECOU	
24	DECOU	
25	AOL	left channel output
26	V_{DD1}	−5 V supply voltage
27	$\overline{OB}$/TWC*	mode selection input
28	V_{DD}	+ 5 V supply voltage

* See Table 1 data selection input.

FUNCTIONAL DESCRIPTION

The TDA1541A accepts input sample formats in time multiplexed mode or simultaneous mode with any bit length. The most significant bit (MSB) must always be first.
This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit-rate and fast settling time facilitates application in 4 x oversampling systems (44,1 kHz to 176,4 kHz or 48 kHz to 192 kHz) with the associated simple analogue filtering function (low order, linear phase filter).

Input data selection (see also Table 1)

With input $\overline{OB}$/TWC connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. The converted samples appear at the output, at the first positive going transition of the bit clock signal after a negative going transition of the word select signal.

With $\overline{OB}$/TWC connected to V_{DD} the mode is the same but the data format must be in two's complement.

When input $\overline{OB}$/TWC is connected to V_{DD1} the two channels of data (L/R) are input simultaneously via DATA L and DATA R, accompanied with BCK and a latch-enable input (LE). With this mode selected the data must be in offset binary. The converted samples appear at the output at the positive going transition of the latch enable signal.

The format of data input signals is shown in figures 3 and 4.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current-divider, based on emitter scaling.
All digital inputs are TTL compatible.

Table 1 Input data selection

$\overline{OB}$/TWC	mode	pin 1	pin 2	pin 3	pin 4
−5 V	simultaneous	LE	BCK	DATA L	DATA R
0 V	time MUX OB	WS	BCK	DATA OB	not used
+ 5 V	time MUX TWC	WS	BCK	DATA TWC	not used

Where:

LE = latch enable
WS = word select, LOW = left channel; HIGH = right channel
BCK = bit clock
DATA L = data left
DATA R = data right
DATA OB = data offset binary
DATA TWC = data two's complement
MUX OB = multiplexed offset binary
MUX TWC = multiplexed two's complement = I^2S – format.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage ranges				
pin 28	V_{DD}	0	7	V
pin 26	$-V_{DD1}$	0	7	V
pin 15	$-V_{DD2}$	0	17	V
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Electrostatic handling*	V_{es}	−1000	+ 1000	V

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 30 K/W

DEVELOPMENT DATA

* Equivalent to discharging a 250 pF capacitor through a 1 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; $-V_{DD1}$ = 5 V; $-V_{DD2}$ = 15 V; T_{amb} = + 25 °C; measured in the circuit of Fig. 1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage ranges						
pin 28		V_{DD}	4,5	5,0	5,5	V
pin 26		$-V_{DD1}$	4,5	5,0	5,5	V
pin 15		$-V_{DD2}$	14,0	15,0	16,0	V
Voltage difference between analogue and digital ground		$V_{GND(A)} - V_{GND(D)}$	−0,3	0	+ 0,3	V
Supply currents						
pin 28		I_{DD}	–	27	40	mA
pin 26		$-I_{DD1}$	–	37	50	mA
pin 15		$-I_{DD2}$	–	25	35	mA
Inputs						
Input current pins (1, 2, 3 and 4)						
digital inputs LOW	0,8 V	$-I_{IL}$	–	–	0,4	mA
digital inputs HIGH	2,0 V	I_{IH}	–	–	20	μA
Digital input current (pin 27)						
+ 5 V		$\|I_{\overline{OB}/TWC}\|$	–	–	1	μA
0 V		$\|I_{\overline{OB}/TWC}\|$	–	–	20	μA
−5 V		$\|I_{\overline{OB}/TWC}\|$	–	–	40	μA
Input frequency/bit rate						
clock input pin 2		f_{BCK}	–	–	6,4	MHz
data inputs pins 3 and 4		f_{DAT}	–	–	6,4	Mbits/s
word select input pin 1		f_{WS}	–	–	200	kHz
latch enable pin 1		f_{LE}	–	–	200	kHz
Input capacitance of digital inputs		C_I	–	12	–	pF
Oscillator (pins 16 and 17)						
Oscillator frequency	C_{osc} = 470 pF	f_{osc}	150	200	275	kHz
Analogue outputs (note 1) (AOL, AOR)						
Resolution		Res	–	16	–	bits
Full scale current		I_{FS}	3,4	4,0	4,6	mA
Zero scale current		$\|I_{ZS}\|$	–	25	50	nA
Full scale temperature coefficient	T_{amb} = − 20 to + 85 °C	TC_{FS}	–	± 200 x 10^{-6}	–	K^{-1}

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Linearity error integral	T_{amb} = 25 °C	E_L	–	0,5	1,0	LSB
	T_{amb} = −20 to + 85 °C	E_L	–	–	1,0	LSB
Linearity error differential	T_{amb} = 25 °C	E_{dL}	–	0,5	1,0	LSB
	T_{amb} = −20 to + 85 °C	E_{dL}	–	–	1,0	LSB
Total harmonic distortion		THD	–	−100	–	dB
Signal-to-noise ratio (including THD)	note 2	S/(N + D)	90	95	–	dB
Settling time ± 1 LSB		t_{cs}	–	0,5	–	μs
Channel separation		α	90	98	–	dB
Unbalance between outputs		$\lvert\Delta\rvert_{FS}\rvert$	–	0,1	0,3	dB
Time delay between outputs		t_d	–	–	0,2	μs
Supply voltage ripple rejection	note 3					
V_{DD} = + 5 V		SVRR	–	−76	–	dB
V_{DD1} = −5 V		SVRR	–	−84	–	dB
V_{DD2} = −15 V		SVRR	–	−58	–	dB
Signal-to-noise ratio						
at bipolar zero		S/N	–	110	–	dB
at full scale		S/N	98	104	–	dB
Timing	Figs 3 and 4					
Rise time		t_r	–	–	32	ns
Fall time		t_f	–	–	32	ns
Bit clock cycle time		t_{CY}	156	–	–	ns
Bit clock HIGH time		t_{HB}	46	–	–	ns
Bit clock LOW time		t_{LB}	46	–	–	ns
Bit clock fall time to latch enable rise time		t_{FBRL}	0	–	–	ns
Bit clock rise time to latch enable fall time		t_{RBFL}	0	–	–	ns
Data set-up time		$t_{SU;DAT}$	32	–	–	ns
Data hold time to bit clock		$t_{HD;DAT}$	0	–	–	ns
Word select hold time		$t_{HD;WS}$	0	–	–	ns
Word select set-up time		$t_{SU;WS}$	32	–	–	ns

Notes to the characteristics

1. To ensure no performance losses, permitted output voltage compliance is ± 25 mV maximum.
2. Signal-to-noise ratio + THD with 1 kHz full scale sinewave generated at a sampling rate of 176,4 kHz.
3. V_{ripple} = 100 mV and f_{ripple} = 100 Hz.

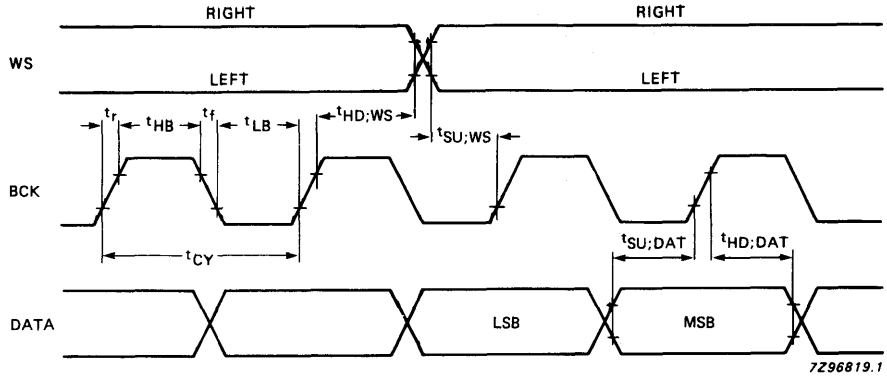


Fig. 3 Format of input signals; time multiplexed (I^2S format).

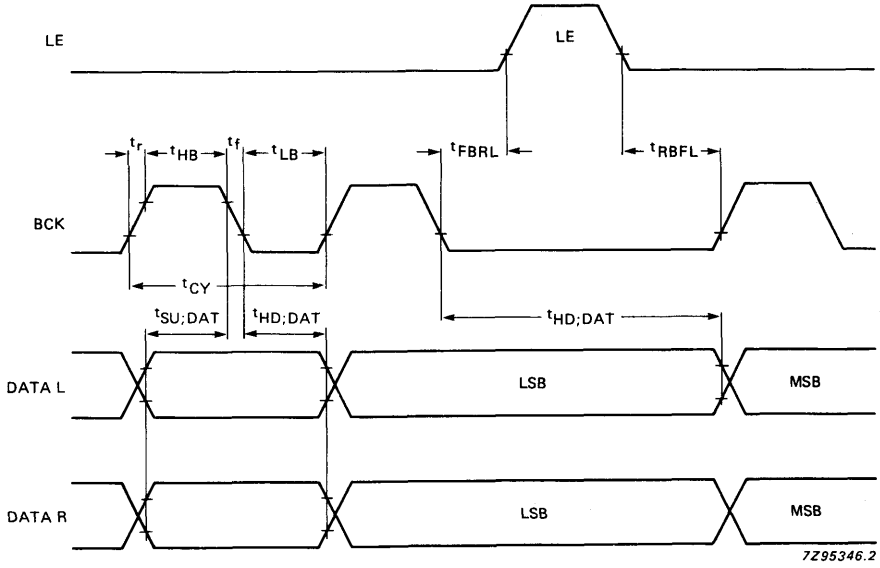


Fig. 4 Format of input signals; simultaneous data.

ACTIVE ELEMENT FOR POST FILTERING.

GENERAL DESCRIPTION

The TDA1542 is a dual channel monolithic integrated circuit encapsulated in a 28 pin DIL plastic package. Each channel incorporates five high performance amplifiers and is designed for use in hi-fi digital audio equipment such as a compact disc player.

Features

- Mute function for click and plop free switching (on and off)
- Switch function for activating a de-emphasis circuit
- Two separate output amplifiers per channel
- Flexible use of filtering
- Extremely low distortion
- High slew-rate input amplifier

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 28		V_{DD1}	4.75	12.0	13.0	V
pin 1		V_{DD2}	4.5	5.0	5.5	V
pin 26		$-V_{DD3}$	4.75	12.0	13.0	V
Input amplifier (A)						
Slew-rate		$\Delta V/\Delta t$	–	30	–	V/μs
Line amplifier (D)						
Output voltage (pins 10 and 19) (r.m.s. value)		$V_{O(rms)}$	1.9	2	–	V
Signal to noise ratio		S/N	110	115	–	dB
Total harmonic distortion	R_L = 1 kΩ	THD	–	−110	−100	dB
Channel separation		α	95	100	–	dB
Headphone amplifier (E)						
Output voltage (pins 13 and 16) (r.m.s. value)		$V_{O(rms)}$	–	6	–	V
Signal to noise ratio		S/N	110	115	–	dB
Total harmonic distortion	R_L = 600 Ω	THD	–	−110	−100	dB
Channel separation		α	95	100	–	dB
Filter amplifiers (A, B and C)						
Amplifiers conform to line amplifier D, without mute function						

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT117).

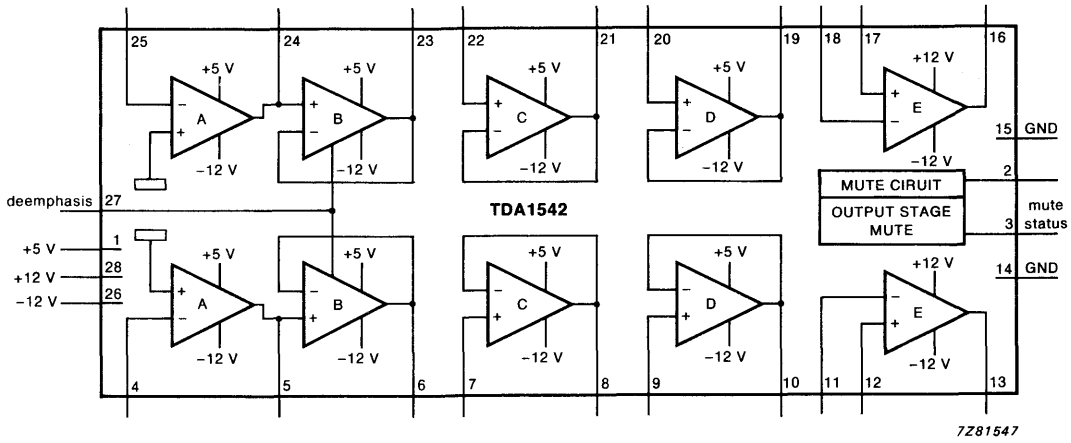


Fig. 1 Block diagram.

PINNING

1	+5 V supply voltage (V_{DD2})	15	Ground left
2	Mute timing capacitor	16	Amplifier E left output
3	Mute status	17	Amplifier E left non-inverting input
4	Amplifier A right input	18	Amplifier E left inverting input
5	Amplifier A right output/Amplifier B input	19	Amplifier D left output
6	Amplifier B right output	20	Amplifier D left input
7	Amplifier C right input	21	Amplifier C left output
8	Amplifier C right output	22	Amplifier C left input
9	Amplifier D right input	23	Amplifier B left output
10	Amplifier D right output	24	Amplifier A left output/Amplifier B input
11	Amplifier E right inverting input	25	Amplifier A left input
12	Amplifier E right non-inverting input	26	−12 V supply voltage (V_{DD3})
13	Amplifier E right output	27	De-emphasis on/off function
14	Ground right	28	+12 V supply voltage (V_{DD1})

FUNCTIONAL DESCRIPTION

The TDA1542 is a high performance, dual channel device designed to perform post filtering in a compact disc player. Since only the active part of the filter is integrated, the user has the option of selecting the desired filter type e.g. Bessel or Cauer etc. Each channel contains two separate output amplifiers, one with fixed gain for line output and the other with variable gain for driving low/high impedance headphones.

A switchable buffer amplifier is incorporated to enable the deemphasis function without producing clicks.

A mute circuit is incorporated to prevent spurious signals appearing at the output.

Both amplifiers are muted, for a preset period of time, when the 5 V supply is switched on or off. An external capacitor determines the mute time. When the mute time has elapsed the signal path is switched directly to the output, without clicks. The mute circuit status is available externally.

The TDA1542 is designed to operate over a wide supply voltage range.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage ranges					
pin 28		V_{DD1}	0	18	V
pin 1		V_{DD2}	0	7	V
pin 26		$-V_{DD3}$	0	18	V
Storage temperature range		T_{stg}	−65	150	°C
Operating ambient temperature range		T_{amb}	−30	85	°C
Electrostatic handling *		V_{es}	–	600	V

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 30 K/W

DEVELOPMENT DATA

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

V_{DD1} = + 12 V; V_{DD2} = + 5 V; V_{DD3} = −12 V; T_{amb} = 25 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 28		V_{DD1}	4.75	12.0	13.0	V
pin 1		V_{DD2}	4.5	5.0	5.5	V
pin 26		$-V_{DD3}$	4.75	12.0	13.0	V
Supply current						
pin 28		I_{DD1}	–	12	18	mA
pin 1		I_{DD2}	–	34	51	mA
pin 26		$-I_{DD3}$	–	46	69	mA
Input current						
Amplifier A (pins 4 and 25)		I_{IA}	–	1	2	μA
Amplifier C (pins 7 and 22)		I_{IC}	–	320	600	nA
Amplifier D (pins 9 and 20)		I_{ID}	–	50	150	nA
Amplifier E (pins 11 and 18)		I_{IE}	–	300	600	nA
Amplifier E (pins 12 and 17)		I_{IE}	–	30	150	nA
Offset voltage						
Amplifier A (pins 4 and 25)		$\lvert V_{IAos}\rvert$	–	1.2	7.0	mV
Amplifier B (pins 6 and 23)		$\lvert V_{IBos}\rvert$	–	0.5	7.0	mV
Amplifier C (pins 8 and 21)		$\lvert V_{ICos}\rvert$	–	0.6	7.0	mV
Amplifier D (pins 10 and 19)		$\lvert V_{IDos}\rvert$	–	1.0	3.0	mV
Amplifier E (pins 11 and 18)		$\lvert V_{IEos}\rvert$	–	0.7	3.0	mV
Mute timing capacitor (pin 2)						
Switch-on voltage		V_{sw}	–	3.5	4.1	V
Loading current		$-I_L$	0.1	0.5	2.0	mA

DEVELOPMENT DATA

AC CHARACTERISTICS

V_{DD1} = + 12 V; V_{DD2} = + 5 V; V_{DD3} = −12 V; T_{amb} = 25 °C; f = 1 kHz; measured in Fig. 2

parameter	conditions	symbol	min.	typ.	max.	unit
Amplifier A to Amplifier E						
Open loop gain		G_{ol}	–	90	–	dB
Overall distortion without de-emphasis		THD	–	−110	−100	dB
Slew rate (Amplifier A)		$\Delta V/\Delta t$	–	30	–	V/μs
Supply voltage ripple rejection						
V_{DD1}	note 1	SVRR	50	60	–	dB
V_{DD2}	note 2	SVRR	50	60	–	dB
V_{DD3}	note 2	SVRR	55	70	–	dB
Line amplifier D						
Output voltage (pins 10 and 19) (r.m.s. value)		$V_{O(rms)}$	1.9	2.0	–	V
Signal to noise ratio	B = 20 Hz to 20 kHz	S/N	110	115	–	dB
Total harmonic distortion		THD	–	−110	−100	dB
Channel separation		α	95	100	–	dB
Output impedance		Z_O	–	–	0.5	Ω
Difference between mute ON and mute OFF output voltage (pins 10 and 19)		V_O	–	–	4	mV
Headphone amplifier (E)						
Output voltage (pins 13 and 16) (r.m.s. value)	R_L = 600 Ω	$V_{O(rms)}$	–	6	–	V
	R_L = 132 Ω	$V_{O(rms)}$	–	5.5	–	V
Signal to noise ratio	B = 20 Hz to 20 kHz	S/N	110	115	–	dB
Total harmonic distortion	R_L = 600 Ω	THD	–	−110	−100	dB
Total harmonic distortion	R_L = 132 Ω	THD	–	−88	−80	dB
Channel separation	20 Hz to 20 kHz; R_L = 600 Ω	α	95	100	–	dB
Output impedance		Z_O	–	–	0.5	Ω
Difference between mute ON and OFF output voltage (pins 13 and 16)		V_O	–	–	6	mV

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Mute status (pin 3)	open collector output					
Output voltage LOW (mute ON)	$-I_{OL} = 3$ mA	–	–	–	0.4	V
Output voltage HIGH (mute OFF)	$I_{OL} \leqslant 1$ μA		2.4	–	V_{DD1}	V
Mute timing	note 3					
De-emphasis switch						
Input voltage HIGH	De-emphasis ON	V_{IH}	2.4	–	V_{DD1}	V
Input voltage LOW	De-emphasis OFF	V_{IL}	0	–	1	V
Input current HIGH	De-emphasis ON	I_{IH}	–	–	5.0	μA
Input current LOW	De-emphasis OFF	$-I_{IL}$	–	–	25	μA

Notes to the characteristics

1. The ripple rejection is measured at the output of the line amplifier; amplitude = 0.5 V_{tt}; f = 100 Hz to 10 kHz.
2. The ripple rejection is measured at the output of the line amplifier; amplitude = 1 V_{tt}; f = 100 Hz to 10 kHz.
3. The mute timing is provided by an external capacitor connected to pin 2.

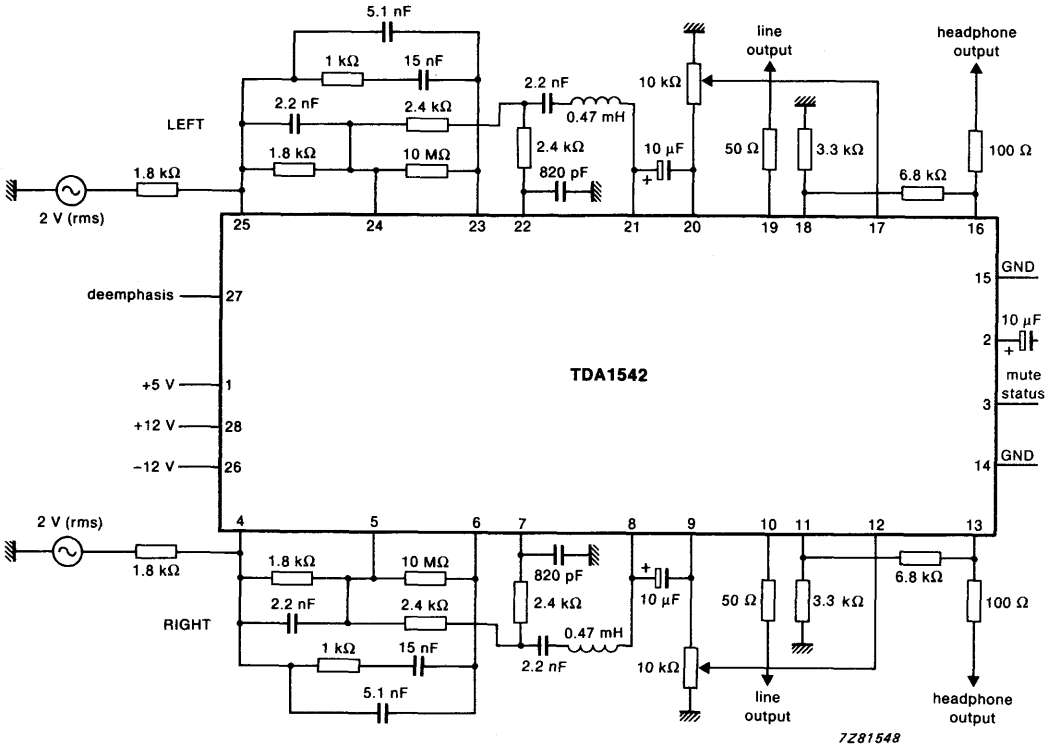


Fig. 2 Test and application circuit.

DUAL 16—BIT DAC (ECONOMY VERSION)

GENERAL DESCRIPTION

The TDA1543 is a monolithic integrated dual 16-bit digital-to-analogue converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders.

Features

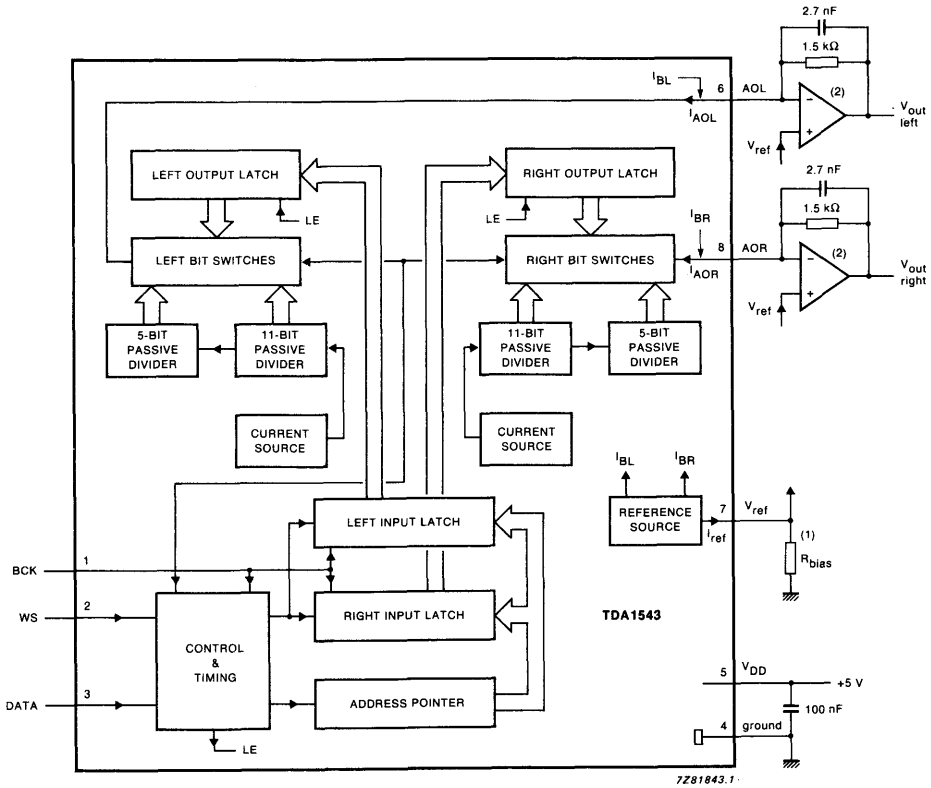
- Low distortion
- 16-bit dynamic range
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- I^2S input format: time multiplexed, two's complement, TTL

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	3.0	5.0	8.0	V
Supply current	I_{DD}	–	50	60	mA
Signal-to-noise ratio (including THD) (full-scale sinewave) at analogue outputs (AOL; AOR)	S/(N + D)	70	75	–	dB
Current settling time to ± 1 LSB	t_{cs}	–	0.5	–	μs
Input bit rate at data input (pin 3)	BR	–	–	6.4	Mbits/s
Clock frequency at clock input (pin 1)	f_{BCK}	–	–	6.4	MHz
Full scale temperature coefficient at analogue outputs (AOL; AOR)	TC_{FS}	–	$\pm 400 \times 10^{-6}$	–	K^{-1}
Operating ambient temperature range	T_{amb}	–30	–	+ 85	°C
Total power dissipation	P_{tot}	–	250	–	mW
Bias current	I_{bias}	–0.5	–	1.8	mA

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).



(1) Optional.
(2) 2 x 1/2 NE5532.

Fig. 1 Block diagram.

PINNING

1	BCK	bit clock input
2	WS	word select input
3	DATA	data input
4	GND	ground
5	V_{DD}	+ 5 V supply voltage
6	AOL	left channel output
7	V_{ref}	reference voltage output
8	AOR	right channel output

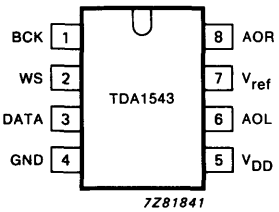
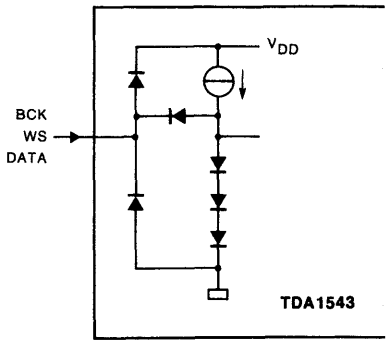
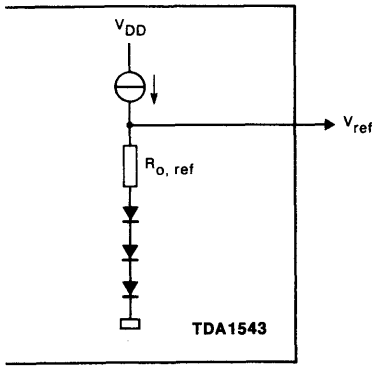


Fig. 2 Pinning diagram.

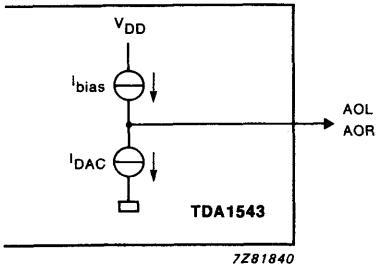
DEVELOPMENT DATA



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig. 3 Circuits at the input and output pins.

FUNCTIONAL DESCRIPTION

The TDA1543 accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig. 4.

This flexible input data format (I^2S) allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits and audio signal processors (ASP).

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig. 1).

With a LOW level on the word select (WS) input data is placed in the left input register and with a HIGH level on the WS input data is placed in the right input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	0	9	V
Crystal temperature	T_{XTAL}	–	150	°C
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 85	°C
Electrostatic handling *	V_{es}	−1000	+ 1000	V

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$		110	K/W

DEVELOPMENT DATA

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = + 25 °C; I_{ref} = 0; measured in the circuit of Fig. 1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	3.0	5.0	8.0	V
Supply current	note 1	I_{DD}	–	50	60	mA
Ripple rejection	note 2	RR	–	*	–	dB
Inputs						
Input current pins (1, 2 and 3)						
digital inputs LOW	V_I = 0.8 V	I_{IL}	–	–	–0.4	mA
digital inputs HIGH	V_I = 2.0 V	I_{IH}	–	–	20	μA
Input frequency/bit rate						
clock input pin 1		f_{BCK}	–	–	6.4	MHz
bit rate data input pin 3		BR	–	–	6.4	Mbits/s
word select input pin 2		f_{WS}	–	–	200	kHz
Input capacitance of digital inputs		C_I	–	*	–	pF
Analogue outputs (AOL; AOR)						
Resolution		Res	–	–	16	bits
Output voltage compliance						
AC		$V_{OC(AC)}$	–	± 25	–	mV
DC		$V_{OC(DC)}$	1.8	–	V_{DD}–1.2	V
Full scale current		I_{FS}	1.6	2.0	2.4	mA
Full scale temperature coefficient		TC_{FS}	–	$\pm 400 \times 10^{-6}$	–	K^{-1}
Offset current	I_{ref} = 0	I_{offset}	–0.1	0	0.1	mA
Bias current (adjustable)		I_{bias}	–0.5	–	1.8	mA
Bias current gain		AI_{bias}	1.9	2.0	2.1	

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output (V_{ref})						
Reference voltage output		V_{ref}	*	2.3	*	V
Reference current output		I_{ref}	−0.3	−	0.9	mA
Reference output impedance		$R_{o,\,ref}$	−	250	−	Ω
Signal-to-noise ratio (including THD)	note 3, Fig. 4	S/(N + D)	70	75	−	dB
Settling time ± 1 LSB		t_{cs}	−	0.5	−	μs
Channel separation		α	−	90	−	dB
Unbalance between outputs	note 3	$\lvert d_{IO}\rvert$	−	< 0.2	0.5	dB
Time delay between outputs		t_d	−	< 0.2	−	μs
Signal-to-noise ratio at bipolar zero	note 4	S/N	90	95	−	dB
Timing	Fig. 5					
Rise time		t_r	−	−	32	ns
Fall time		t_f	−	−	32	ns
Bit clock cycle time		t_{CY}	156	−	−	ns
Bit clock HIGH time		t_{HB}	46	−	−	ns
Bit clock LOW time		t_{LB}	46	−	−	ns
Data set-up time		$t_{SU;DAT}$	32	−	−	ns
Data hold time to bit clock		$t_{HD;DAT}$	0	−	−	ns
Word select hold time		$t_{HD;WS}$	0	−	−	ns
Word select set-up time		$t_{SU;WS}$	32	−	−	ns

DEVELOPMENT DATA

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. With 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
4. At code 0000H.

* Value to be fixed.

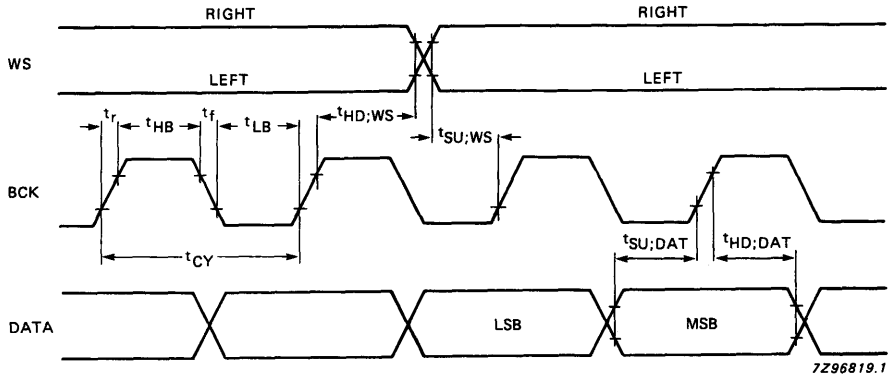


Fig. 4 Format of input signals (I^2S format).

AM RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TDA1572 integrated AM receiver circuit performs all the active functions and part of the filtering required of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle RF signals up to 500 mV.

RF radiation and sensitivity to interference are minimized by an almost symmetrical design. The controlled-voltage oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range, even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the IF amplifier.

Features

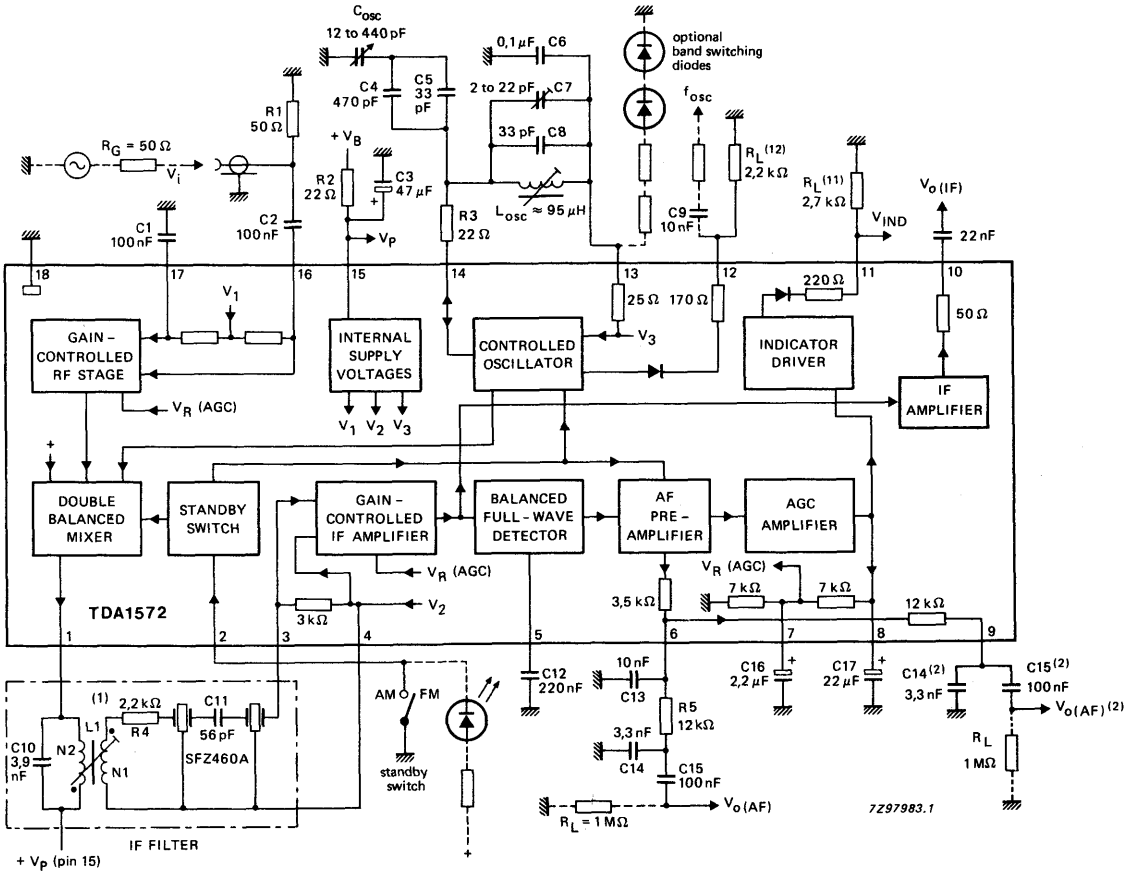
- Inputs protected against damage by static discharge
- Gain-controlled RF stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled IF stage with wide AGC range
- Full-wave, balanced envelope detector
- Internal generation of AGC voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- AF preamplifier with possibilities for simple AF filtering
- Electronic standby switch
- IF output for stereo demodulator and search tuning

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	7,5	–	18,0	V
Supply current range	I_P	15	–	30	mA
RF input voltage for (S+N)/N = 6 dB at m = 30%	$V_{i(RF)}$	–	1,5	–	μV
RF input voltage for 3% total harmonic distortion (THD) at m = 80%	$V_{i(RF)}$	–	500	–	mV
IF output voltage with V_i = 2 mV	$V_{o(IF)}$	–	230	–	mV
AF output voltage with V_i = 2 mV; f_i = 1 MHz; m = 30%; f_m = 400 Hz	$V_{o(AF)}$	–	310	–	mV
AGC range: change of V_i for 1 dB change of $V_{o(AF)}$		–	86	–	dB
Field strength indicator voltage at V_i = 500 mV; $R_{L(11)}$ = 2,7 kΩ	V_{IND}	–	2,8	–	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1 : N1/N2 = 12/32; Q_o = 65; Q_B = 57.
Filter data: Z_F = 700 Ω at R_{3-4} = 3 kΩ; Z_I = 4,8 kΩ.

(2) AF output is pin 6 is not used.

Fig. 1 Block diagram and test circuit (connections shown in broken lines are not part of the test circuit).

FUNCTIONAL DESCRIPTION

Gain-controlled RF stage and mixer

The differential amplifier in the RF stage employs an AGC negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by AGC delays at the various signal stages. Large signals are handled with low distortion and the (S+N)/N ratio of small signals is improved. Low noise working is achieved in the differential amplifier by using transistors with low base resistance.

A double balanced mixer provides the IF output signal to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{13\text{-}18}$. An extra buffered oscillator putput (pin 12) is available for driving a synthesizer. If this is not needed, resistor $R_{L(12)}$ can be omitted.

Gain-controlled IF amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the AGC negative feedback network. The IF output is available at pin 10.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. Residual IF carrier is blocked from the signal path by an internal low-pass filter.

AF preamplifier

This stage preamplifies the audio frequency output signal. The amplifier output has an emitter follower with a series resistor which, together with an external capacitor, yields the required low-pass for AF filtering.

AGC amplifier

The AGC amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the AGC voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives fast AGC settling time which is advantageous for electronic search tuning. The AGC settling time can be further reduced by using capacitors of smaller value in the external filter (C16 and C17). The AGC voltage is fed to the RF and IF stages via suitable AGC delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If the field strength information is not needed, $R_{L(11)}$ can be omitted.

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and AF preamplifier are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	$V_P = V_{15-18}$	–	20	V
Total power dissipation	P_{tot}	–	875	mW
Input voltage	$\|V_{16-17}\|$	–	12	V
	$-V_{16-18}$, $-V_{17-18}$	–	0,6	V
	V_{16-18}, V_{17-18}	–	V_P	V
Input current	$\|I_{16}\|$, $\|I_{18}\|$	–	200	mA
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−55	+ 150	°C
Junction temperature	T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$		80	K/W

CHARACTERISTICS

$V_P = V_{15-18} = 8{,}5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{IF} = 460$ kHz; measured in test circuit of Fig. 1; all voltages referenced to ground; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 15)	V_P	7,5	8,5	18,0	V
Supply current (pin 15)	I_P	15	23	30	mA
RF stage and mixer (pins 16 and 17)					
DC input voltage	V_I	–	$V_P/2$	–	V
RF input impedance at $V_I < 300\ \mu V$	Z_i	–	5,5	–	kΩ
RF input capacitance	C_i	–	25	–	pF
RF input impedance at $V_I > 10$ mV	Z_i	–	8	–	kΩ
RF input capacitance	C_i	–	22	–	pF
IF output impedance (pin 1)	Z_o	200	–	–	kΩ
IF output capacitance	C_o	–	6	–	pF
Conversion transconductance before start of AGC	I_1/V_i	–	6,5	–	mA/V
Maximum IF output voltage, inductive coupling to pin 1 (peak-to-peak value)	$V_{1-15(p-p)}$	–	5	–	V
DC value of output current; at $V_I = 0$ V (pin 1)	I_O	–	1,2	–	mA
AGC range of input stage		–	30	–	dB
RF signal handling capability: (r.m.s. value): input voltage for THD = 3% at m = 80%	$V_{i(rms)}$	–	500	–	mV

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Oscillator					
Frequency range	f_{osc}	0,1	–	60	MHz
Oscillator amplitude (pins 13 to 14)	V	–	130	150	mV
External load impedance (pins 14 to 13)	$R_{(ext)}$	0,5	–	200	kΩ
External load impedance for no oscillation (pins 14 to 13)	$R_{(ext)}$	–	–	60	Ω
Ripple rejection at $V_{P(rms)}$ = 100 mV; f_p = 100 Hz (SVRR = 20 log [V_{15}/V_{13}])	RR	–	55	–	dB
Source voltage for switching diodes (6 x V_{BE}) (pin 13)	V	–	4,2	–	V
DC output current (for switching diodes) (pin 13)	$-I_O$	0	–	20	mA
Change of output voltage at ΔI_{13} = 20 mA (switch to maximum load) (pin 13)	ΔV_I	–	0,3	–	V
Buffered oscillator output (pin 12)					
DC output voltage	V_O	–	0,8	–	V
Output signal amplitude (peak-to-peak value)	$V_{o(p-p)}$	–	320	–	mV
Output impedance	Z_O	–	170	–	Ω
Output current	$-I_{O(peak)}$	–	–	3	mA
IF, AGC and AF stages					
DC input voltage (pins 3 and 4)	V_I	–	2,0	–	V
IF input impedance (pins 3 to 4)	Z_i	2,4	3,0	3,9	kΩ
IF input capacitance	C_i	–	7	–	pF
IF input voltage for THD = 3% at m = 80% (pins 3 and 4)	V_i	–	90	–	mV
IF output impedance (pin 10)	Z_o	–	50	–	Ω
Unloaded IF output voltage at V_i = 10 mV (pin 10)	V_o	180	230	290	mV
Voltage gain before start of AGC (pins 3 to 4; 6 to 18)	G_v	–	68	–	dB
AGC range of IF stages: change of V_{3-4} for 1 dB change of $V_{o(AF)}$; $V_{3-4(ref)}$ = 75 mV	ΔV_v	–	55	–	dB
AF output voltage at $V_{3-4(IF)}$ = 50 μV	$V_{o(AF)}$	–	130	–	mV
AF output voltage at $V_{3-4(IF)}$ = 1 mV	$V_{o(AF)}$	–	310	–	mV
AF output impedance (pin 6)	$\|Z_o\|$	2,8	3,5	4,2	kΩ

parameter	symbol	min.	typ.	max.	unit
Indicator driver (pin 11)					
Output voltage at V_i = 0 mV; R_L = 2,7 kΩ	V_o	–	–	140	mV
Output voltage at V_i = 500 mV; R_L = 2,7 kΩ	V_o	2,5	2,8	3,1	V
Load resistance	R_L	1,5	–	–	kΩ
Standby switch					
Switching threshold at; V_P = 7,5 to 18 V; T_{amb} = −40 to +80 °C					
ON-voltage	V_{2-1}	0	–	2,0	V
OFF-voltage	V_{2-1}	3,5	–	20,0	V
ON-current at V_{2-1} = 0 V	$-I_2$	–	100	200	μA
OFF-current at V_{2-1} = 20 V	$\|I_2\|$	–	–	10	μA

DEVELOPMENT DATA

OPERATING CHARACTERISTICS

V_P = 8,5 V; f_i = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
RF sensitivity					
RF input required for (S+N)/N = 6 dB	V_i	–	1,5	–	μV
RF input required for (S+N)/N = 26 dB	V_i	–	15	–	μV
RF input required for (S+N)/N = 46 dB	V_i	–	150	–	μV
RF input at start of AGC	V_i	–	30	–	μV
RF large signal handling					
RF input at THD = 3%; m = 80%	V_i	–	500	–	mV
RF input at THD = 3%; m = 30%	V_i	–	700	–	mV
RF input at THD = 10%; m = 30%	V_i	–	900	–	mV
AGC range					
Change of V_i for 1 dB change of $V_{o(AF)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	86	–	dB
Change of V_i for 6 dB change of $V_{o(AF)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	91	–	dB
Output signal					
IF output voltage at V_i = 2 mV	$V_{o(IF)}$	180	230	290	mV
AF output voltage at V_i = 4 μV; m = 80%	$V_{o(AF)}$	–	130	–	mV
AF output voltage at V_i = 2 mV	$V_{o(AF)}$	240	310	390	mV
THD at V_i = 1 mV	d_{tot}	–	0,5	–	%
THD at V_i = 500 mV	d_{tot}	–	1	–	%
Signal plus noise-to-noise ratio at V_i = 100 mV	(S+N)/N	–	58	–	dB
Ripple rejection at V_i = 2 mV; $V_{P(rms)}$ = 100 mV; f_p = 100 Hz ($SVRR = 20 \log [V_P/V_{o(AF)}]$)	RR	–	38	–	dB
a) additional AF signal at IF output	RR	–	0*	–	dB
b) add modulation at IF output (m_{ref} = 30%)	RR	–	40	–	dB

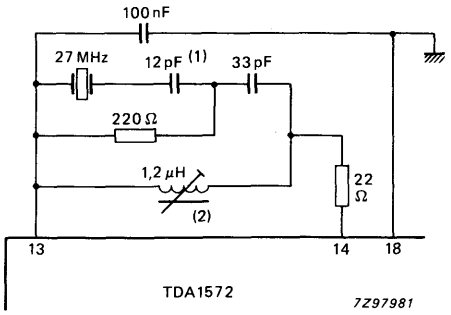
* AF signals at the IF output will be suppressed by a coupling capacitor to the demodulator and by full wave-detection in the demodulator.

parameter	symbol	min.	typ.	max.	unit
Unwanted signals					
Suppression of IF whistles at V_i = 15 μV; m = 0% related to AF signal of m = 30%					
at $f_i \approx 2 \times f_{IF}$	α_{2IF}	–	*	–	dB
at $f_i \approx 3 \times f_{IF}$	α_{3IF}	–	*	–	dB
IF suppression at RF input;					
for symmetrical input	α_{IF}	–	40	–	dB
for asymmetrical input	α_{IF}	–	40	–	dB
Residual oscillator signal at mixer output;					
at f_{osc}	$I_{1(osc)}$	–	1	–	μA
at $2 \times f_{osc}$	$I_{1(2osc)}$	–	1,1	–	μA

DEVELOPMENT DATA

* Value to be fixed.

APPLICATION INFORMATION



(1) Capacitor values depend on crystal type.
(2) Coil data: 9 windings of 0,1 mm dia laminated Cu wire on TOKO coil set 7K 199CN; $Q_o = 80$.

Fig. 2 Oscillator circuit using quartz crystal; centre frequency = 27 MHz.

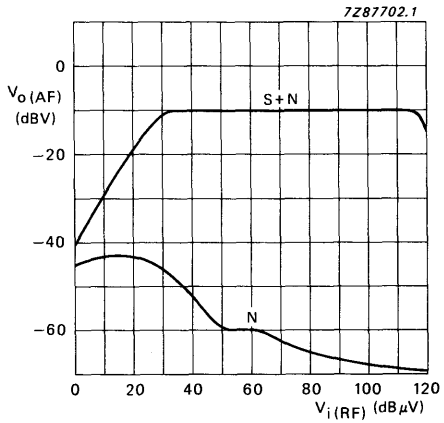


Fig. 3 AF output as a function of RF input in the circuit of Fig. 1; f_i = 1 MHz; f_m = 400 Hz; m = 30%.

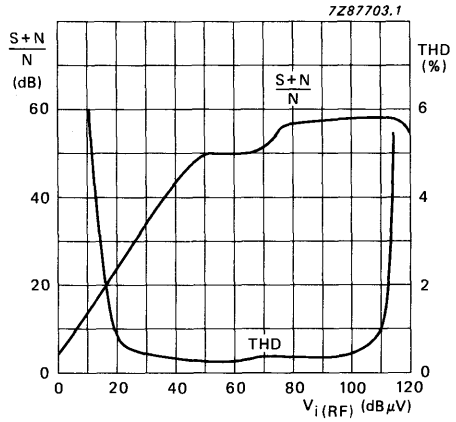


Fig. 4 Total harmonic distortion and (S + N)/N as functions of RF input in the circuit of Fig. 1; m = 30% for (S + N)/N curve and m = 80% for THD curve.

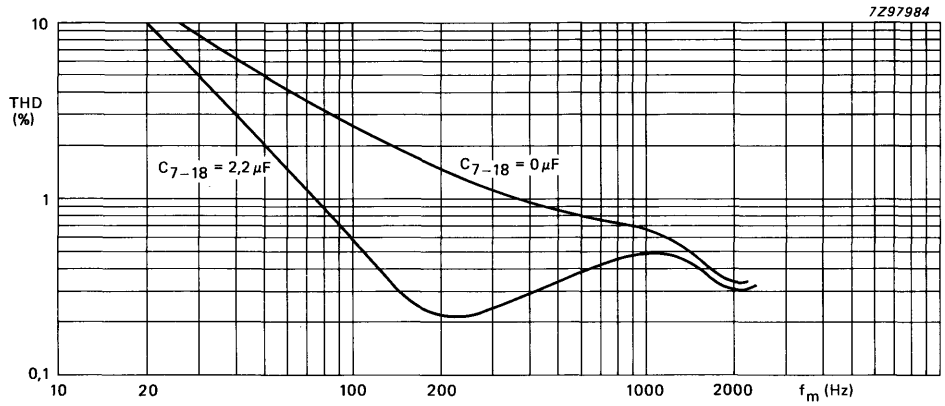


Fig. 5 Total harmonic distortion as a function of modulation frequency at V_i = 5 mV; m = 80%; measured in the circuit of Fig. 1 with $C_{7\text{-}18(ext)}$ = 0 μF and 2,2 μF.

DEVELOPMENT DATA

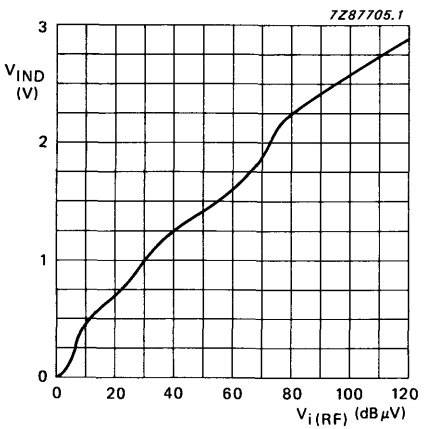


Fig. 6 Indicator driver voltage as a function of RF input in the circuit of Fig. 1.

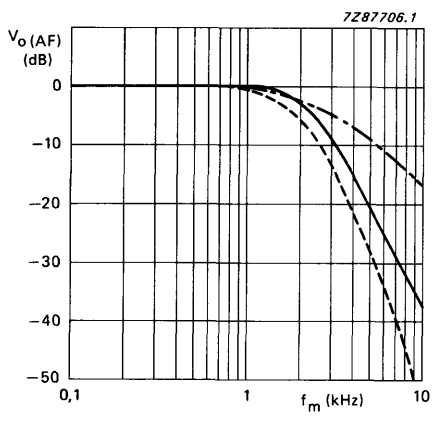


Fig. 7 Typical frequency response curves from Fig. 1 showing the effect of filtering as follows:

——— with IF filter;
—·—·— with AF filter;
– – – – – with IF and AF filters.

APPLICATION INFORMATION (continued)

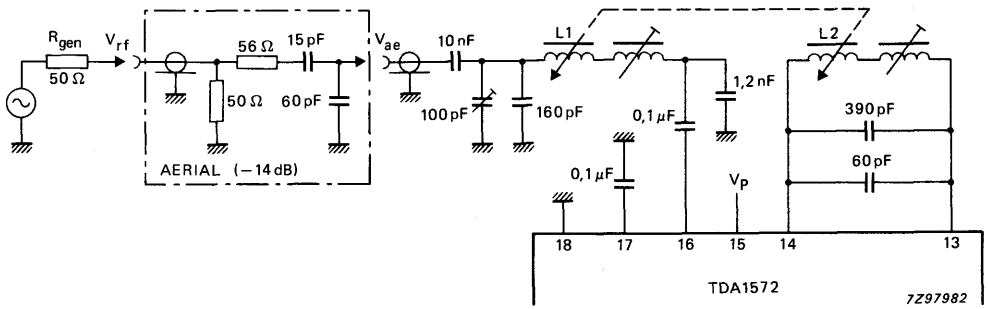


Fig. 8 Car radio application with inductive tuning.

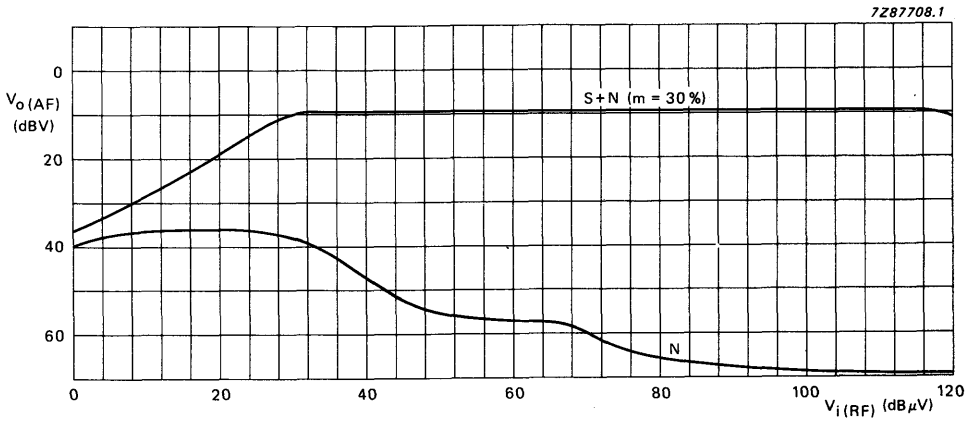


Fig. 9 AF output as a function of RF input using the circuit of Fig. 8 with that of Fig. 1.

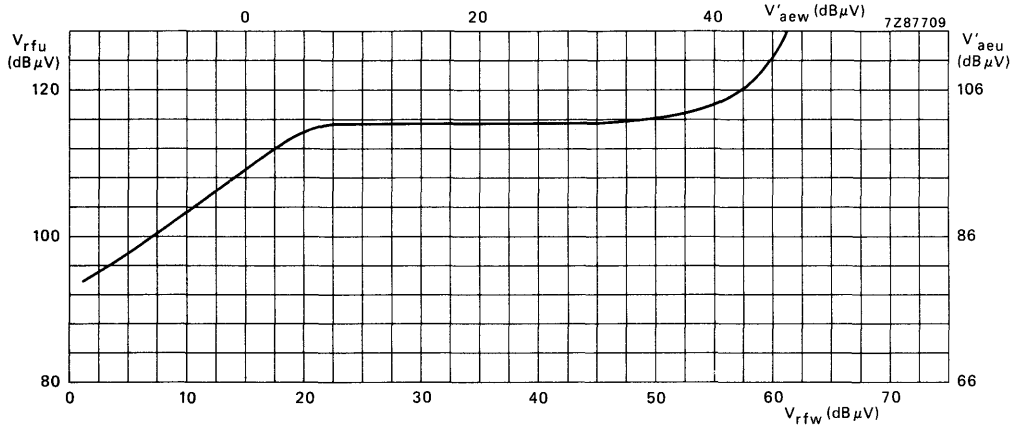


Fig. 10 Suppression of cross-modulation as a function of input signal, measured in the circuit of Fig. 8 with the input circuit as shown in Fig. 11. Curve is for Wanted $V_{o(AF)}$/Unwanted $V_{o(AF)}$ = 20 dB; V_{rfw}, V_{rfu} are signals at the aerial input, V'_{aew}, V'_{aeu} are signals at the unloaded output of the aerial.

Wanted signal (V'_{aew}, V_{rfw}): f_i = 1 MHz; f_m = 400 Hz; m = 30%.

Unwanted signal (V'_{aeu}, V_{rfu}): f_i = 900 kHz; f_m = 400 Hz; m = 30%.

Effective selectivity of input tuned circuit = 21 dB.

DEVELOPMENT DATA

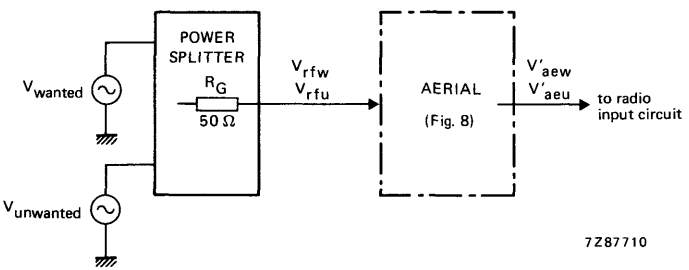


Fig. 11 Input circuit to show cross-modulation suppression (see Fig. 10).

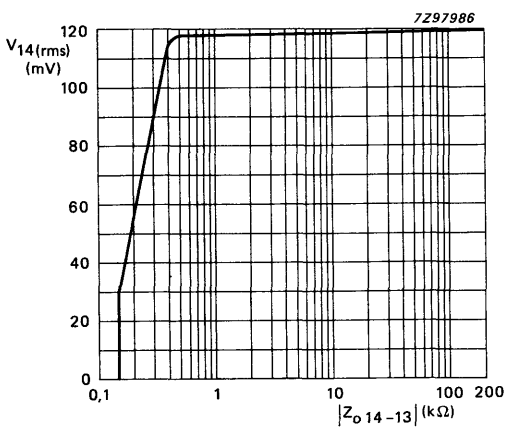


Fig. 12 Oscillator amplitude as a function of pin 13, 14 impedance in the circuit of Fig. 8.

APPLICATION INFORMATION (continued)

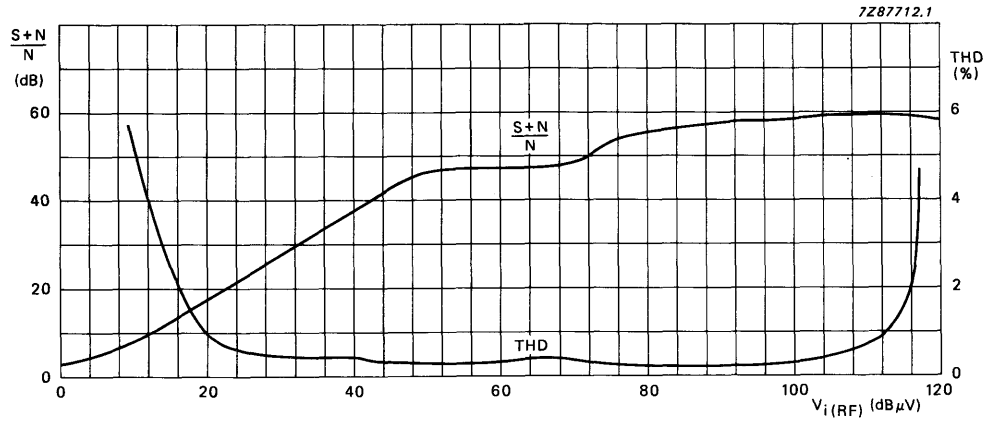


Fig. 13 Total harmonic distortion and (S + N)/N as functions of RF input using the circuit of Fig. 8 with that of Fig. 1.

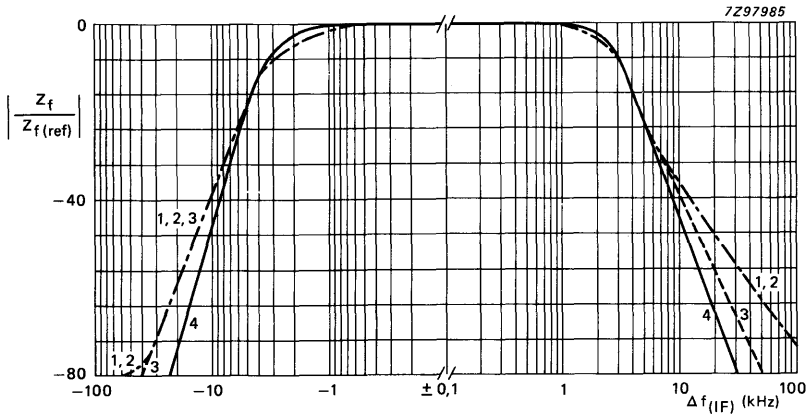


Fig. 14 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig. 15; centre frequency = 455 kHz.

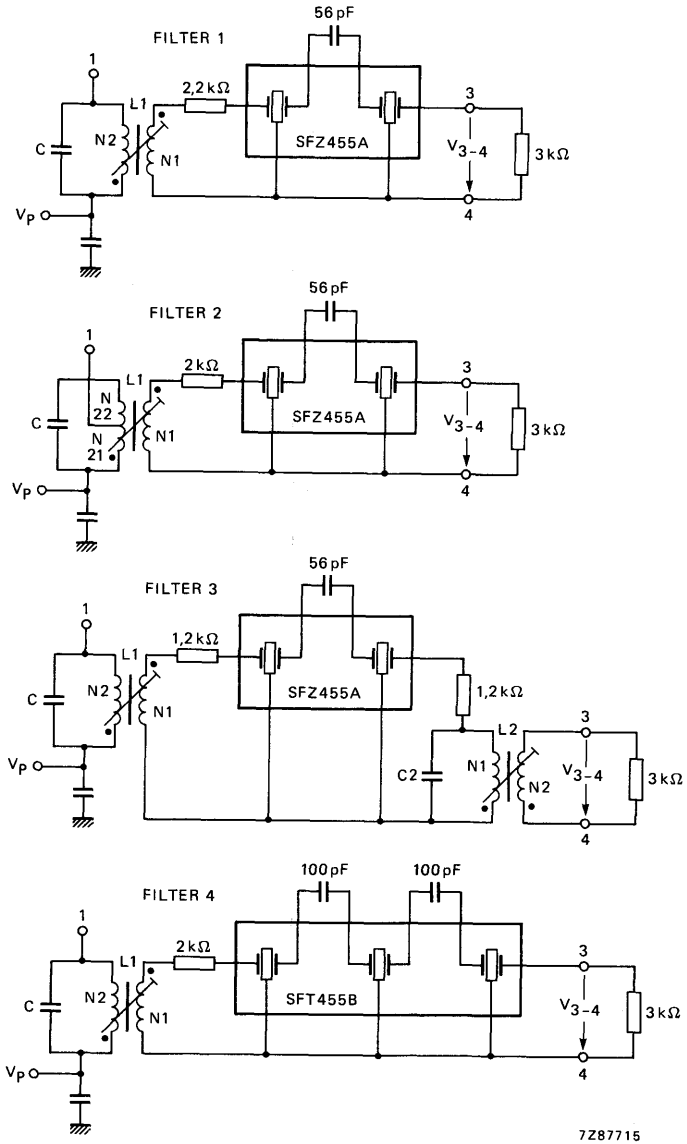


Fig. 15 IF filter variants applied to the circuit of Fig. 1. For filter data, refer to Table 1.

APPLICATION INFORMATION (continued)

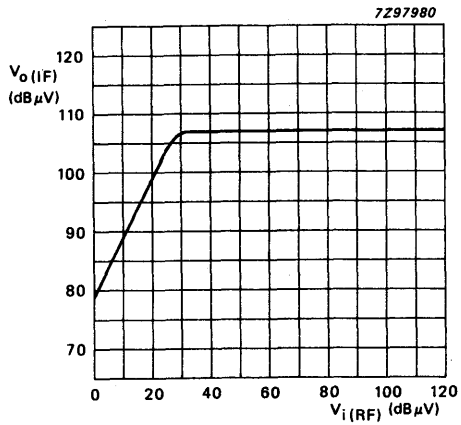
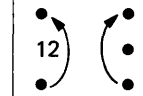
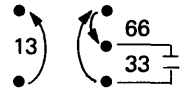
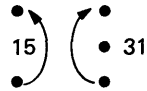
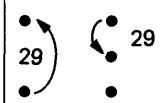
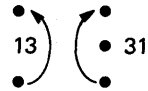


Fig. 16 IF output voltage as a function of RF input in the circuit of Fig. 1; f_i = 1 MHz.

DEVELOPMENT DATA

Table 1 Data for IF filters shown in Fig. 15. Criteria for adjustment is Z_F = maximum (optimum selectivity curve at centre frequency f_0 = 455 kHz). See also Fig. 14.

filter no.	1	2	3		4	unit
Coil data	L1	L1	L1	L2	L1	
Value of C	3900	430	3900	4700	3900	pF
N1: N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	
Diameter of Cu laminated wire	0,09	0,08	0,09	0,08	0,09	mm
Q_o	65 (typ.)	50	75	60	75	
Schematic* of windings						
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY	
Resonators						
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	
D (typical value)	4	4	4		6	dB
R_G, R_L	3	3	3		3	kΩ
Bandwidth (−3 dB)	4,2	4,2	4,2		4,5	kHz
S_{9kHz}	24	24	24		38	dB
Filter data						
Z_I	4,8	3,8	4,2		4,8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	
Z_F	0,70	0,67	0,68		0,68	kΩ
Bandwidth (−3 dB)	3,6	3,8	3,6		4,0	kHz
S_{9kHz}	35	31	36		42	dB
S_{18kHz}	52	49	54		64	dB
S_{27kHz}	63	58	66		74	dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding, N2 the outer winding.

AM RECEIVER

GENERAL DESCRIPTION

The TDA1572T integrated AM receiver circuit performs all the active functions and part of the filtering required of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle RF signals up to 500 mV.

RF radiation and sensitivity to interference are minimized by an almost symmetrical design. The controlled-voltage oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range, even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the IF amplifier.

Features

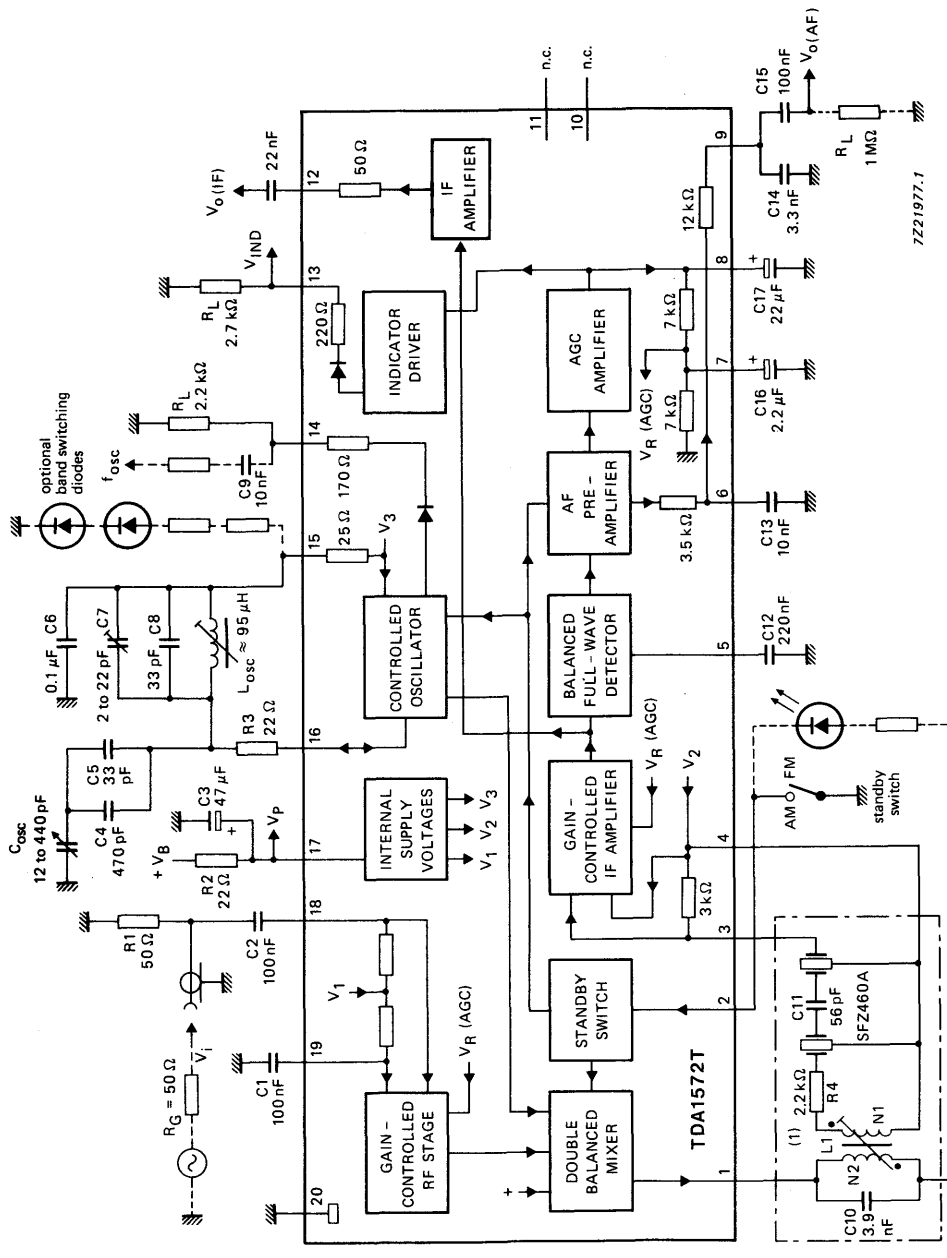
- Inputs protected against damage by static discharge
- Gain-controlled RF stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled IF stage with wide AGC range
- Full-wave, balanced envelope detector
- Internal generation of AGC voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- AF preamplifier with possibilities for simple AF filtering
- Electronic standby switch
- IF output for stereo demodulator and search tuning

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	7.5	8.5	14.0	V
Supply current range	V_P = 8.5 V	I_P	15	25	28	mA
RF input voltage (RMS value)						
for (S + N)/N = 6 dB	m = 30%	$V_{iFR(rms)}$	–	1.5	–	μV
for THD = 3%	m = 80%	$V_{iRF(rms)}$	–	500	–	mV
IF output voltage (RMS value)	V_i = 2 mV(rms)	$V_{oIF(rms)}$	180	230	290	mV
AF output voltage (RMS value)	V_i = 2 mV(rms); f_i = 1 MHz; m = 30%; f_m = 400 Hz	$V_{oAF(rms)}$	240	310	390	mV
AGC range						
Change of V_i for 1 dB change of V_{oAF}		ΔV_i	–	86	–	dB
Indicator driver (pin 13)						
Output voltage	V_i = 500 mV(rms); R_L = 2.7 kΩ	V_o	2.5	2.8	3.1	V

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1 : N1/N2 = 12/32; Q_O = 65; Q_B = 57.
Filter data: Z_F = 700 Ω at R_{3-4} = 3 kΩ; Z_I = 4.8 kΩ.

Fig. 1 Block diagram and test circuits (connections shown in broken lines are not part of the test circuits).

DEVELOPMENT DATA

PINNING

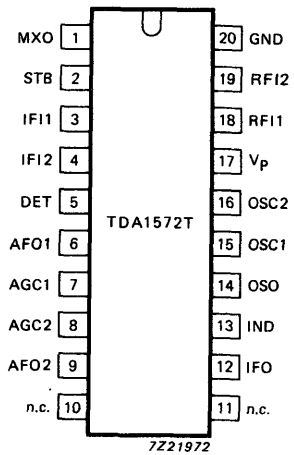


Fig.2 Pinning diagram.

1	MXO	mixer output
2	STB	standby switch
3	IFI1	IF input 1
4	IFI2	IF input 2
5	DET	detector
6	AFO1	AF output 1
7	AGC1	AGC stage 1
8	AGC2	AGC stage 2
9	AFO2	AF output 2
10	n.c.	not connected
11	n.c.	not connected
12	IFO	IF output
13	IND	indicator output
14	OSO	buffered oscillator output
15	OSC1	oscillator 1
16	OSC2	oscillator 2
17	V_P	supply voltage
18	RFI1	RF input 1
19	RFI2	RF input 2
20	GND	ground

FUNCTIONAL DESCRIPTION

Gain-controlled RF stage and mixer

The differential amplifier in the RF stage employs an AGC negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by AGC delays at the various signal stages. Large signals are handled with low distortion and the (S + N)/N ratio of small signals is improved. Low noise working is achieved in the differential amplifier by using transistors with low base resistance.

A double balanced mixer provides the IF output signal to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{15\text{-}20}$. An extra buffered oscillator putput (pin 14) is available for driving a synthesizer. If this is not needed, resistor $R_{L(14)}$ can be omitted.

Gain-controlled IF amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the AGC negative feedback network. The IF output is available at pin 12.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. Residual IF carrier is blocked from the signal path by an internal low-pass filter.

AF preamplifier

This stage preamplifies the audio frequency output signal. The amplifier output has an emitter follower with a series resistor which, together with an external capacitor, yields the required low-pass for AF filtering.

AGC amplifier

The AGC amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the AGC voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives fast AGC settling time which is advantageous for electronic search tuning. The AGC settling time can be further reduced by using capacitors of smaller value in the external filter (C16 and C17). The AGC voltage is fed to the RF and IF stages via suitable AGC delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If the field strength information is not needed, $R_{L(13)}$ can be omitted.

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and AF preamplifier are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 17)	$V_P = V_{17-20}$	–	16	V
Input voltage	$\|V_{18-19}\|$	–	12	V
	$-V_{18-19}$; $-V_{19-20}$	–	0.6	V
	V_{18-19}; V_{19-20}	–	V_P	V
Input current (pins 18 and 20)	$\|I_{18}\|$; $\|I_{20}\|$	–	200	mA
Total power dissipation	P_{tot}	–	500	mW
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	−40	+85	°C
Junction temperature	T_j	–	+125	°C
Electrostatic handling*				
all pins except pins 3, 6, 9, 14	V_{es}	−2000	+2000	V
pins 3, 6, 14	V_{es}	−1500	+2000	V
pin 9	V_{es}	−1000	+2000	V

THERMAL RESISTANCE

From junction to ambient (in free air)

$R_{th\ j\text{-}a\ (max.)} = 95$ K/W

DEVELOPMENT DATA

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor; (5 pulses, both polarities).

CHARACTERISTICS

$V_P = V_{17-20} = 8.5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{IF} = 460$ kHz; measured in test circuit of Fig. 1; all voltages referenced to ground; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 17)	V_P	7.5	8.5	14.0	V
Supply current (pin 17)	I_P	15	25	28	mA
RF stage and mixer (pins 18 and 19)					
DC input voltage	V_I	–	$V_P/2$	–	V
RF input impedance at $V_I < 300\ \mu V$ (rms)	Z_i	–	5.5	–	kΩ
RF input capacitance	C_i	–	25	–	pF
RF input impedance at $V_I > 10$ mV (rms)	Z_i	–	8	–	kΩ
RF input capacitance	C_i	–	22	–	pF
IF output impedance (pin 1)	Z_o	200	–	–	kΩ
IF output capacitance	C_o	–	6	–	pF
Conversion transconductance before start of AGC	I_1/V_i	–	6.5	–	mA/V
Maximum IF output voltage, inductive coupling to pin 1 (peak-to-peak value)	$V_{1-17(p-p)}$	–	5	–	V
DC value of output current; at $V_I = 0$ V (pin 1)	I_O	–	1.2	–	mA
AGC range of input stage		–	30	–	dB
RF signal handling capability					
Input voltage (RMS value) for THD = 3% at m = 80%	$V_{i(rms)}$	–	500	–	mV

parameter	symbol	min.	typ.	max.	unit
Oscillator					
Frequency range	f_{osc}	0.1	–	60	MHz
Voltage amplitude (pins 15 to 16) (RMS value)	$V_{(rms)}$	80	130	150	mV
External load impedance (pins 16 to 15)	$R_{(ext)}$	0.5	–	200	kΩ
External load impedance for no oscillation (pins 16 to 15)	$R_{(ext)}$	–	–	60	Ω
Supply voltage ripple rejection at V_P = 100 mV(rms); f_p = 100 Hz (SVRR = 20 log [V_{17}/V_{15}])	SVRR	–	55	–	dB
Source voltage for switching diodes (6 x V_{BE}) (pin 15)	$V_{15\text{-}20}$	–	4.2	–	V
DC output current (for switching diodes) (pin 15)	$-I_O$	0	–	20	mA
Change of output voltage at ΔI_{15} = 20 mA (switch to maximum load) (pin 15)	ΔV_I	–	0.3	–	V
Buffered oscillator output (pin 14)					
DC output voltage	V_O	–	0.8	–	V
Output signal amplitude (peak-to-peak value)	$V_{o(p\text{-}p)}$	–	320	–	mV
Output impedance	Z_O	–	170	–	Ω
Output current (peak value)	$-I_{O(peak)}$	–	–	3	mA
IF, AGC and AF stages					
DC input voltage (pins 3 and 4)	V_I	–	2.0	–	V
IF input impedance (pins 3 to 4)	Z_i	2.4	3.0	3.9	kΩ
IF input capacitance	C_i	–	7	–	pF
IF input voltage for THD = 3% at m = 80% (pins 3 and 4) (RMS value)	$V_{iIF(rms)}$	–	90	–	mV
IF output impedance (pin 12)	Z_o	–	50	–	Ω
Unloaded IF output voltage at V_i = 10 mV (pin 12) (RMS value)	$V_{oIF(rms)}$	180	230	290	mV
Voltage gain before start of AGC (pins 3 to 4; 6 to 20)	G_v	–	68	–	dB
AGC range of IF stages: change of $V_{3\text{-}4}$ for 1 dB change of $V_{o(AF)}$; $V_{3\text{-}4(ref)}$ = 75 mV(rms)	ΔV_v	–	55	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
IF, AGC and AF stages (continued)					
AF output voltage (RMS value)					
at $V_{3\text{-}4(IF)}$ = 50 μV(rms)	$V_{oAF(rms)}$	–	130	–	mV
at $V_{3\text{-}4(IF)}$ = 1 mV(rms)	$V_{oAF(rms)}$	–	310	–	mV
AF output impedance (pin 6)	$\|Z_o\|$	2.8	3.5	4.2	kΩ
AF output impedance (pin 9)	$\|Z_o\|$	12.4	15.5	18.6	kΩ
Indicator driver (pin 13)					
Output voltage at V_i = 0 mV(rms); R_L = 2.7 kΩ	V_o	–	–	140	mV
Output voltage at V_i = 500 mV(rms); R_L = 2.7 kΩ	V_o	2.5	2.8	3.1	V
Load resistance	R_L	1.5	–	–	kΩ
Output current at V_i = 500 mV(rms)	$-I_o$	–	–	2.0	mA
Output impedance at $-I_o$ = 0.5 mA	Z_o	–	220	–	Ω
Reverse output voltage at AM off	V_o	–	6	–	V
Standby switch					
Switching threshold at; V_P = 7.5 to 14 V; T_{amb} = −40 to +80 °C					
ON-voltage	$V_{2\text{-}20}$	0	–	2.0	V
OFF-voltage	$V_{2\text{-}20}$	3.5	–	20.0	V
ON-current at $V_{2\text{-}20}$ = 0 V	$-I_2$	–	100	200	μA
OFF-current at $V_{2\text{-}20}$ = 14 V	$\|I_2\|$	–	–	10	μA

DEVELOPMENT DATA

OPERATING CHARACTERISTICS

V_P = 8.5 V; f_i = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig.1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
RF sensitivity					
RF input voltage (RMS value)					
for (S + N)/N = 6 dB	$V_{iRF(rms)}$	–	1.5	–	μV
for (S + N)/N = 26 dB	$V_{iRF(rms)}$	–	15	–	μV
for (S + N)/N = 46 dB	$V_{iRF(rms)}$	–	150	–	μV
at start of AGC	$V_{iRF(rms)}$	–	30	–	μV
RF large signal handling					
RF input voltage (RMS value)					
at THD = 3%; m = 80%	$V_{iRF(rms)}$	–	500	–	mV
at THD = 3%; m = 30%	$V_{iRF(rms)}$	–	700	–	mV
at THD = 10%; m = 30%	$V_{iRF(rms)}$	–	900	–	mV
AGC range					
Change of V_i for 1 dB change of V_{oAF}; $V_{i(ref)}$ = 500 mV(rms)	ΔV_i	–	86	–	dB
Change of V_i for 6 dB change of V_{oAF}; $V_{i(ref)}$ = 500 mV(rms)	ΔV_i	–	91	–	dB
Output signal					
(RMS value)					
IF output voltage at V_i = 2 mV(rms)	$V_{oIF(rms)}$	180	230	290	mV
AF output voltage					
at V_i = 4 μV(rms); m = 80%	$V_{oAF(rms)}$	–	130	–	mV
at V_i = 2 mV(rms)	$V_{oAF(rms)}$	240	310	390	mV
Total harmonic distortion					
at V_i = 2 mV(rms); m = 30%	THD	–	0.5	–	%
at V_i = 2 mV(rms); m = 80%	THD	–	1.0	–	%
at V_i = 500 mV(rms); m = 30%	THD	–	1.0	–	%
Signal-to-noise ratio at V_i = 100 mV(rms)	(S + N)/N	–	58	–	dB
Supply voltage ripple rejection at V_i = 2 mV(rms) V_P = 100 mV(rms); f_p = 100 Hz ($SVRR = 20 \log[V_P/V_{oAF}]$)	SVRR	–	38	–	dB
(a) additional AF signal at IF output	SVRR	–	0*	–	dB
(b) add modulation at IF output (m_{ref} = 30%)	SVRR	–	40	–	dB

* AF signals at the IF output will be suppressed by a coupling capacitor to the demodulator and by full wave-detection in the demodulator.

OPERATING CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Unwanted signals					
Suppression of IF whistles at V_i = 15 μV; m = 0% related to AF signal of m = 30%					
at $f_i \approx 2 \times f_{IF}$	α_{2IF}	–	37	–	dB
at $f_i \approx 3 \times f_{IF}$	α_{3IF}	–	44	–	dB
IF suppression at RF input;					
for symmetrical input	α_{IF}	–	40	–	dB
for asymmetrical input	α_{IF}	–	40	–	dB
Residual oscillator signal at mixer output;					
at f_{osc}	$I_{1(osc)}$	–	1	–	μA
at 2 x f_{osc}	$I_{1(2osc)}$	–	1.1	–	μA

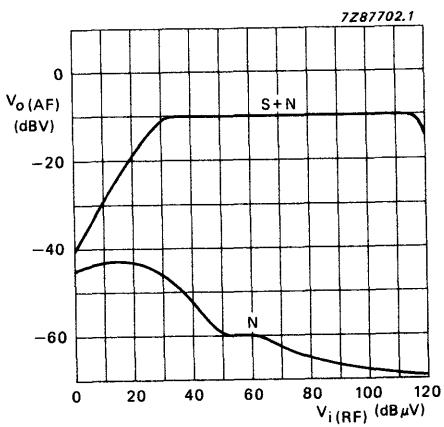


Fig. 3 AF output as a function of RF input in the circuit of Fig. 1; f_i = 1 MHz; f_m = 400 Hz; m = 30%.

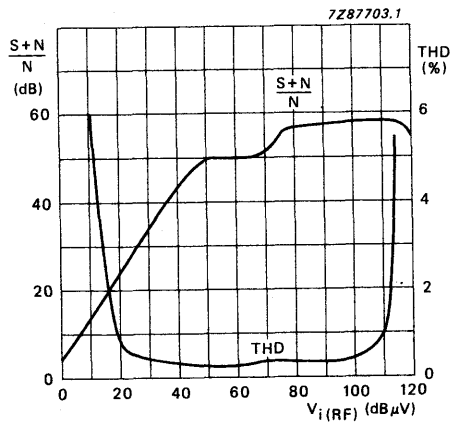


Fig. 4 Total harmonic distortion and (S + N)/N as functions of RF input in the circuit of Fig. 1; m = 30% for (S + N)/N curve and m = 80% for THD curve.

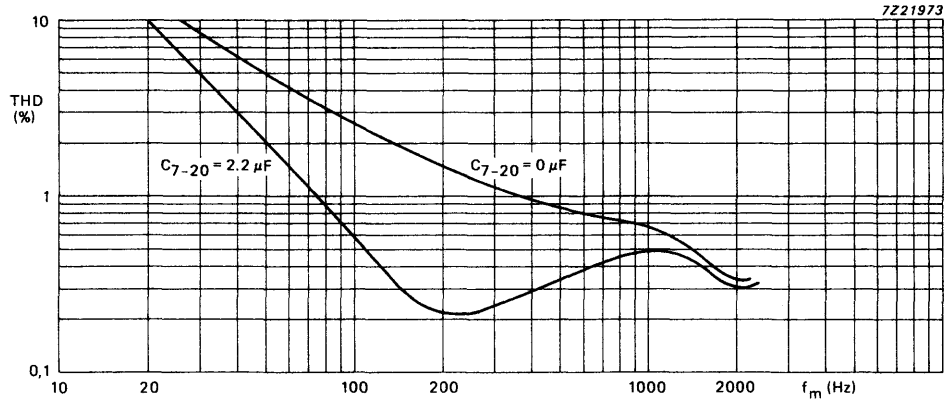


Fig. 5 Total harmonic distortion as a function of modulation frequency at V_i = 5 mV; m = 80%; measured in the circuit of Fig. 1 with $C_{7-20(ext)}$ = 0 μF and 2.2 μF.

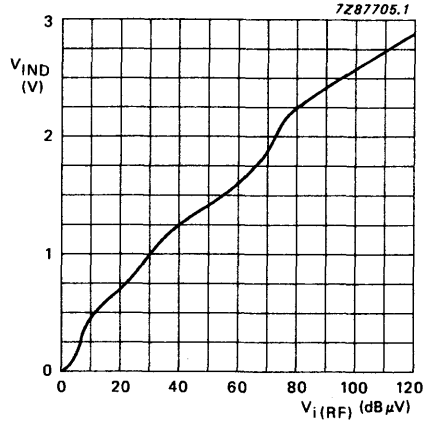
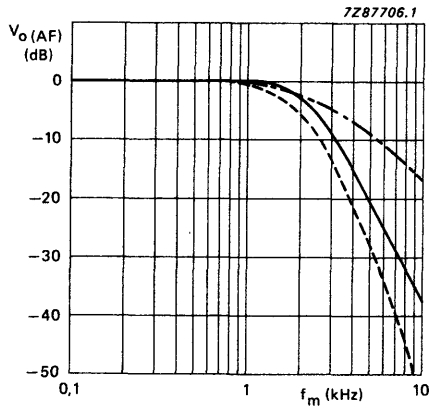


Fig. 6 Indicator driver voltage as a function of RF input in the circuit of Fig. 1.



——— with IF filter;
—·—·— with AF filter;
– – – – – – with IF and AF filters.

Fig.7 Typical frequency response curves from Fig.1 showing the effect of filtering.

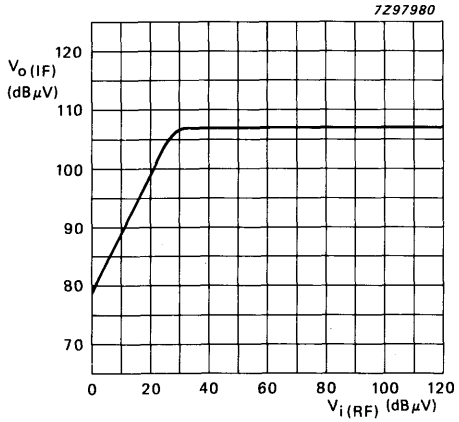


Fig.8 IF output voltage as a function of RF input in the circuit of Fig.1; f_i = 1 MHz.

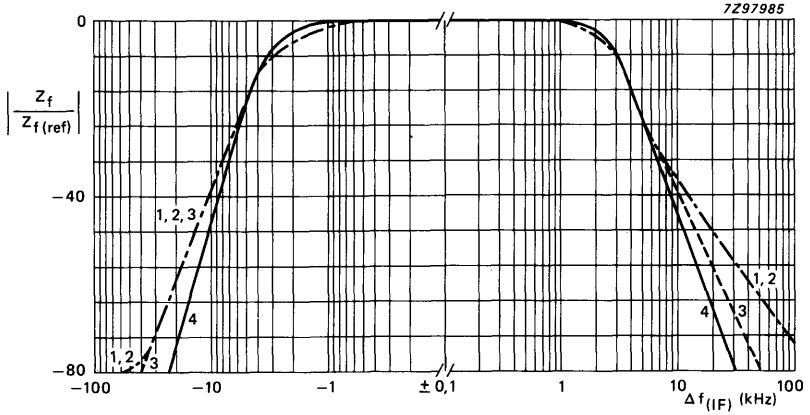


Fig.9 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig.10; centre frequency = 455 kHz.

APPLICATION INFORMATION

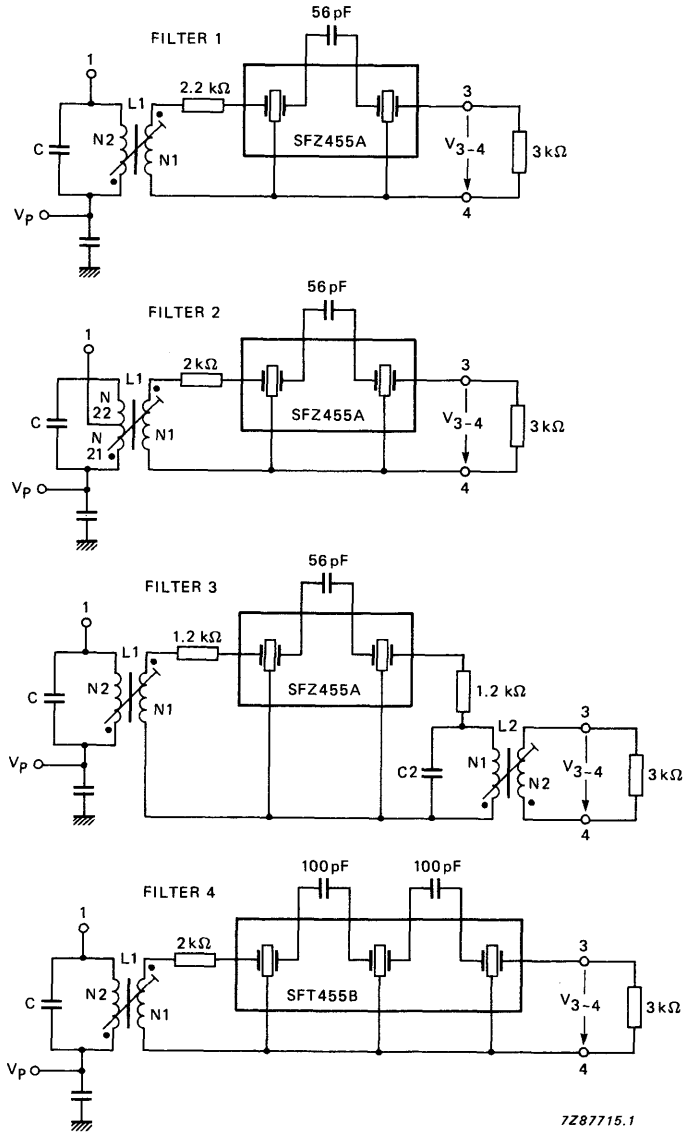


Fig. 10 IF filter variants applied to the circuit of Fig. 1. For filter data, refer to Table 1.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

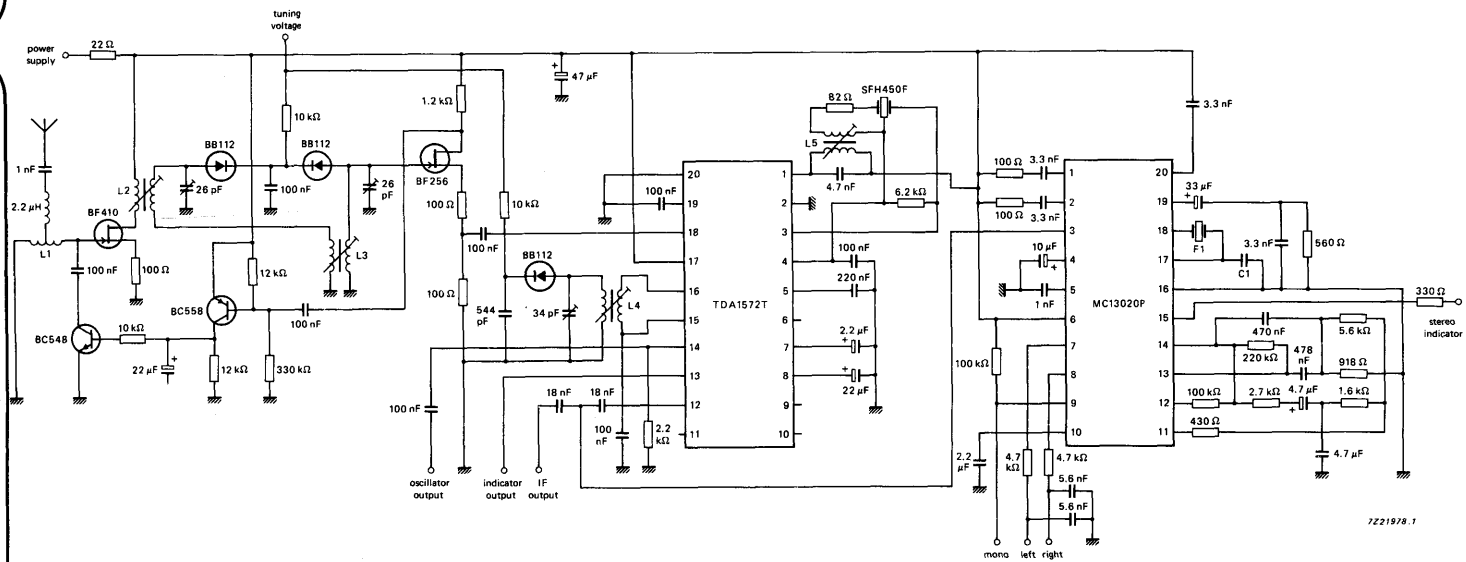


Fig.11 Application diagram.

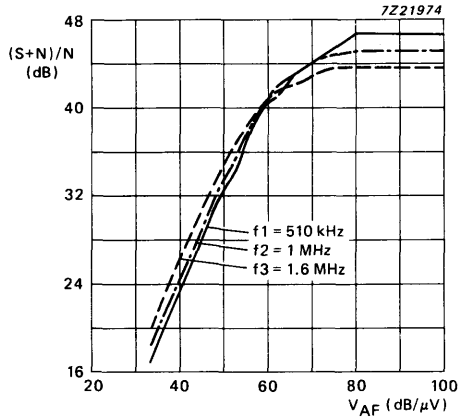


Fig.12 (S + N)/N as a function of input voltage; measured in the circuit of Fig.11 for AM stereo.

DEVELOPMENT DATA

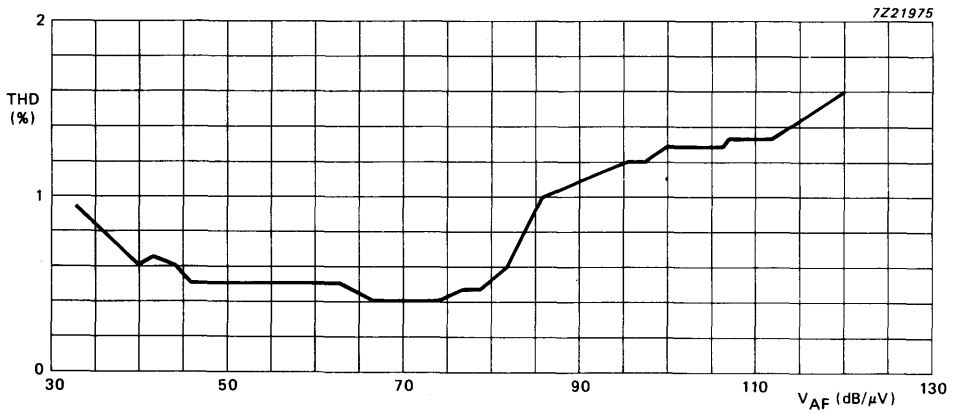
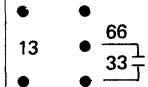


Fig.13 Total harmonic distortion (THD) as a function of input voltage; measured in the circuit of Fig.11 for AM stereo.

filter no.	1	2	3		4	5	unit
Coil data	L1	L1	L1	L2	L1	L1	
Value of C	3900	430	3900	4700	3900	4700	pF
N1 : N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	26 : 32	
Diameter of CU laminated wire	0.09	0.08	0.09	0.08	0.09	0.07	mm
Q_o	65 (typ.)	50	75	60	75	50	
Schematic* of windings							
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY		
Resonators							
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	SFH450F	
D (typical value)	4	4	4		6	6	dB
R_G, R_L	3	3	3		3	2	kΩ
Bandwidth (−3 dB)	4.2	4.2	4.2		4.5	10	kHz
S_{9kHz}	24	24	24		38		dB
Filter data							
Z_I	4.8	3.8	4.2		4.8	1.8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	20	
Z_F	0.70	0.67	0.68		0.68	0.70	kΩ
Bandwidth (−3 dB)	3.6	3.8	3.6		4.0	10	kHz
S_{9kHz}	35	31	36		42		dB
S_{18kHz}	52	49	54		64		dB
S_{27kHz}	63	58	66		74		dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding, N2 the outer winding.

Table 1 Data for IF filters shown in Fig.10 (Filter 1 to 4) and Fig.11 (Filter 5). Criteria for adjustment is IF = maximum (optimum selectivity curve at centre frequency f_0 = 455 kHz). Filter 5 is used for AM stereo application with centre frequency f_0 = 450 kHz.

INTEGRATED FM TUNER FOR RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1574 is a monolithic integrated FM tuner circuit designed for use in the r.f./i.f. section of car radios and home-receivers. The circuit comprises a mixer, oscillator and a linear i.f. amplifier for signal processing, plus the following additional features.

Features

- Keyed automatic gain control (a.g.c.)
- Regulated reference voltage
- Buffered oscillator output
- Electronic standby switch
- Internal buffered mixer driving

QUICK REFERENCE DATA

Supply voltage range (pin 15)	V_P		7 to 16 V
Mixer input bias voltage (pins 1 and 2)	$V_{1,2-4}$	typ.	1 V
noise figure	NF	typ.	9 dB
Oscillator output voltage (pin 6)	V_{6-4}	typ.	2 V
output admittance at pin 6 for f = 108,7 MHz	Y22	typ.	1,5 + j2 mS
Oscillator output buffer			
D.C. output voltage (pin 9)	V_{9-4}	typ.	6 V
Total harmonic distortion	THD	typ.	−15 dBC
Linear i.f. amplifier output voltage (pin 10)	V_{10-4}	typ.	4,5 V
noise figure at R_S = 300 Ω	NF	typ.	6,5 dB
Keyed a.g.c. output voltage range (pin 18)	V_{18-4}	+ 0,5 to V_P−0,3	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

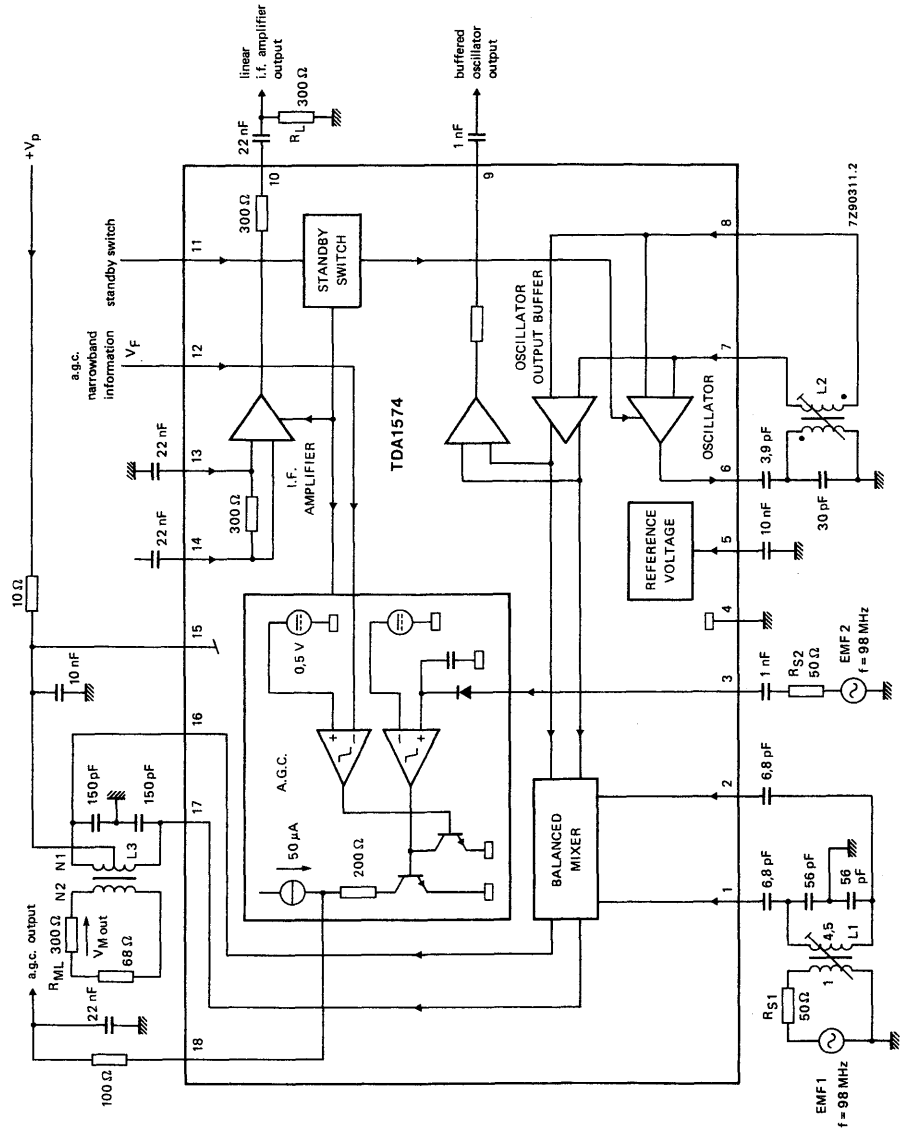


Fig. 1 Block diagram and test circuit.

Coil data

L1: TOKO MC-108, 514HNE-1500145 14; L = 0,078 µH
L2: TOKO MC-111, E516HNS-200057; L = 0,08 µH
L3: TOKO coil set 7P, N1 = 5,5 + 5,5 turns, N2 = 4 turns

FUNCTIONAL DESCRIPTION

Mixer

The mixer circuit is a double balanced multiplier with a preamplifier (common base input) to obtain a large signal handling range and a low oscillator radiation.

Oscillator

The oscillator circuit is an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tanh-transfer-function to obtain low order 2nd harmonics.

Linear IF amplifier

The IF amplifier is a one stage, differential input, wideband amplifier with an output buffer.

Keyed AGC

The AGC processor combines narrow- and wideband information via an RF level detector, a comparator and an ANDing stage. The level dependent, current sinking output has an active load, which sets the AGC threshold.
The AGC function can either be controlled by a combination of wideband and narrowband information (keyed AGC), or by a wideband information only, or by narrowband information only. If only narrowband AGC is wanted pin 3 should be connected to pin 5. If only wideband AGC is wanted pin 12 should be connected to pin 13.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_P = V_{15-4}$	max.	18	V
Mixer output voltage (pins 16 and 17)	$V_{16,\ 17-4}$	max.	35	V
Standby switch input voltage (pin 11)	V_{11-4}	max.	23	V
Reference voltage (pin 5)	V_{5-4}	max.	7	V
Field strength input voltage (pin 12)	V_{12-4}	max.	7	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−40 to +	85	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}amb}$	=	80	K/W

Note

All pins are short-circuit protected to ground.

CHARACTERISTICS

$V_P = V_{15-4} = 8{,}5$ V; $T_{amb} = 25$ °C; measured in test circuit Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 15)					
Supply voltage	$V_P = V_{15-4}$	7	–	16	V
Supply current (except mixer)	$I_P = I_{15}$	16	23	30	mA
Reference voltage (pin 5)	V_{5-4}	3,9	4,1	4,4	V
Mixer					
D.C. characteristics					
Input bias voltage (pins 1 and 2)	$V_{1,2-4}$	–	1	–	V
Output voltage (pins 16 and 17)	$V_{16,17-4}$	4	–	35	V
Output current (pin 16 + pin 17)	$I_{16} + I_{17}$	–	4,0	–	mA
A.C. characteristics (f_i = 98 MHz)					
Noise figure	NF	–	9	–	dB
Noise figure including transforming network	NF	–	11	–	dB
3rd order intercept point	$EMF1_{IP3}$	–	115	–	dBμV
Conversion power gain					
$10 \log \frac{4\ (V_{M(out)}\ 10{,}7\ MHz)^2}{(EMF1\ 98\ MHz)^2} \times \frac{R_{S1}}{R_{ML}}$	G_P	–	14	–	dB
Input resistance (pins 1 and 2)	$R_{1,2-4}$	–	14	–	Ω
Output capacitance (pins 16 and 17)	$C_{16,17}$	–	13	–	pF
Oscillator					
D.C. characteristics					
Input voltage (pins 7 and 8)	$V_{7,8-4}$	–	1,3	–	V
Output voltage (pin 6)	V_{6-4}	–	2	–	V
A.C. characteristics (f_{osc} = 108,7 MHz)					
Residual FM (Bandwidth 300 Hz to 15 kHz); de-emphasis = 50 μs	Δf	–	2,2	–	Hz

parameter	symbol	min.	typ.	max.	unit
Linear i.f. amplifier					
D.C. characteristics					
Input bias voltage (pin 13)	V_{13-4}	–	1,2	–	V
Output voltage (pin 10)	V_{10-4}	–	4,5	–	V
A.C. characteristics (f_i = 10,7 MHz)					
Input impedance					
	R_{14-13}	240	300	360	Ω
	C_{14-13}	–	13	–	pF
Output impedance					
	R_{10-4}	240	300	360	Ω
	C_{10-4}	–	3	–	pF
Voltage gain					
$20 \log \frac{V_{10-4}}{V_{14-13}}$	G_{VIF}	27	30	–	dB
T_{amb} = −40 to + 85 °C	ΔG_{VIF}	–	0	–	dB
1 dB compression point (r.m.s. value)					
at V_P = 8,5 V	$V_{10-4rms}$	–	750	–	mV
at V_P = 7,5 V	$V_{10-4rms}$	–	550	–	mV
Noise figure					
at R_S = 300 Ω	NF	–	6,5	–	dB
Keyed a.g.c.					
D.C. characteristics					
Output voltage range (pin 18)	V_{18-4}	0,5	–	V_P−0,3	V
A.G.C. output current					
at I_3 = ϕ or					
V_{12-4} = 450 mV; $V_{18-4} = V_P/2$	$-I_{18}$	25	50	100	μA
at V_{3-4} = 2 V and					
V_{12-4} = 1 V; $V_{18-4} = V_{15-4}$	I_{18}	2	–	5	mA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Narrowband threshold					
at V_{3-4} = 2 V; V_{12-4} = 550 mV	V_{18-4}	–	–	1	V
at V_{3-4} = 2 V; V_{12-4} = 450 mV	V_{18-4}	V_P–0,3	–	–	V
A.C. characteristics (f_i = 98 MHz)					
Input impedance					
	R_{3-4}	–	4	–	kΩ
	C_{3-4}	–	3	–	pF
Wideband threshold (r.m.s. value) (see figures 2, 3, 4 and 5)					
at V_{12-4} = 0,7 V; $V_{18-4} = V_P/2$; I_{18} = 0	$EMF2_{rms}$	–	17	–	mV
Oscillator output buffer (pin 9)					
D.C. output voltage	V_{9-4}	–	6,0	–	V
Oscillator output voltage (r.m.s. value)					
at $R_L = \infty$; C_L = 2 pF	$V_{9-4(rms)}$	–	110	–	mV
at R_L = 75 Ω	$V_{9-4(rms)}$	30	50	–	mV
D.C. output impedance	R_{9-15}	–	2,5	–	kΩ
Signal purity					
Total harmonic distortion	THD	–	–15	–	dBC
Spurious frequencies					
at EMF1 = 0,2 V; R_{S1} = 50 Ω	f_S	–	–35	–	dBC
Electronic standby switch (pin 11)					
Oscillator; linear i.f. amplifier; a.g.c.					
at T_{amb} = –40 to + 85 °C					
Input switching voltage					
for threshold ON; $V_{18-4} = \geqslant V_P$–3 V	V_{11-4}	0	–	2,3	V
for threshold OFF; $V_{18-4} = \leqslant$ 0,5 V	V_{11-4}	3,3	–	23	V
Input current					
at ON condition; V_{11-4} = 0 V	$-I_{11}$	–	–	150	μA
at OFF condition; V_{11-4} = 23 V	I_{11}	–	–	10	μA
Input voltage					
at $I_{11} = \phi$	V_{11-4}	–	–	4,4	V

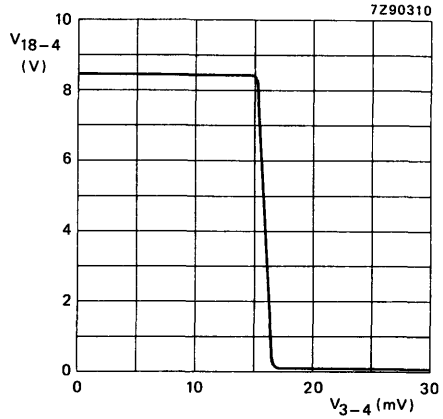


Fig. 2 Keyed a.g.c. output voltage V_{18-4} as a function of r.m.s. input voltage V_{3-4}. Measured in test circuit Fig. 1 at $V_{12-4} = 0{,}7$ V; $I_{18} = \phi$.

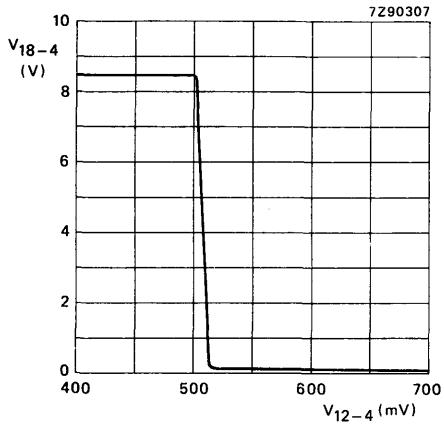


Fig. 3 Keyed a.g.c. output voltage V_{18-4} as a function of input voltage V_{12-4}. Measured in test circuit Fig. 1 at $V_{3-4} = 2$ V; $I_{18} = \phi$.

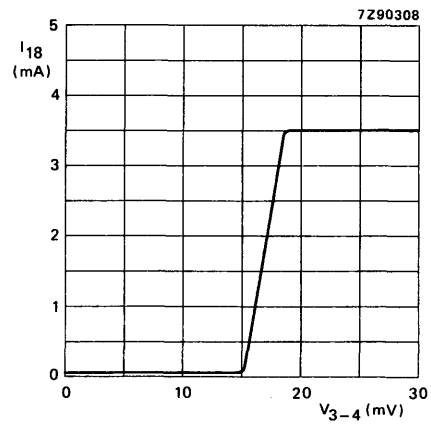


Fig. 4 Keyed a.g.c. output current I_{18} as a function of r.m.s. input voltage V_{3-4}. Measured in test circuit Fig. 1 at $V_{12-4} = 0{,}7$ V; $V_{18-4} = 8{,}5$ V.

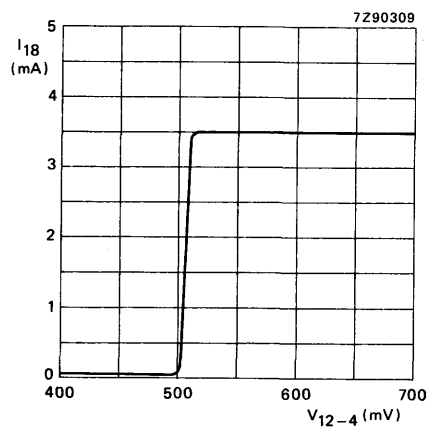


Fig. 5 Keyed a.g.c. output current I_{18} as a function of input voltage V_{12-4}. Measured in test circuit Fig. 1 at $V_{3-4} = 2$ V; $V_{18-4} = 8{,}5$ V.

APPLICATION INFORMATION

Coil data

L1: TOKO MC-108,
514HNE-15023S15,
N1 = 5,5 turns, N2 = 1 turn

L2:
L3: see Fig. 1

(1) Field strength indication of main i.f. amplifier.

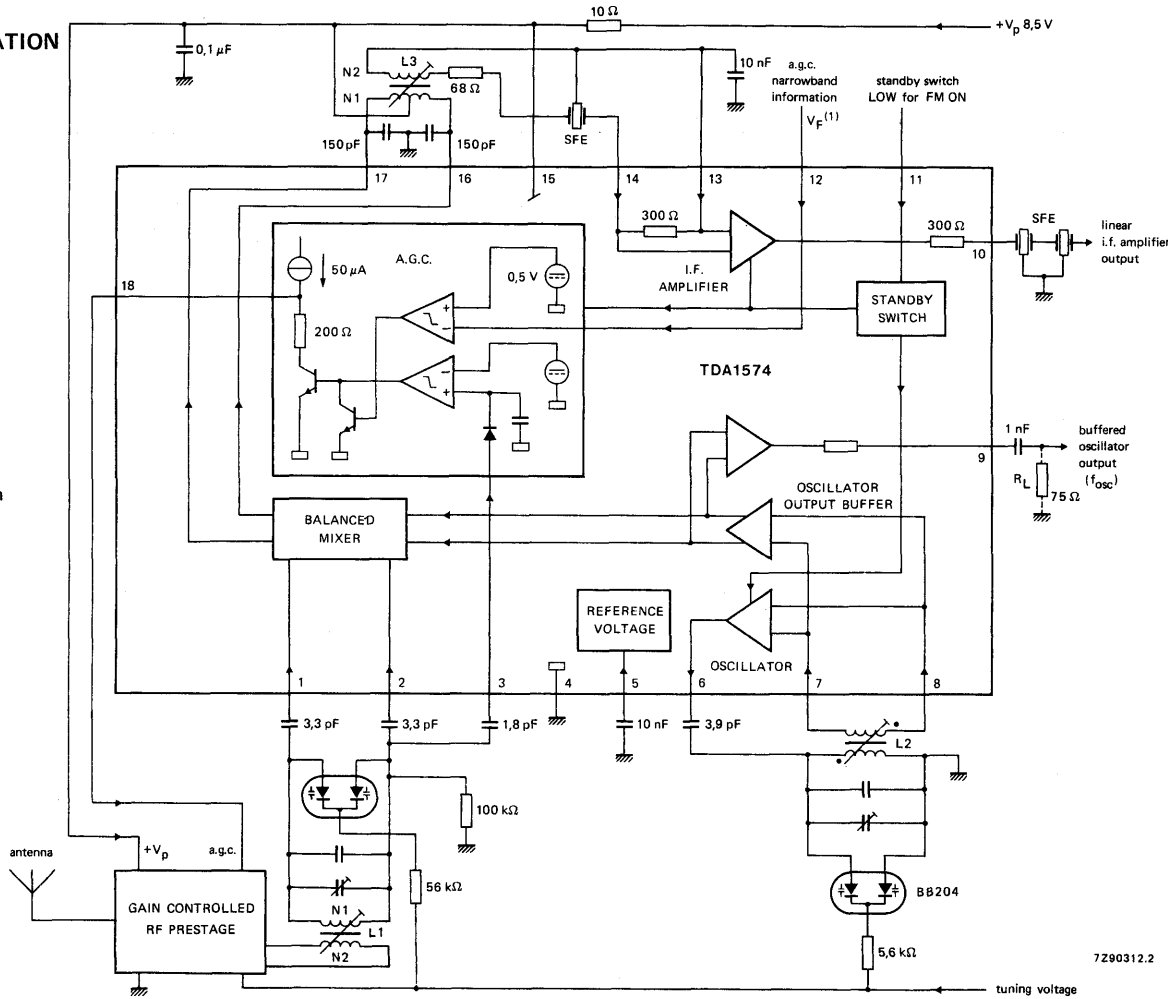


Fig. 6 TDA1574 application diagram.

INTEGRATED FM TUNER FOR RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1574T is an integrated FM tuner circuit designed for use in the RF/IF section of car radios and home-receivers. The circuit contains a mixer and an oscillator and a linear IF amplifier for signal processing. The circuit also incorporates the following features.

Features

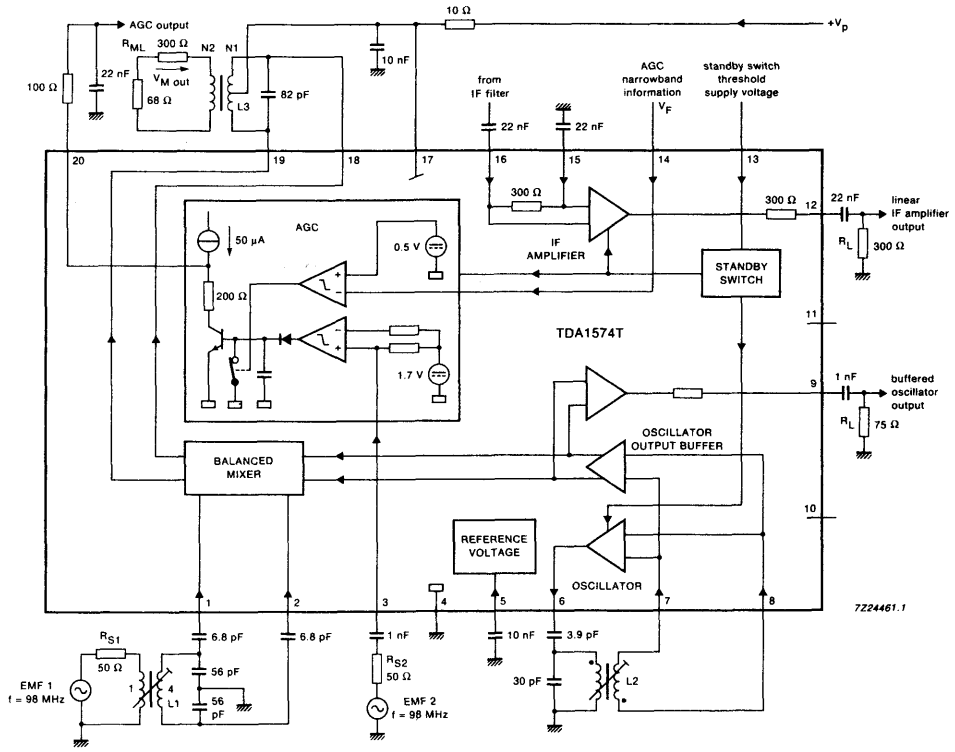
- Keyed Automatic Gain Control (AGC)
- Regulated reference voltage
- Buffered oscillator output
- Electronic standby switch
- Internal buffered mixer driving

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 17)		V_P	7	–	14	V
Mixer input bias voltage (pins 1 and 2)		$V_{1,2-4}$	–	1	–	V
Noise factor		NF	–	9	–	dB
Oscillator output voltage (pin 6)		V_{6-4}	–	2	–	V
Output admittance at pin 6	f = 108.7 MHz	Y22	–	1.5 + j2		ms
Oscillator output buffer DC output voltage (pin 9)		V_{9-4}	–	6	–	V
Total harmonic distortion		THD	–	–15	–	dB
Linear IF amplifier output voltage (pin 12)		V_{12-4}	–	4.5	–	V
Noise factor	R_S = 300 Ω	NF	–	6.5	–	dB
Keyed AGC output voltage range (pin 20)		V_{20-4}	0.5	–	V_P–0.3	V

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).



Coil data

L1: TOKO MC-108, 514HNE-150023S14; L = 0.078 μH
L2: TOKO MC-111, E516HNS-200057; L = 0.08 μH
L3: TOKO Coil set 7P, N1 = 5.5 + 5.5 turns, N2 = 4 turns

Fig.1 Block diagram and test circuit.

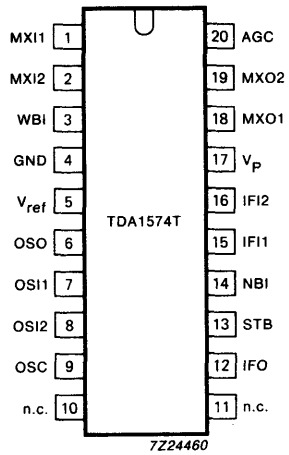


Fig.2 Pinning diagram.

PINNING

1. Mixer input 1
2. Mixer input 2
3. Wideband information input
4. Ground
5. Voltage reference
6. Oscillator output
7. Oscillator input 1
8. Oscillator input 2
9. Buffered oscillator output
10. Not connected
11. Not connected
12. IF output
13. Standby switch
14. Narrowband information input
15. IF input 1
16. IF input 2
17. Supply voltage
18. Mixer output 1
19. Mixer output 2
20. AGC output

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Mixer

The mixer circuit uses a double balanced multiplier with a preamplifier (common base input) in order to obtain a large signal handling range and low oscillator radiation.

Oscillator

The oscillator circuit uses an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tan h-transfer-function to obtain low order 2nd harmonics.

Linear IF amplifier

The IF amplifier is a one stage, differential input, wideband amplifier with an output buffer.

Keyed AGC

The AGC processor combines narrow and wideband information via an RF level detector, a comparator and an ANDing stage. The level dependent current sinking output has an active load which sets the AGC threshold.

The AGC function can either be controlled by a combination of wideband and narrowband information (keyed AGC) or by a wideband/narrowband information only. If narrowband AGC is required pin 3 should be connected to pin 5. If wideband AGC is required pin 14 should be connected to pin 15.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 17)		V_{17-4}	–	14	V
Mixer output voltage (pins 18 and 19)		$V_{18,19-4}$	–	35	V
Standby switch input voltage (pin 13)		V_{13-4}	–	23	V
Reference voltage (pin 5)		V_{5-4}	–	7	V
Total power dissipation		P_{tot}	–	500	mW
Storage temperature range		T_{stg}	–55	+ 150	°C
Operating ambient temperature range		T_{amb}	–40	+ 85	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\,j-a}$ = 95 K/W

Note to the ratings

All pins are short-circuit protected to ground.

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{17-4} = 8.5$ V; $T_{amb} = 25$ °C; measured in test circuit Fig.1;
All measurements are with respect to ground (pin 4); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 17)						
Supply voltage	$V_P = V_{17}$	V_{17}	7	–	14	V
Supply current (except mixer)	$I_P = I_{17}$	I_{17}	16	23	30	mA
Reference voltage (pin 5)		V_5	4.0	4.2	4.4	V
Mixer						
DC characteristics						
Input bias voltage (pins 1 and 2)		$V_{1,2}$	–	1	–	V
Output voltage (pins 18 and 19)		$V_{18,19}$	4	–	35	V
Output current (pins 18 and 19)		I_{18+19}	–	4.5	–	mA
AC characteristics	$f_i = 98$ MHz					
Noise figure		NF	–	9	–	dB
Noise figure including transforming network		NF	–	11	–	dB
3rd order intercept point		$EMF1_{IP3}$	–	115	–	dB/μV
Conversion power gain	note 1	G_{CP}	–	14	–	dB
Input resistance (pins 1 and 2)		$R_{1,2}$	–	14	–	Ω
Output capacitance (pins 18 and 19)		$C_{18,19}$	–	13	–	pF
Oscillator						
DC characteristics						
Input voltage (pins 7 and 8)		$V_{7,8}$	–	1.3	–	V
Output voltage (pin 6)		V_6	–	2	–	V
AC characteristics						
Residual FM (bandwidth = 300 Hz to 15 kHz)	de-emphasis = 50 μs	Δf	–	2.2	–	Hz
Linear IF amplifier						
DC characteristics						
Input bias voltage (pin 15)		V_{15}	–	1.2	–	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage (pin 12)		V_{12}	–	4.5	–	V
AC characteristics	f_i = 10.7 MHz					
Input impedance		$R_{16\text{-}15}$	240	300	360	Ω
		$C_{16\text{-}15}$	–	13	–	pF
Output impedance		R_{12}	240	300	360	Ω
		C_{12}	–	3	–	pF
Voltage gain	note 2	G_v	27	30	–	dB
Voltage gain with variation of temperature	T_{amb} = –40 to + 85 °C	ΔG_T	–	0	–	dB
1 dB compression point (RMS value)						
at V_P = 8.5 V		$V_{12(rms)}$	–	750	–	mV
at V_P = 7.5 V		$V_{12(rms)}$	–	550	–	mV
Signal-to-noise ratio	R_S = 300 Ω	S/N	–	6.5	–	dB
Keyed AGC						
DC characteristics						
Output voltage range (pin 20)		ΔV_{20}	0.5	–	V_P–0.3	V
AGC output current at I_3 = 0 or V_{14} = 450 mV; V_{20} = V_P/2		$-I_{20}$	25	50	100	μA
at V_3 = 2 V and V_{14} = 1 V; V_{20} = V_{15}		I_{20}	2	–	5	mA
Narrowband threshold						
at V_3 = 2 V; V_{14} = 550 mV		V_{20}	–	–	1	V
at V_3 = 2 V; V_{14} = 450 mV		V_{20}	V_P–0.3	–	–	V
AC characteristics	f_i = 98 MHz					
Input impedance		R_3	–	4	–	kΩ
		C_3	–	3	–	pF

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Wideband threshold (RMS value) (see Figs 3, 4, 5 and 6) at V_{14} = 0.7 V; $V_{20} = V_P/2$; $I_{20} = 0$		$EMF_{2(rms)}$	–	17	–	mV
Oscillator output buffer (pin 9)						
DC output voltage		V_9	–	6	–	V
Oscillator output voltage (RMS value)						
at R_L = oo; C_L = 2 pF		$V_{9(rms)}$	–	110	–	mV
at R_L = 75 Ω		$V_{9(rms)}$	30	50	–	mV
DC output resistance		R_{9-17}	–	2.5	–	kΩ
Signal purity						
Total harmonic distortion		THD	–	–15	–	dB
Spurious frequencies at EMF1 = 1 V; R_{S1} = 50 Ω		f_S	–	–35	–	dB
Electronic standby switch (pin 11)						
Oscillator; linear IF amplifier; AGC	T_{amb} = –40 to + 85 °C					
Input switching voltage						
for threshold ON	$V_{20} = > V_P - 3$ V	V_{13}	0	–	2.3	V
for threshold OFF	$V_{20} = < 0.5$ V	V_{13}	3.3	–	23	V
Input current						
at ON condition	V_{13} = 0 V	$-I_{13}$	–	–	150	μA
at OFF condition	V_{13} = 23 V	$-I_{13}$	–	–	10	μA
Input voltage	$I_{13} = 0$	V_{13}	–	–	4.4	V

Notes to the characteristics

1. Power gain conversion is equated by the following equation:

$$10 \log \frac{4\,(V_{M(out)}\ 10.7\ MHz)^2}{(EMF1\ 98\ MHz)^2} \times \frac{R_{S1}}{R_{ML}}$$

2. Voltage gain is equated by the following equation:

$$20 \log \frac{V_{12}}{V_{16\text{-}15}}$$

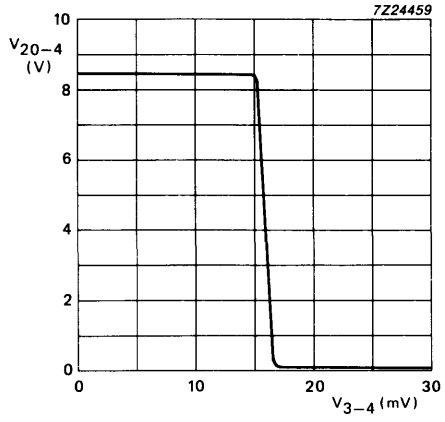


Fig.3 Keyed AGC output voltage V_{20} as a function of RMS input voltage V_3. Measured in test circuit Fig.1 at V_{14} = 0.7 V; I_{20} = 0.

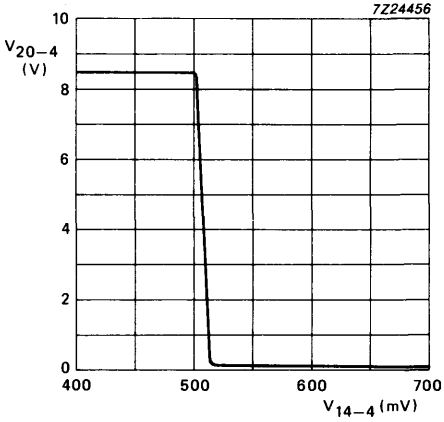


Fig.4 Keyed AGC output voltage V_{20} as a function of input voltage V_{14}. Measured in test circuit Fig.1 at V_3 = 2 V; I_{20} = 0.

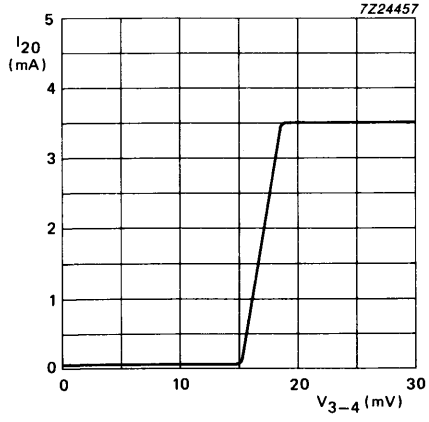


Fig.5 Keyed AGC output current I_{20} as a function of RMS input voltage V_3. Measured in test circuit Fig.1 at V_{14} = 0.7 V; V_{20} = 8.5 V.

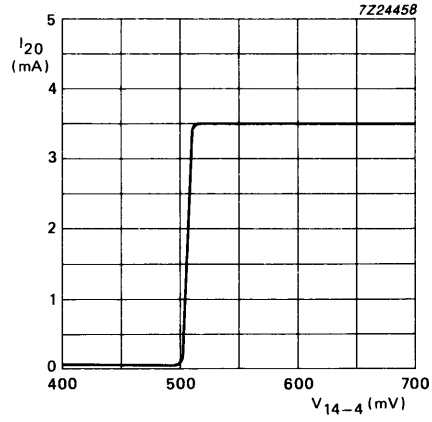
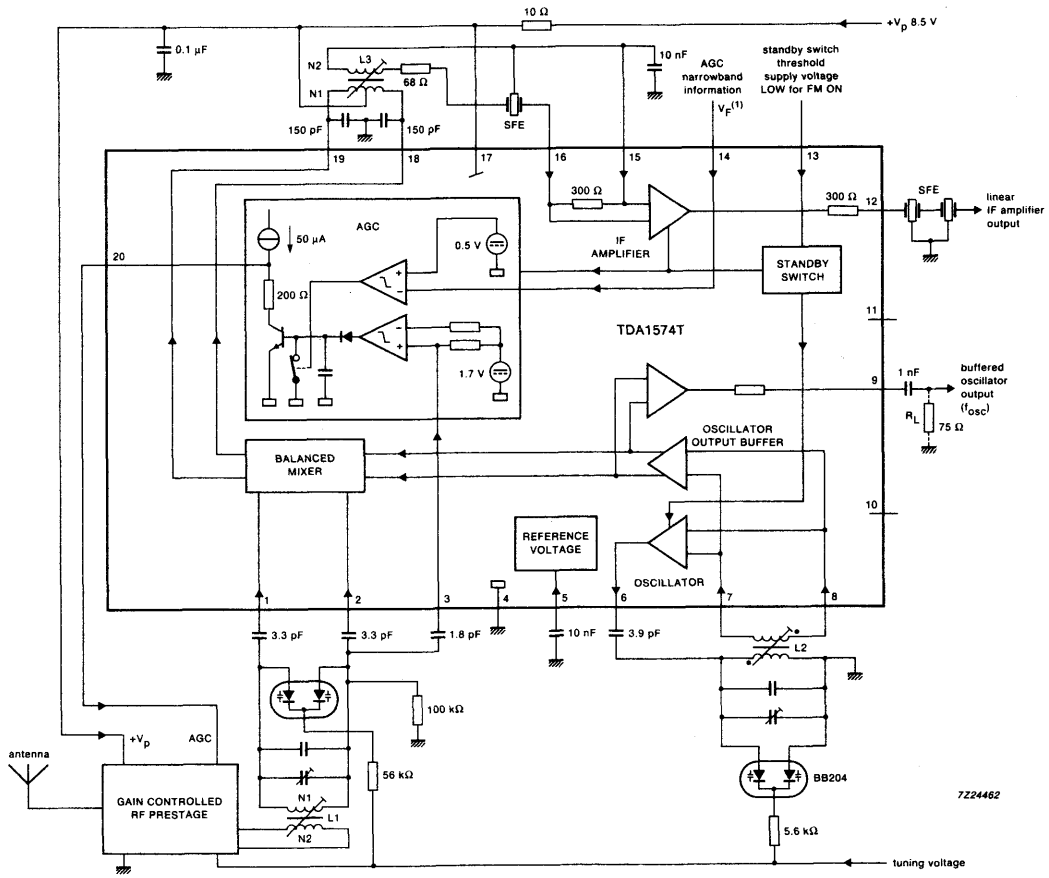


Fig.6 Keyed AGC output voltage I_{20} as a function of input voltage V_{14}. Measured in test circuit Fig.1 at V_3 = 2 V; V_{20} = 8.5 V.

DEVELOPMENT DATA



Coil data

L1: TOKO MC-108, N1 = 5.5 turns, N2 = 1 turn

L2: } see Fig.1
L3: }

(1) Field strength indication of main IF amplifier.

Fig.7 TDA1574T application diagram.

FM/IF AMPLIFIER CIRCUIT

The TDA1576 is a monolithic integrated f.m./i.f. amplifier circuit provided with the following functions:

- symmetrical limiting i.f. amplifier
- symmetrical quadrature demodulator
- internal muting circuit
- symmetrical a.f.c. output
- field-strength indication output
- detune-detector
- reference voltage output
- electronic smoothing of the supply voltage
- standby on/off switching circuit.

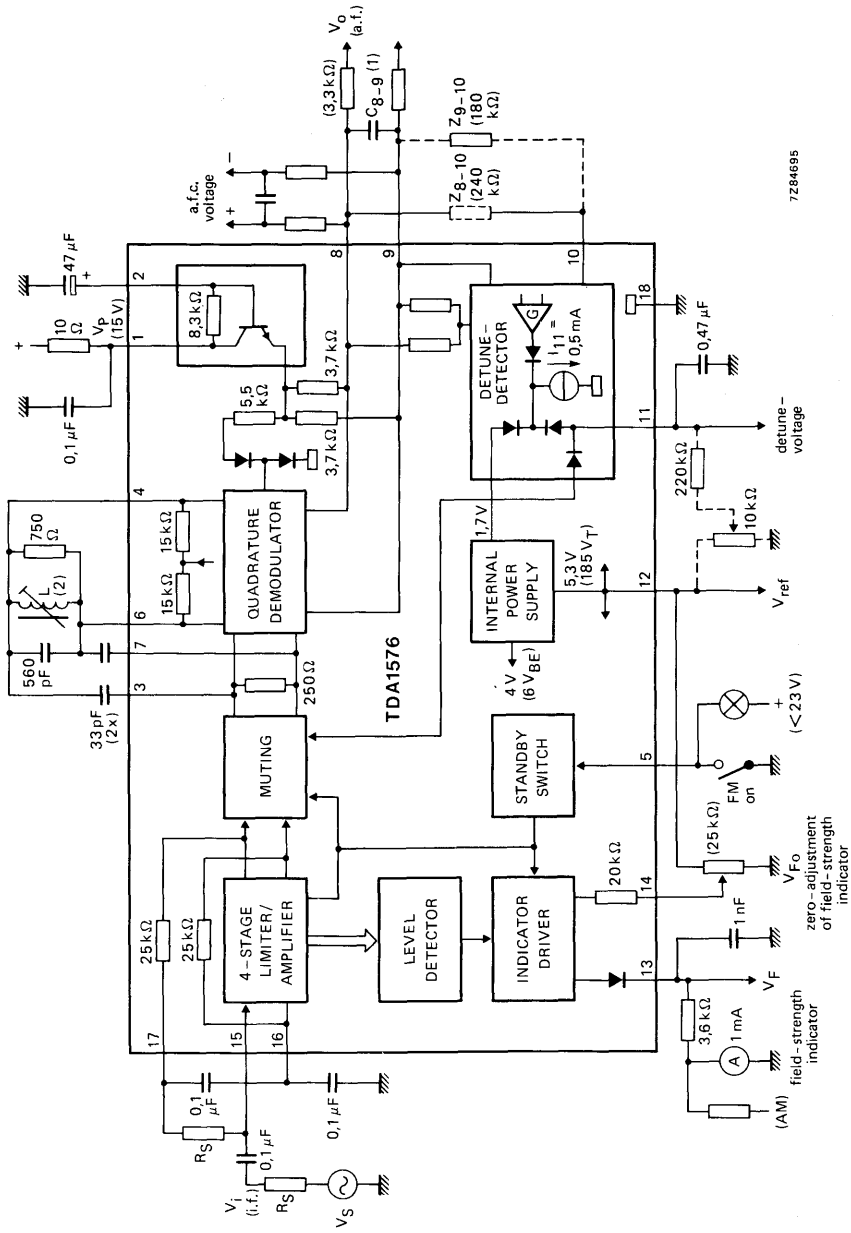
QUICK REFERENCE DATA

f_o = 10,7 MHz; $\Delta f = \pm$ 22,5 kHz; f_m = 400 Hz; Q_L = 20; de-emphasis τ = 50 μs

Supply voltages (pin 1)	V_P		8,5	15	V
Supply current	I_P	typ.	16	18	mA
Sensitivity at −3 dB before limiting	V_i	typ.	22		μV
I.F. sensitivity for					
S + N/N = 26 dB	V_i	typ.	8		μV
S + N/N = 46 dB	V_i	typ.	35		μV
A.F. output voltage	V_o	typ.	67	135	mV
Total distortion					
single tuned circuit	d_{tot}	typ.	0,1		%
two tuned circuits	d_{tot}	typ.	0,02		%
Signal plus noise-to-noise ratio; $V_i > 1$ mV	S + N/N	typ.	76	80	dB
A.M. rejection	α	typ.	50		dB
A.F.C. offset drift	$\pm \Delta f$	typ.	3		kHz
		<	6		kHz
Field-strength indication range	ΔV_i	typ.	90		dB
Permissible indicator (load) current	I_L	<	2		mA
Supply voltage range (pin 1)	V_P		7,5 to 20		V
Ambient temperature range	T_{amb}		−30 to +80		°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) For de-emphasis $\tau = 50\ \mu s$: $C_{8\text{-}9} = 6{,}8$ nF.
For stereo operation: $C_{8\text{-}9} = 56$ pF.

(2) L = 0,38 μH; $Q_O = 70$; $Q_L = 20$; adjusted to minimum 2nd harmonic distortion (d_2); at $V_i = 1$ mV; coil: 6 turns CuL (0,25 mm) on coil former KAN (C).

Fig. 1 Block diagram and test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-18}$	max.	23	V
Voltages				
at pin 2	V_{2-18}	max.	V_P	V
	$-V_{2-18}$	max.	0	V
at pin 5	V_{5-18}	max.	23	V
	$-V_{5-18}$	max.	0	V
at pin 12	V_{12-18}	max.	7	V
	$-V_{12-18}$	max.	0	V
at pin 13	V_{13-18}	max.	6	V
at pin 14	V_{14-18}	max.	23	V
	$-V_{14-18}$	max.	0	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr-a}$	=	80	K/W

CHARACTERISTICS

f_o = 10,7 MHz; Δf = ± 22,5 kHz; f_m = 400 Hz; R_S = 60 Ω; de-emphasis τ = 50 μs (C_{8-9} = 6,8 nF); T_{amb} = 25 °C; measured in Fig. 1, unless otherwise specified. The demodulator circuit is adjusted at minimum 2nd harmonic (d_2) distortion: V_i = 1 mV; Δf = ± 75 kHz.

Supply voltage range (pin 1)		V_P		7,5 to 20	V
		V_P = 8,5 V		V_P = 15 V	
Supply current; without load ($I_{12} = I_{13} = 0$)	I_P	typ.	16	18	mA
			10 to 23	12 to 25	mA
I.F. amplifier/detector					
Sensitivity at −3 dB before limiting	V_i	typ.	22		μV
		<	30		μV
I.F. sensitivity for					
S + N/N = 26 dB	V_i	typ.	8		μV
S + N/N = 46 dB	V_i	typ.	35		μV
I.F. output voltage (peak-to-peak value) V_i = 1 mV; $Z_{3-18} = Z_{7-18}$ = 1 MΩ in parallel with 10 pF	$V_{3-7(p-p)}$	typ.	680		mV
I.F. output resistance	R_{3-7}	typ.	250		Ω
Detector input impedance	R_{4-6}	typ.	30		kΩ
	C_{4-6}	typ.	1		pF
Output resistance	R_8; R_9	typ.	3,7		kΩ
D.C. output voltage	$V_{8-18} = V_{9-18}$	typ.	5,5	9,8	V
A.F. output voltage; Q_L = 20	V_o	typ.	67	135	mV
			60 to 75	120 to 150	mV
Total distortion					
single tuned circuit; Q_L = 20	d_{tot}	typ.	0,1		%
two tuned circuits	d_{tot}	typ.	0,02		%
Signal plus noise-to-noise ratio B = 250 Hz to 15 kHz; V_i > 1 mV	S + N/N	typ.	76	80	dB
A.M. rejection; V_i = 10 mV f.m.: f_m = 70 Hz; Δf = ± 22,5 kHz a.m.: f_m = 1 kHz; m = 0,3	α	typ.	54		dB*
I.F. input voltage range; α > 40 dB	V_i		0,5 to 500		mV
Hum suppression at f = 100 Hz $V_P = V_{1-18}$ = 100 mV r.m.s.; C_{2-18} = 47 μF	α_{100}	>	43		dB
		typ.	48		dB
A.F.C. tuning slope at Q_L = 20	$\frac{\Delta V_{8-9}}{\Delta f_o}$	typ.	8,5	17	mV/kHz
A.F.C. offset voltages; Q_L = 20 at V_i = 1 mV	$\pm \Delta V_{8-9}$	<	100	200	mV
at V_i = 30 μV to 500 mV (reference at 1 mV and muting)	$\pm \Delta V_{8-9}$	typ.	25	50	mV
		<	50	100	mV

* Simultaneously measured.

Field-strength indication

			V_P = 8,5 V	V_P = 15 V	
Indicator sensitivity; $I_{14} = 0$	V_i		20 μV to 600 mV		
Field-strength indicator voltage $R_{13\text{-}18}$ = 3,6 kΩ; $I_{14} = 0$ $V_i = 0$	$V_F = V_{13\text{-}18}$	typ.	0		mV
		<	200		mV
V_i = 250 mV	$V_F = V_{13\text{-}18}$	typ.	3,6		V
			3,2 to 4,1		V
Available output current	$-I_{13}$	>	2		mA
Reverse voltage at the output for FM 'off'; $V_{5\text{-}18} > 3{,}5$ V	$V_{13\text{-}18}$	>	5		V

Detune-detector

Quiescent input current; $V_{10\text{-}9} = 0$	I_{10}	typ.	20		nA
		<	100		nA
Output voltage range	$V_{11\text{-}18}$		1,8 to 5,0		V
Available output current	I_{11}	typ.	0,5		mA
			0,35 to 0,65		mA
Voltage gain: $\Delta V_{11}/\Delta(\pm V_{10\text{-}9})$ at I_{11} = 0,25 mA	G_v	typ.	–	3,3	
Input offset voltage (pin 10) at $V_{11\text{-}18}$ = 2,5 V	$V_{10\text{-}9}$	typ.	20		mV

Reference voltage

Output voltage; $-I_{12}$ = 1 mA	$V_{ref} = V_{12\text{-}18}$	typ.	5,1	5,3	V
Available output current	$-I_{12}$	typ.	2,5		mA

Standby switch

Required control voltage within the rated ambient temperature and supply voltage ranges for FM 'on'	$V_{5\ on}$	<	2		V
for FM 'off'	$V_{5\ off}$	>	3,5		V
Input switching current for FM 'on'	$-I_5$	<	100		μA

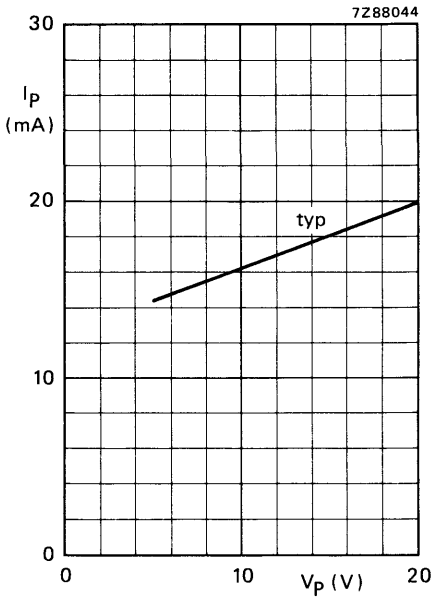


Fig. 2 Supply current consumption; without load.

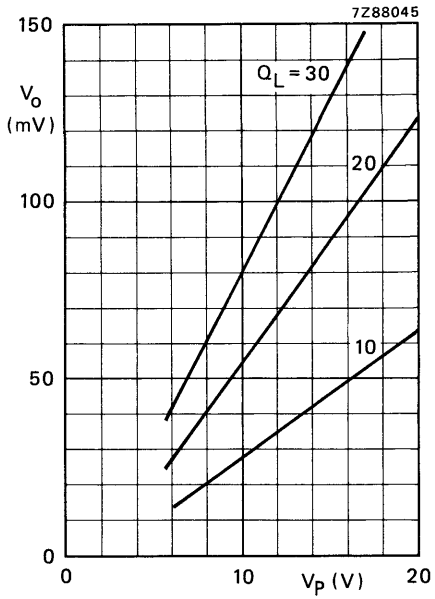


Fig. 3 A.F. output voltage; V_i = 1 mV (i.f.); $\Delta f = \pm$ 15 kHz; f_m = 400 Hz; typical values.

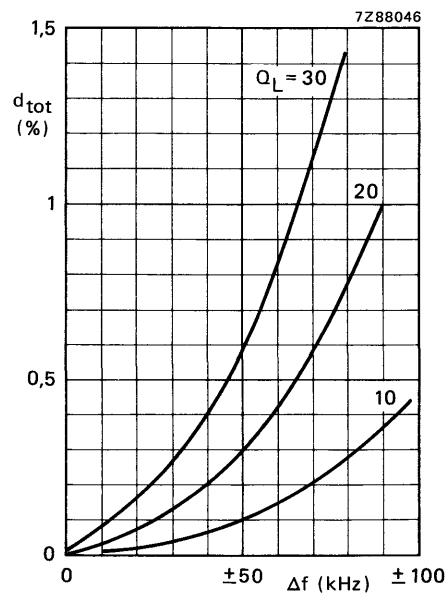


Fig. 4 Total distortion for single tuned circuit; V_i = 1 mV (i.f.); f_m = 400 Hz; adjusted at minimum 2nd harmonic distortion; typical values.

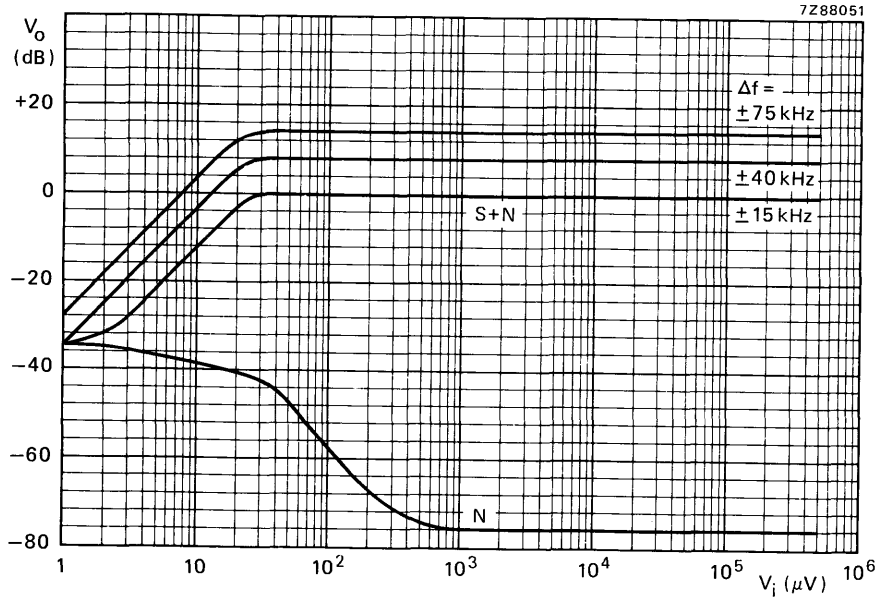


Fig. 5 A.F. output voltage level as a function of i.f. input voltage; S = signal voltage; N = noise voltage; V_P = 15 V; f_m = 400 Hz; B = 250 Hz to 16 kHz; Q_L = 20; $C_{8\text{-}9}$ = 6,8 nF; typical values.

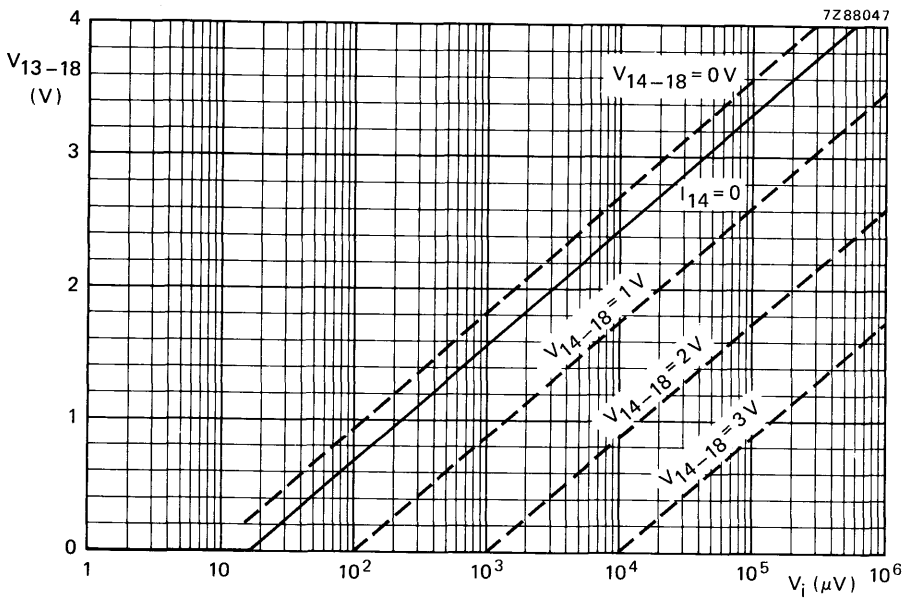


Fig. 6 Voltage at field-strength indicator output (proportional to $V_{12\text{-}18}$); $R_{13\text{-}18}$ = 3,6 kΩ.

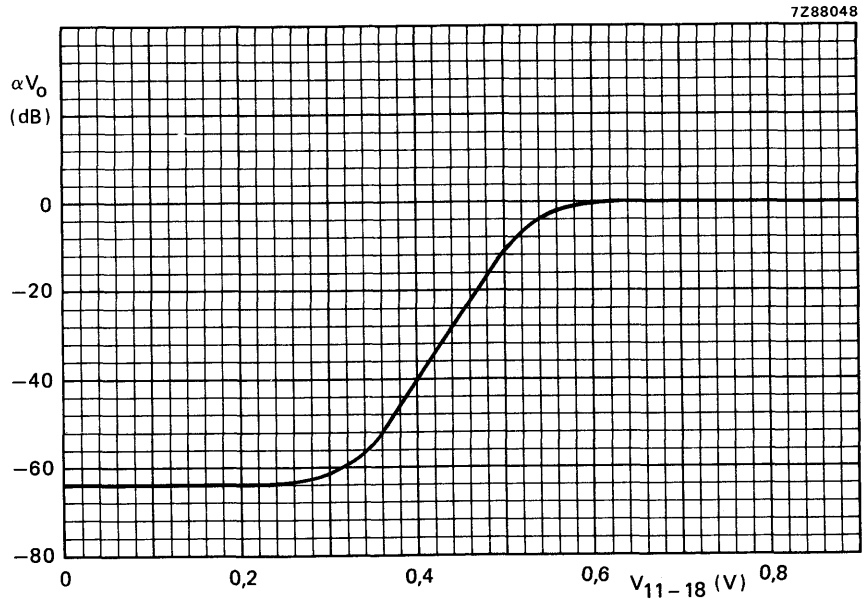


Fig. 7 Attenuation of output voltage (αV_o) as a function of the muting control voltage $V_{11\text{-}18}$.

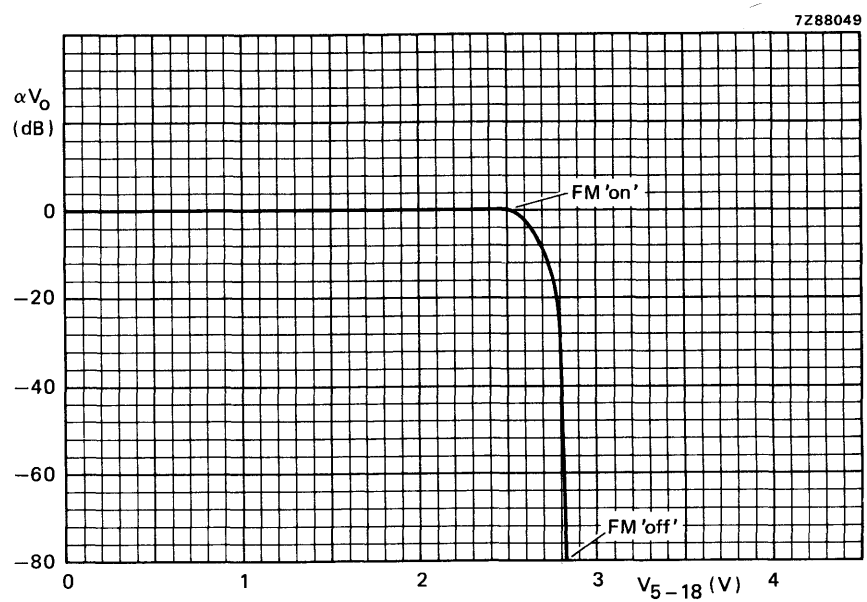
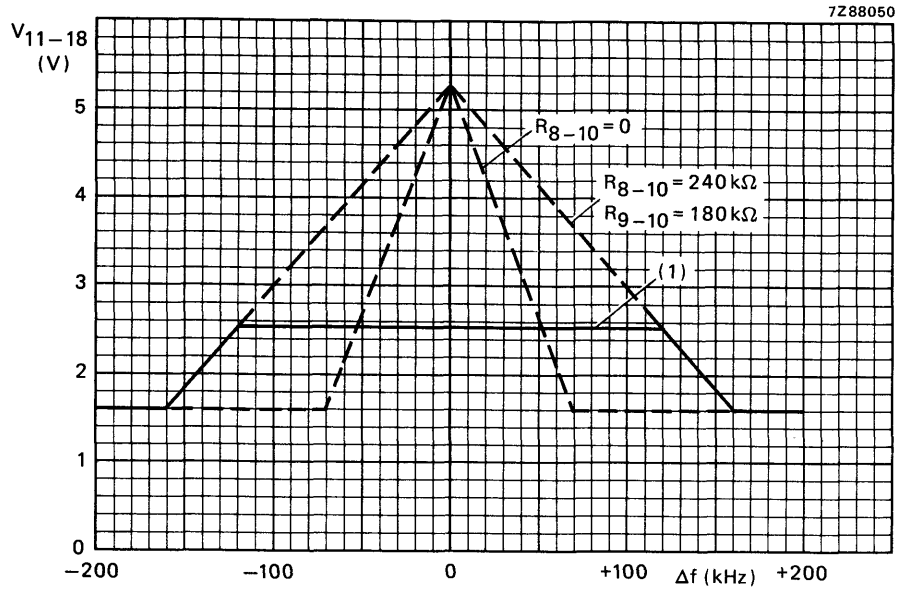


Fig. 8 FM 'on'/FM 'off' stand-by switch; attenuation of output voltage (αV_o) as a function of control voltage $V_{5\text{-}18}$.



(1) Limited by external preset ($\alpha \cdot V_{12\text{-}18}$).

Fig. 9 Detune-detector output voltage; V_P = 7,5 to 20 V; Q_L = 20.

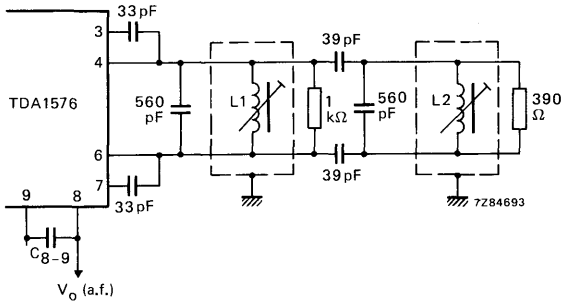


Fig. 10 Example of the TDA1576 when using a demodulator with two tuned circuits. Adjustment of the demodulator circuit is obtained with an i.f. signal which is higher than the 3 dB limiting level, L2 should be short-circuited or detuned, L1 should be adjusted to min. d_2 distortion, and then L2 to min. d_2 distortion. Coil data: L1 = L2 = 0,38 μH; Q_0 = 70; coil former KAN (C).

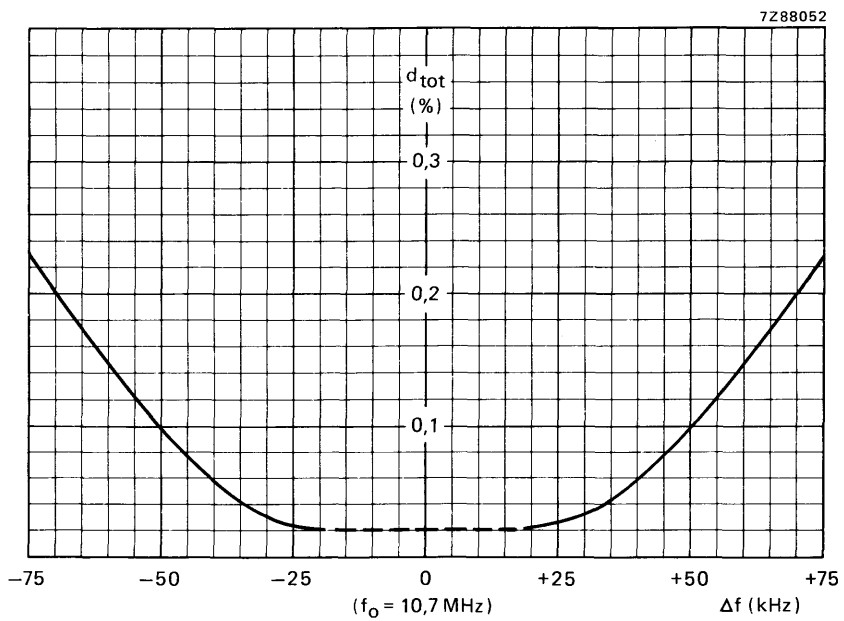
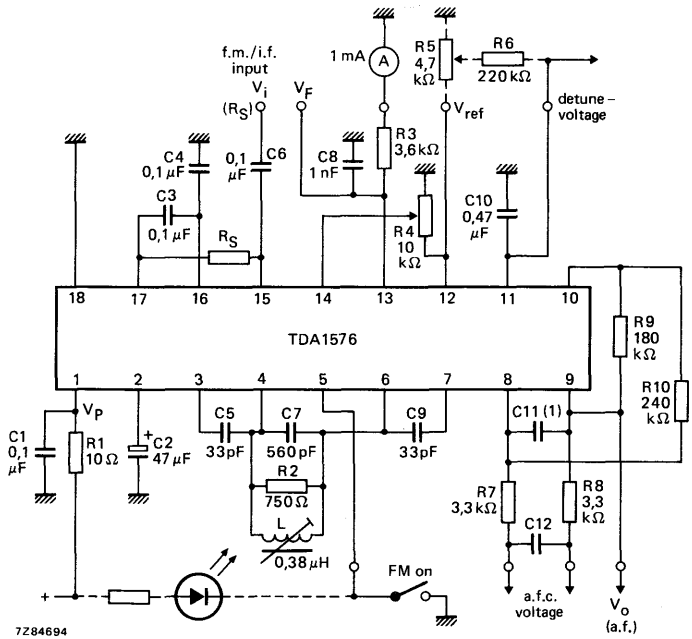


Fig. 11 Total distortion as a function of detuning; f_m = 400 Hz; C_{8-9} = 6,8 nF; Δf = ± 75 kHz; V_o = 330 mV for a frequency deviation Δf = ± 75 kHz.



(1) For mono: C11 = 6,8 nF; for stereo: C11 = 56 pF.

Fig. 12 Application example of using TDA1576.

TIME MULTIPLEX PLL STEREO DECODER

GENERAL DESCRIPTION

The TDA1578A is a PLL stereo decoder based on the time-division multiplex principle.

Features

- adjustable input and output voltage levels
- automatic mono/stereo switching with hysteresis, controlled by both pilot signal and field strength level
- analogue control of mono/stereo change over
- pilot indicator driver
- analogue muting control
- muting indicator driver
- oscillator with decoupled frequency measurement output
- electronic smoothing of the supply voltage

QUICK REFERENCE DATA

Measured with a frequency deviation $\Delta f = \pm 75$ kHz without pilot; $f_m = 1$ kHz					
Supply voltage (pin 8)	$V_P = V_{8-7}$	typ.	8,5	15	V
Supply current (pin 8)	$I_P = I_8$	typ.	21	30	mA
Multiplex input signal (adjustable)	$V_{MUX(p-p)}$	typ.	0,5	1	V
Input resistance (adjustable)	R_i	typ.		47	kΩ
A.F. output voltage (R = 15 kΩ)	V_o	typ.	0,75	1,5	V
Output resistance	R_o		low-ohmic		
Spread in gain	ΔG_v	⩽		1	dB
Channel separation	α	typ.		50	dB
Total harmonic distortion	THD	⩽	0,3	0,1	%
Signal-to-noise ratio	S/N	typ.		90	dB
Carrier and harmonic suppression					
pilot signal; f = 19 kHz	α_{19}	typ.		32	dB
subcarrier; f = 38 kHz	α_{38}	typ.		50	dB
f = 57 kHz	α_{57}	typ.		46	dB
f = 76 kHz	α_{76}	typ.		60	dB
traffic radio (V.W.F.); f = 57 kHz	$\alpha_{57(VWF)}$	typ.		70	dB
SCA (Subsidiary Communications Authorization); f = 67 kHz	α_{67}	typ.		70	dB
ACI (Adjacent Channel Interference); f = 114 kHz	α_{114}	typ.		80	dB
intermodulation; f = 10/13 kHz	α_2, α_3	typ.		70	dB
Supply voltage range (pin 8)	$V_P = V_{8-7}$		7,5 to 18		V
Operating ambient temperature range	T_{amb}		−30 to + 80		°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

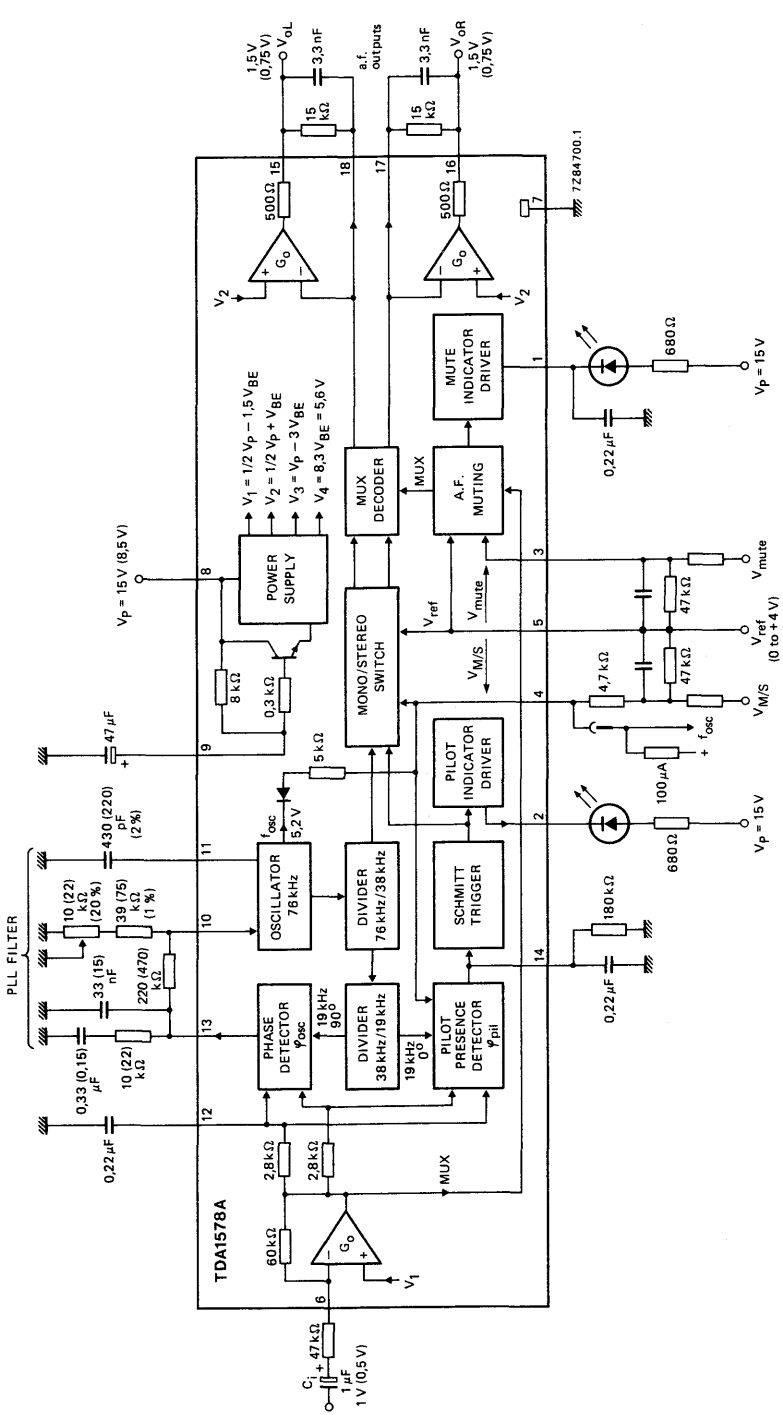


Fig. 1 Block diagram with external components; used as test circuit. Values given in parentheses are for V_P = 8,5 V.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-7}$	max.	20	V
Input voltages (pins 3, 4 and 5)	$V_{3;4;5-7}$		0 to 12	V
Indicator driver output voltage	$V_{1;2-7}$	max.	24	V
Indicator driver output current	$I_1; I_2$	max.	30	mA
Total power dissipation at T_{amb} = 25 °C	P_{tot}	max.	1,2	W
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ c-a}$	=	80	K/W

CHARACTERISTICS (measured in Fig. 1)

Input signal: m = 100% ($\Delta f = \pm 75$ kHz); pilot signal: m = 9% ($\Delta f = \pm 6{,}75$ kHz);
modulation frequency: 1 kHz; $V_{3\text{-}5} = V_{4\text{-}5} = 0$ V;
de-emphasizing time: T = 50 μs; oscillator adjusted to f_{osc} at a pilot voltage $V_i = 0$ V;
$T_{amb} = 25\ ^{o}C$; unless otherwise specified

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Supply voltage range (pin 8)	–	V_P	7,5	–	18	V
Supply current (except output and indicator) pin 8	8,5	I_P	–	21	–	mA
	15	I_P	–	30	40	mA
Nominal multiplex input voltage (peak-to-peak value)	8,5	$V_{MUX(p\text{-}p)}$	–	0,5	–	V
$R_i = 47$ kΩ	15	$V_{MUX(p\text{-}p)}$	–	1,0	–	V
Overdrive reserve of input						
at THD = 1 %	8,5		3	6	–	dB
at THD = 0,3 %	15		3	6	–	dB
A.F. output voltage (r.m.s. value; mono without pilot)						
$R_{15\text{-}18} = R_{16\text{-}17} = 15$ kΩ	8,5	$V_{o(rms)}$	–	0,75	–	V
	15	$V_{o(rms)}$	–	1,5	–	V
$R_{15\text{-}18} = R_{16\text{-}17} = 24$ kΩ	8,5	$V_{o(rms)}$	–	1,2	–	V
	15	$V_{o(rms)}$	–	2,4	–	V
Overdrive reserve of output $R_{15\text{-}18} = R_{16\text{-}17} = 24$ kΩ	*		3	–	–	dB
Spread in output voltage levels	*	$\pm \Delta V_o/V_o$	–	–	1	dB
Difference of output voltage levels	*	$\pm \Delta V_{15\text{-}16}/V_o$	–	–	1	dB
Output resistance	*	R_o	low-ohmic			
Available output current pins 15 and 16	*	$\pm I_o$	–	–	–	mA
Modulation range at output (unloaded)	*	$V_{15;16\text{-}7}$	–	1 to $V_{9\text{-}7} - 1$	–	V
Internal current limiting	*	I_o	–	15	–	mA
D.C. output voltage	8,5	$V_{15;16\text{-}7}$	3,6	4,1	4,6	V
$R_{15\text{-}18} = R_{16\text{-}17} = 24$ kΩ	15	$V_{15;16\text{-}7}$	7,0	7,7	8,4	V
D.C. current (pins 17 and 18)	8,5	$-I_{17;18}$	–	33	–	μA
	15	$-I_{17;18}$	–	23	–	μA

* $V_P = 8{,}5$ or 15 V.

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Channel separation	8,5	α	32	50	–	dB
at $V_{4-5} = 0$ V	15	α	39	50	–	dB
Total harmonic distortion	8,5	THD	–	0,1	0,3	%
	15	THD	–	0,04	0,1	%
Signal-to-noise ratio	8,5	S/N	–	87	–	dB
f = 20 Hz to 16 kHz	15	S/N	–	90	–	dB
Carrier and harmonic suppression at the output						
pilot signal; f = 19 kHz	*	α_{19}	–	32	–	dB
subcarrier; f = 38 kHz	*	α_{38}	40	50	–	dB
f = 57 kHz	*	α_{57}	–	46	–	dB
f = 76 kHz	*	α_{76}	–	60	–	dB
intermodulation (note 1) f_m = 10 kHz; spurious signal f_s = 1 kHz						
PLL-filter Fig. 1	*	α_2	–	50	–	dB
PLL-filter Fig. 2	*	α_2	–	70	–	dB
f_m = 13 kHz; spurious signal f_s = 1 kHz	*	α_3	–	75	–	dB
traffic radio (V.W.F.); f = 57 kHz (note 2)	*	$\alpha_{57(VWF)}$	–	70	–	dB
SCA (Subsidiary Communications Authorization); f = 67 kHz (note 4)	*	α_{67}	–	70	–	dB
ACI (Adjacent Channel Interference) (note 3);						
f = 114 kHz	*	α_{114}	–	80	–	dB
f = 190 kHz	*	α_{190}	–	52	–	dB
Ripple rejection at the output; f = 100 Hz; $V_{P(rms)}$ = 100 mV (pin 8)	*	RR_{100}	40	43	–	dB
Voltage on filter capacitor without external load	*	V_{9-7}	–	V_P–0,25	–	V
Source resistance	*	R_{9-8}	6	8	10	kΩ

* V_P = 8,5 or 15 V.

CHARACTERISTICS (continued)

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Mono/stereo control						
Pilot threshold voltages (peak-to-peak values)						
for stereo 'ON'	8,5	$V_{i(p-p)}$	–	21	30	mV
	15	$V_{i(p-p)}$	–	43	61	mV
for mono 'ON'	8,5	$V_{i(p-p)}$	6	15	–	mV
	15	$V_{i(p-p)}$	12	30	–	mV
Switch hysteresis						
$V_{i\,ON}/V_{i\,OFF}$	*	ΔV_i	–	3	–	dB
Switching time at $C_{14-7} = 0{,}22\ \mu F$						
for stereo 'ON'	*	$t_{st\,ON}$	–	15	–	ms
for mono 'ON'	*	$t_{m\,ON}$	–	27	–	ms
External mono/stereo control (see Fig. 12 and note 5)						
Switching voltage for external mono control	8,5	V_{14-7}	–	–	0,7	V
	15	V_{14-7}	–	–	1,4	V
	*	or: $-V_{4-5}$	315	–	–	mV
Control voltage for channel separation: α = 6 dB	8,5	$-V_{4-5}$	–	120	–	mV
	15	$-V_{4-5}$	–	130	–	mV
	*	ΔV_{4-5}	–	–	± 20	mV
α = 26 dB	8,5	$-V_{4-5}$	–	70	–	mV
	15	$-V_{4-5}$	–	80	–	mV
Control voltage for mono 'ON'	8,5	$-V_{4-5}$	–	240	–	mV
	15	$-V_{4-5}$	–	270	–	mV
for stereo 'ON'	8,5	$-V_{4-5}$	–	220	–	mV
	15	$-V_{4-5}$	–	250	–	mV
Control voltage difference for α = 6 dB; stereo 'ON'	8,5	ΔV_{4-7}	80	100	120	mV

* V_P = 8,5 or 15 V.

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Muting circuit (see Fig. 13 and note 5)						
Control voltage for an attenuation: α = 3 dB	8,5	$-V_{3-5}$	–	140	–	mV
	15	$-V_{3-5}$	–	145	–	mV
	*	ΔV_{3-5}	–	± 20	–	mV
α = 26 dB	8,5	$-V_{3-5}$	–	255	–	mV
	15	$-V_{3-5}$	–	270	–	mV
Attenuation						
with V_{3-5} = 0 V	*	α	–	–	0,2	dB
with $-V_{3-5}$ = 450 mV	*	α	–	80	–	dB
LED driver output current at an attenuation: α = 3 dB	*	I_1	1,2	1,7	2,2	mA
Control voltage for I_1 = 200 μA	8,5	$-V_{3-5}$	–	150	–	mV
	15	$-V_{3-5}$	–	160	–	mV
Control inputs						
Recommended voltage range	*	$V_{3;4;5-7}$	0	–	4	V
Input bias current	*	$I_{3;4;5}$	–	10	100	nA
Indicator driver						
Output saturation voltages at I_1 = 20 mA; V_{3-5} = 0 V	*	V_{1-7sat}	–	1,2	1,8	V
at I_2 = 20 mA	*	V_{2-7sat}	–	0,5	1,0	V
Output leakage current at $V_{1;2-7}$ = 24 V	*	$I_{1;2}$	–	20	–	μA

* V_P = 8,5 or 15 V.

CHARACTERISTICS (continued)

parameter	V_P (V)	symbol	min.	typ.	max.	unit
VCO						
Oscillator frequency adjustable with R_{10-7}	*	f_{osc}	–	76	–	kHz
Spread of free-running frequency at nominal external circuitry	*	f_{osc}	71	–	82	kHz
Free-running frequency dependency (note 6)						
with temperature	*	TC	–	1×10^{-4}	–	K^{-1}
with supply voltage	*	$\Delta f_{osc}/\Delta V_P$	–	–	400	Hz/V
Capture and holding range for a pilot input voltage $V_{pil} = 0{,}5 \times V_{pil\,nom}$	*	$\Delta f/f$	± 2	–	–	%
PLL control slope (total)	*	S_{tot}	–	4,5	–	kHz/μs
D.C. voltage at pin 10	*	V_{10-7}	–	2,1	–	V
		or:	–	3,2 V_{BE}	–	V
Frequency measuring point; internal switching threshold	*	V_{4-7}	–	6	–	V
		or:	–	9 V_{BE}	–	V
Output voltage (peak-to-peak value) at pin 4; R = 4,7 kΩ	*	$V_{4-7(p-p)}$	–	350	–	mV
Output resistance	*	R_{4-7}	–	5	–	kΩ

* V_P = 8,5 or 15 V.

Notes to the characteristics

1. Intermodulation suppression (BFC: Beat-Frequency Components)

$$\alpha_2 = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 1\ kHz)};\ f_s = (2 \times 10\ kHz) - 19\ kHz$$

$$\alpha_3 = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 1\ kHz)};\ f_s = (3 \times 13\ kHz) - 38\ kHz$$

measured with: 91% mono signal; f_m = 10 or 13 kHz; 9% pilot signal.

2. Traffic radio (V.W.F.) suppression

$$\alpha_{57(VWF)} = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 1\ kHz \pm 23\ kHz)}$$

measured with: 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 kHz, f_m = 23 Hz AM, m = 60%).

3. ACI (Adjacent Channel Interference)

$$\alpha_{114} = \frac{V_{o\ (signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 4\ kHz)};\ f_s = 110\ kHz - (3 \times 38\ kHz)$$

$$\alpha_{190} = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 4\ kHz)};\ f_s = 186\ kHz - (5 \times 38\ kHz)$$

measured with: 90% mono signal; f_m = 1 kHz; 9% pilot signal; 1% spurious signal (f_s = 110 or 186 kHz, unmodulated).

4. SCA (Subsidiary Communications Authorization)

$$\alpha_{67} = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 9\ kHz)};\ f_s = (2 \times 38\ kHz) - 67\ kHz$$

measured with: 81% mono signal; f_m = 1 kHz; 9% pilot signal; 10% SCA-subcarrier (f_s = 67 kHz, unmodulated).

5. Assuming $V_T = \frac{k \times T}{q}$ = 28,6 mV at T_j = 330 K.

6. The effects of external components are not taken into account.

APPLICATION NOTES

1. When mono/stereo control and muting control are not used, pins 3, 4 and 5 have to be grounded.
2. In a receiver, channel separation adjustment can be obtained by:
   a. A capacitor at pin 12 (C_{12-7}): phasing 19/38 kHz
   b. RC or LCR filter at the input: frequency response compensation ($V_G = f(\omega)$)
   c. Feeding the output signals of the output amplifier to the inputs of the other channel.
3. PLL-filter for reduced intermodulation (α_2); see Fig. 2.
4. External mono 'ON' switch; see Fig. 3.
5. Switching 'OFF' the oscillator; see Fig. 4.

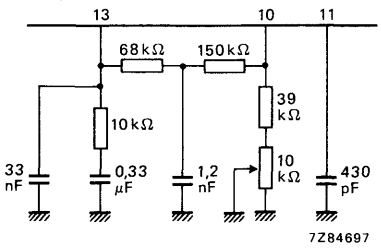


Fig. 2 PLL-filter for α_2 = 70 dB at V_P = 15 V (see also Fig. 1).

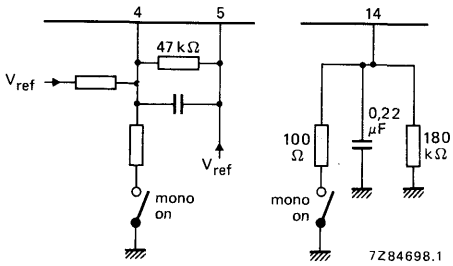


Fig. 3 (a) At pin 4; $-V_{4-5} > 300$ mV; (b) at pin 14.

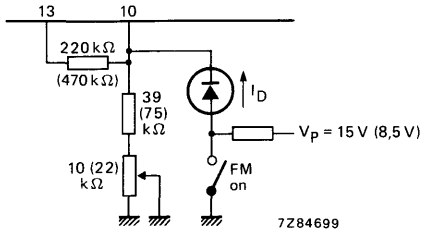


Fig. 4 The oscillator is switched-off when: $I_D > 100$ µA (> 50 µA for V_P = 8,5 V) and $I_D < 1$ mA.

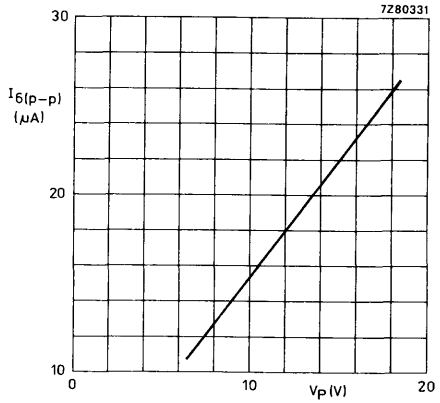


Fig. 5 Signal handling range at the input for I_{6nom} (± 75 kHz); $V_{9-7} = V_P$.

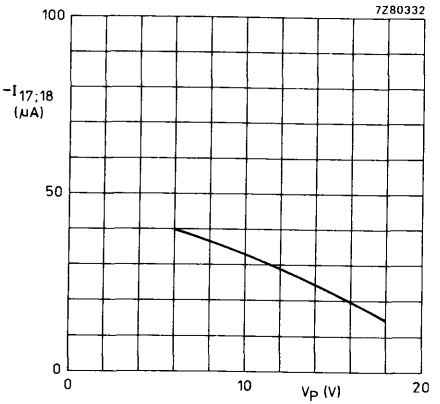
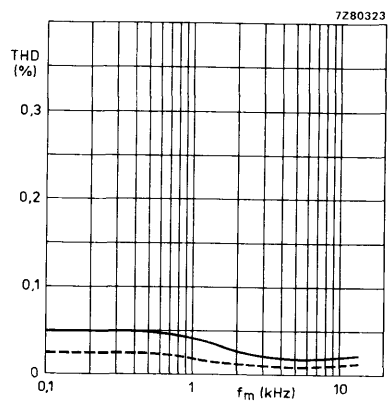


Fig. 7 D.C. current in the feedback loop of the output amplifier.



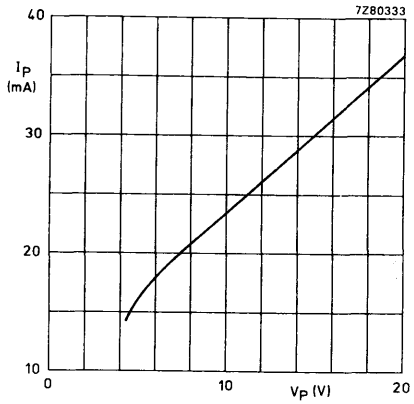


Fig. 6 Supply current comsumption at $V_{9-7} = V_P$.

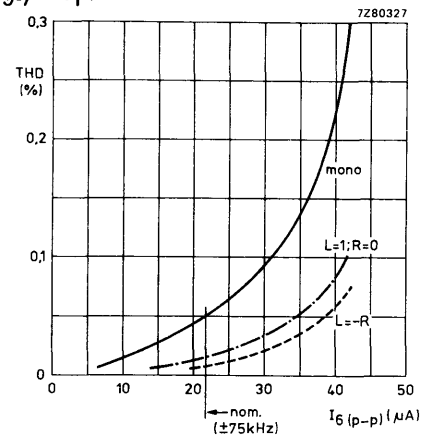


Fig. 8 Total harmonic distortion (THD) as a function of the peak-to-peak input current at pin 6; V_P = 15 V; f_m = 1 kHz; $V_{3-5} = V_{4-5}$ = 0 V.

Fig. 9 Total harmonic distortion (THD) as a function of the modulation frequency (f_m); V_P = 15 V; $I_{6(p-p)}$ = 21,5 μA.

———— mono

– – – – stereo; L = –R; 91% + 9% pilot signal.

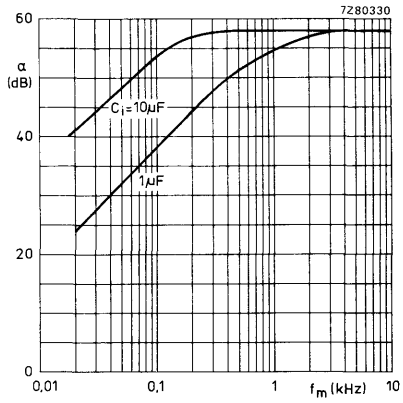


Fig. 10 Channel separation (α) as a function of the modulation frequency (f_m); V_P = 15 V; R_i = 47 kΩ; V_{4-5} = 0 V.

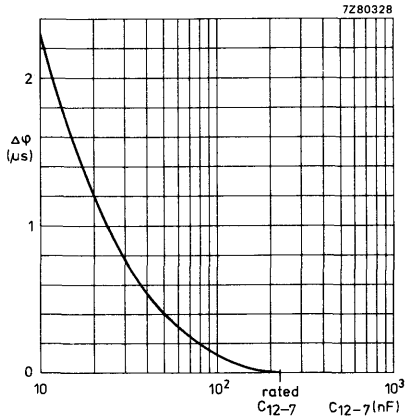


Fig. 11 Phase shift between pilot signal at the input and the internal carrier processing as a function of C_{12-7}.

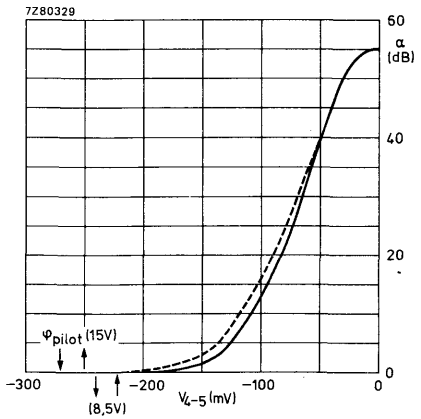


Fig. 12 Mono/stereo control at f_m = 1 kHz; α is the channel separation.
——— V_P = 8,5 V
– – – – V_P = 15 V

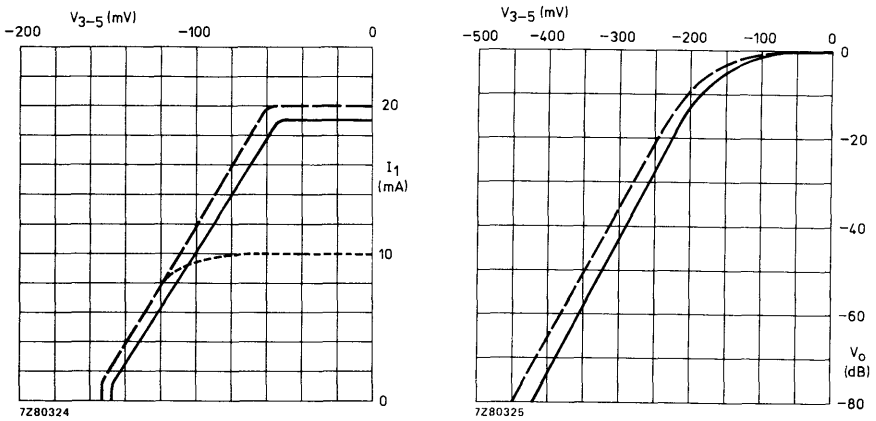


Fig. 13 Muting (V_o) and muting indicator current (I_1) as a function of V_{3-5}.

V_o in dB curves; ——— V_P = 8,5 V
– – – – V_P = 15 V

I_1 in mA curves for V_{PL}/R_{bias1} (pin 1); – – – – 22 V/1 kΩ
——— 14 V/680 Ω
- - - - - - - 10 V/680 Ω

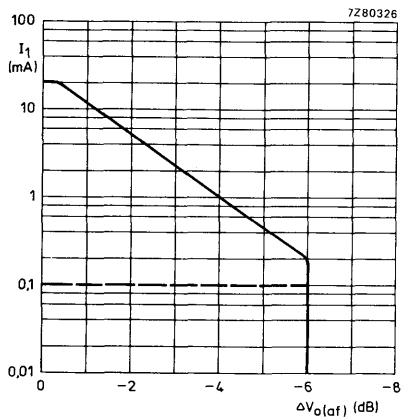


Fig. 14 Muting indicator current; V_P = 8,5 to 15 V; V_{PL} = 14 V.

——— R_{bias1} = 680 Ω
– – – – R_{bias1} = matched

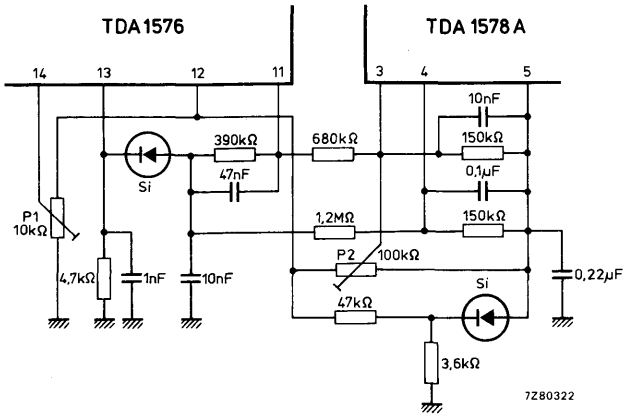


Fig. 15 Application information for external circuitry to provide external mono/stereo and muting control.

Adjustment recommendations:

at $V_{i(hf)}$ = 100 μV with P1 to α = 6 dB (channel separation),
at $V_{i(hf)}$ = 15 μV with P2 to $V_{o(af)}$ = −3 dB.

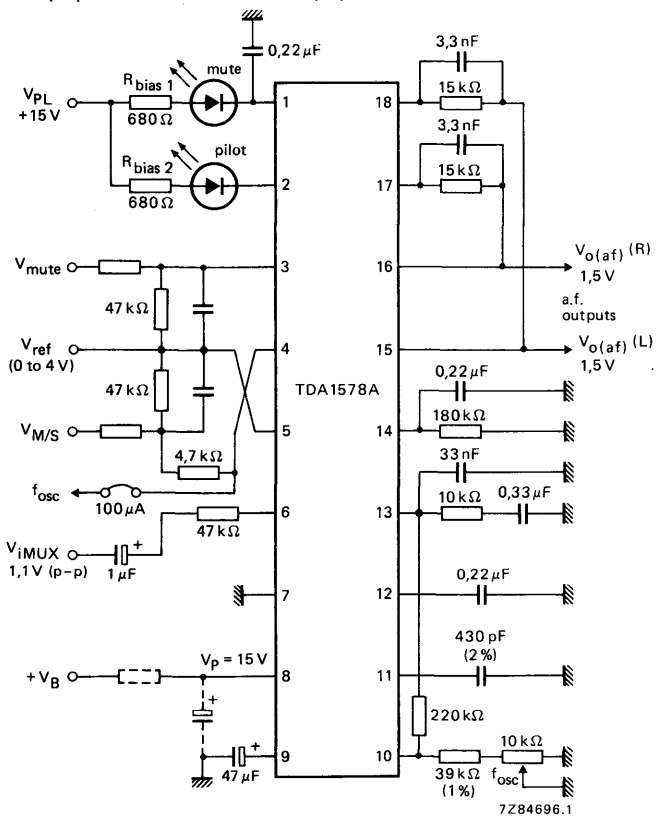


Fig. 16 Typical application circuit using TDA1578A for V_P = 15 V.

DECODER FOR TRAFFIC WARNING (VWF) RADIO TRANSMISSIONS

GENERAL DESCRIPTION

The TDA1579 decoder is for radio transmissions having 57 kHz amplitude-modulated subcarriers as used in the German 'Verkehrs Warnfunk' (VWF) traffic warning system.

Features

- Selective subcarrier amplifier (57 kHz) with gain control
- Transmitter identification signal (SK) decoder
- Area identification signal (BK) and announcement identification signal (DK) active filtering
- BK and DK decoders (Schmitt trigger with switched hysteresis)
- BK and DK switch-on/switch-off delay circuits
- Driver output for SK indicator (LED)
- SK and BK control outputs

QUICK REFERENCE DATA

Measured in Fig. 1 at V_{iSK} = 8 mV; f = 57 kHz amplitude modulated with f_m = 34.95 Hz and m = 60% for 'BK-traffic area C' signal; or with f_m = 125 Hz and m = 30% for DK signal

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	7.5	8.5	12	V
Supply current		I_P	–	6	–	mA
Nominal input voltage	at f = 57 kHz	V_{iSK}	–	8	–	mV
Input impedance	at f ≤ 57 kHz	$\|Z_i\|$	100	–	–	kΩ
Control level	−3 dB	V_{iSK}	–	2.4	–	mV
Input voltage	peak-to-peak value	$V_{i(p-p)}$	2	–	–	V
SK switch-on threshold level		m_{BKon}	–	42	–	%
SK switch hysteresis		Δm_{BK}	–	3.5	–	dB
SK switch-on delay		t_{dSKon}	–	150	–	ms
SK switch-off delay		t_{dSKoff}	–	750	–	ms
DK switch-on threshold level		m_{DKon}	–	13	–	%
DK switch hysteresis		Δm_{DK}	–	3.6	–	dB
DK switch-on delay		t_{dDKon}	–	750	–	ms
DK switch-off delay		t_{dDKoff}	–	750	–	ms
Ambient operating temperature range		T_{amb}	−30	–	+ 80	°C

PACKAGE OUTLINES

TDA1579: 18-lead DIL; plastic (SOT102).
TDA1579T: 20-lead mini-pack; plastic (SO20; SOT163A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
All pin numbers in this table apply to TDA1579; for TDA1579T refer to Fig. 1.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 7	$V_P = V_{7\text{-}18}$	–	–	18	V
Switch output voltage	pin 1	$V_{1\text{-}18}$	–	–	23	V
	pins 2 or 3	$V_{2;3\text{-}18}$	–	–	18	V
	pins 1, 2 or 3	$-V_{1;2;3\text{-}18}$	–	–	0.5	V
Switch output current	pin 1	I_1	–	–	50	mA
	pins 2 or 3	$I_{2;3}$	–	–	5	mA
	pins 1, 2 or 3	$-I_{1;2;3}$	–	–	10	mA
Signal input voltage	pin 13	$V_{13\text{-}18}$	–	–	V_P	
	pin 13	$-V_{13\text{-}18}$	–	–	0.5	V
Signal input current	pin 13	$-I_{13}$	–	–	10	mA
Total power dissipation		P_{tot}	–	–	800	mW
Storage temperature range		T_{stg}	−55	–	+ 150	°C
Operating ambient temperature range		T_{amb}	−30	–	+ 80	°C

CHARACTERISTICS

V_P = 8.5 V; T_{amb} = 25 °C; measured at nominal input signal: V_{iSK} = 8 mV, f = 57 kHz amplitude modulated with f_m = 34.95 Hz and m = 60% for 'BK-traffic area C' signal; or with f_m = 125 Hz and m = 30% for DK signal.
All pin numbers in this table apply to TDA1579, for TDA1579T refer to Fig. 1.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 7	V_P	7.5	–	12	V
Supply current	pin 7	I_P	–	6	10	mA
SK amplifier/decoder						
Input impedance	f ⩽ 57 kHz	$\|Z_i\|$	100	–	–	kΩ
Input voltage (peak-to-peak value)		$V_{i(p\text{-}p)}$	2	–	–	V
Input voltage at start of gain control	V_{o9BK} = −3 dB	V_{iSK}	–	2.4*	–	mV
Voltage gain	V_{9BK}/V_{13SK}	$G_{v9\text{-}13}$	–	44*	–	dB

* Selectable by $R_{12\text{-}8}$ or $Z_{10\text{-}8}$.

parameter	conditions	symbol	min.	typ.	max.	unit
SK amplifier/decoder (continued)						
Gain spread		$\pm \Delta G_{v9\text{-}13}$	–	–	2	dB
Gain control range		ΔG_v	40	–	–	dB
Controlled output voltage		V_{o9BK}	–	440	–	mV
		V_{o9DK}	–	220	–	mV
BK circuit						
Switch-on threshold level	pin 3 high-Z	V_{o5BKon}	600	670	750	mV
Switch hysteresis		$\frac{V_{o5BKon}}{V_{o5BKoff}}$	3	3.5	4	dB
BK switch threshold level for BK-off (SK-off) (typ. value = $0.21V_{8\text{-}18}$)	pin 3 conducting	$V_{4\text{-}18off}$	0.8	0.88	0.97	V
SK output (pin 3)						
allowable load current		I_3	–	–	1.5	mA
saturation voltage	I_3 = 1.5 mA	$V_{3\text{-}18sat}$	–	–	0.35	V
rejection voltage	$I_3 < 5\ \mu A$	$V_{3\text{-}18}$	18	–	–	V
Indicator driver (pin 1)						
allowable load current		I_1	–	–	40	mA
saturation voltage	I_1 = 20 mA	$V_{1\text{-}18sat}$	–	–	0.8	V
rejection voltage	$I_1 < 10\ \mu A$	$V_{1\text{-}18}$	23	–	–	V
DK circuit						
Switch-on threshold level	pin 2 high-Z	V_{15DKon}	600	670	750	mV
Switch hysteresis		$\frac{V_{15DKon}}{V_{15DKoff}}$	3.1	3.6	4.1	dB
DK switch threshold level for DK-off (Schmitt trigger output) (typ. value = 1 x V_{BE})	pin 2 conducting	$V_{16\text{-}18off}$	–	0.6	–	V
DK output (pin 2)						
allowable load current		I_2	–	–	1.5	mA
saturation voltage	I_2 = 1.5 mA	$V_{2\text{-}18sat}$	–	–	0.35	V
rejection voltage	$I_2 < 5\ \mu A$	$V_{2\text{-}18}$	18	–	–	V
BK and DK filter amplifiers						
Open loop gain	f = 100 Hz	G_o	84	–	–	dB
Current gain		G_i	120	–	–	dB
Input bias current		$\pm I_i$	–	–	50	nA
Output offset voltage	$R_{5\text{-}6} = R_{14\text{-}15}$ = 680 kΩ	$\pm V_{o5\text{-}8}$ / $\pm V_{15\text{-}8}$	–	–	50	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
BK and DK filter amplifiers (continued)						
Available output current		$\pm I_o$	1	–	–	mA
Output resistance		R_o	–	2	3.5	kΩ
Allowable load capacitance		C_L	–	–	50	pF
Internal reference voltage						
Output voltage (typ. value = 0.5 V_P)		$V_{8\text{-}18}$	4.0	4.25	4.5	V
Internal resistance of voltage source		R_8	–	–	5	Ω
Available output current		$-I_8$	2	–	–	mA
		$+I_8$	0.6	–	–	mA
Output short-circuit current (typ. value = V_P/1 kΩ)		$-I_{8sc}$	–	8	–	mA
Reference current source						
Reference voltage (typ. value = $V_{8\text{-}18}-V_{BE}$)		$V_{17\text{-}18}$	–	3.6	–	V
Internal biasing resistor		R_{i17}	–	5	–	kΩ
Allowable range of external reference resistor		$R_{17\text{-}18}$	180	–	270	kΩ

APPLICATION INFORMATION (Fig. 1)

parameter	symbol		application	unit
SK switch-on threshold level at m_{BK} = 60%	V_{iSKon}	typ.	1.8	mV
SK switch-on threshold level at V_{iSK} = 8 mV	m_{BKon}	typ.	32	%
SK switch hysteresis	$\frac{m_{BKon}}{m_{BKoff}}$	>	3.0	dB
		typ.	3.5	dB
		<	4.0	dB
SK switch-on delay (note 1)	t_{dSKon}	typ.	95	ms
		<	130	ms
SK switch-off delay (note 2)	t_{dSKoff}	>	380	ms
		typ.	500	ms
		<	620	ms
DK switch-on threshold level at m_{DK} = 30%	V_{iDKon}	typ.	1.5	mV
DK switch-on threshold level at V_{iDK} = 8 mV	m_{DKon}	typ.	13	%
DK switch hysteresis	$\frac{m_{DKon}}{m_{DKoff}}$	>	3.1	dB
		typ.	3.6	dB
		<	4.1	dB
DK switch-on delay (note 1)	t_{dDKon}	typ.	750	ms
		<	1000	ms
DK switch-off delay (note 2)	t_{dDKoff}	>	600	ms
		typ.	750	ms
		<	1000	ms

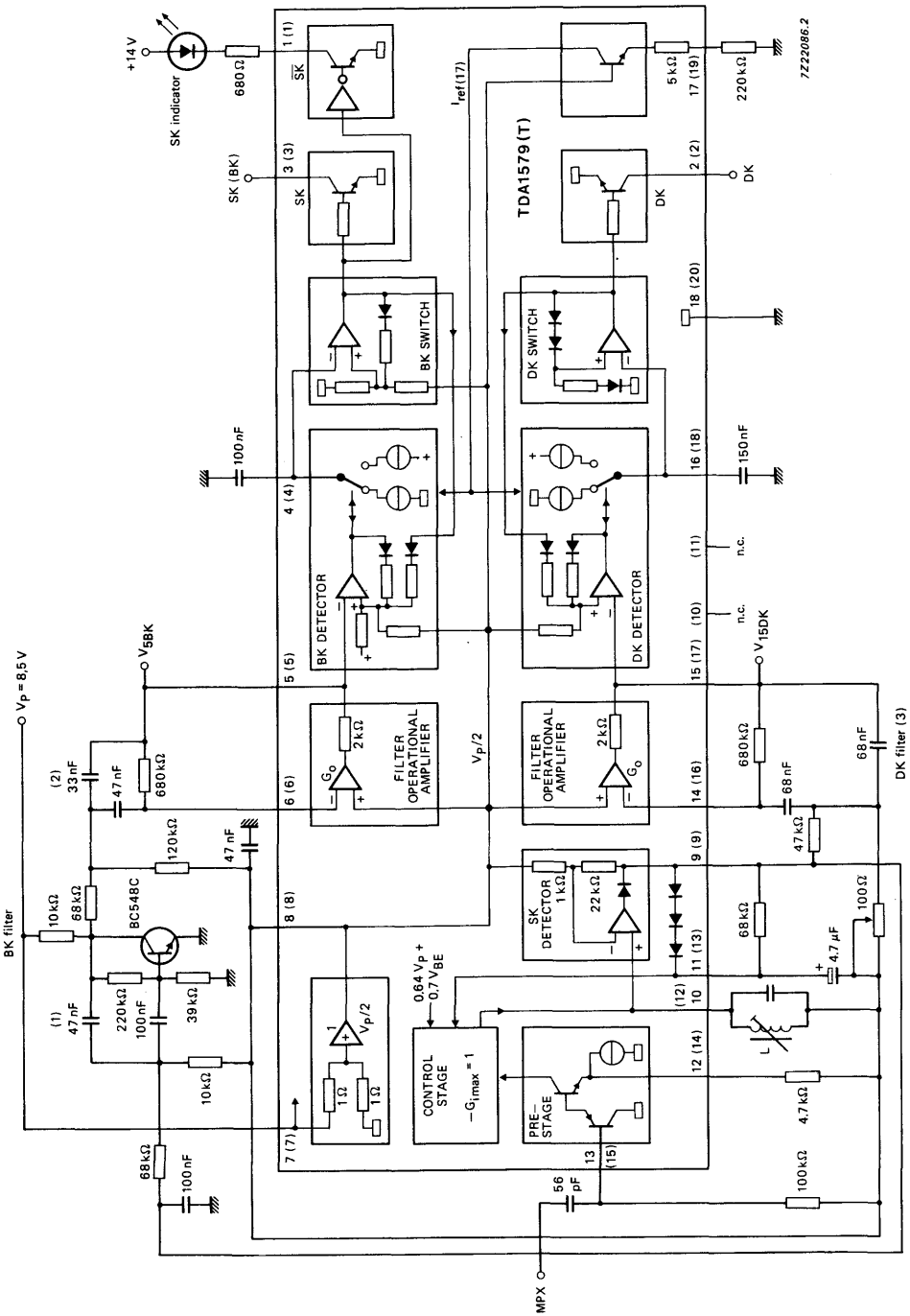
Notes

1. **Sequence for measuring switch-on delay times** (t_{don})
   a) Nominal BK or DK input signal at pin 13: $V_{i(p\text{-}p)}$ = 8 mV; f = 57 kHz; modulation-on.
   b) Pin 4 of the BK detector (pin 16 of the DK detector) is switched to ground to cause a low signal at the SK output at pin 3 (DK output at pin 2).
   c) t_{don} commences when the ground connection is removed from pin 4 (pin 16) as the positive-going V_{oBK} signal at pin 5 (V_{oDK} signal at pin 15) crosses zero.

   t_{don} ends when the positive-going edge of the SK output arrives at pin 13 (DK at pin 2).
2. **Sequence for measuring switch-off delay times** (t_{doff})
   a) Nominal operating conditions as in note 1.
   b) t_{doff} commences when the input is switched off as the negative-going V_{oBK} signal at pin 5 (V_{oDK} signal at pin 15) crosses zero.

   t_{doff} ends when the negative-going edge of the SK output arrives at pin 3 (DK at pin 2).

APPLICATION INFORMATION (continued)



L = 2.36 mH; Q_L = 70; C = 3.3 nF; f_o = 57 kHz.
Pin numbers in parentheses are for TDA1579T, other pin numbers are for TDA1579.

(1) f_o = 55 Hz; Q = 1.9
(2) f_o = 24 Hz; Q = 1.9
(3) f_o = 125 Hz

Fig. 1 Application diagram.

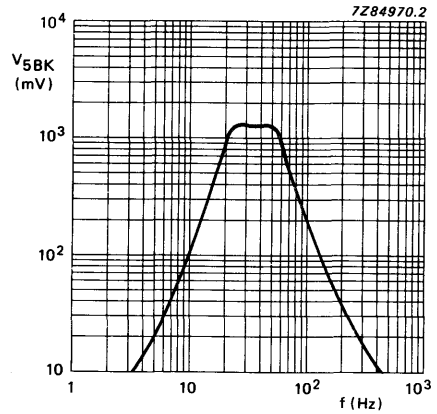


Fig. 2 BK signal voltage at pin 5 as a function of frequency.

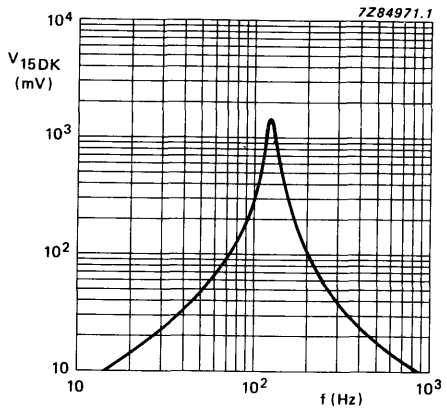


Fig. 3 DK signal voltage at pin 15 as a function of frequency: f_o = 125 Hz; Q ≈ 18.

APPLICATION INFORMATION (continued)

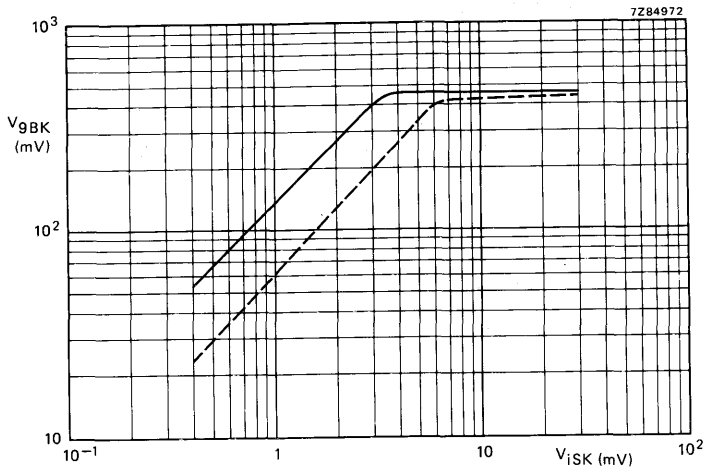


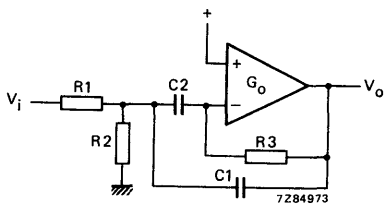
Fig. 4 Control characteristic of the SK amplifier at V_P = 8.5 V, m_{BK} = 60% and Q_L = 70.

FILTER INFORMATION

Gain

Amplifier conditions: $G_o >> G_v$ and $G_o >> 2 \cdot Q^2$

$$G_v = - \frac{\frac{p}{R1 \cdot C1}}{p^2 + p \frac{C1 + C2}{R3 \cdot C1 \cdot C2} + \frac{R1 + R2}{R1 \cdot R2 \cdot R3 \cdot C1 \cdot C2}}$$, in which $p = j\omega$ and $G_v = \frac{V_o}{V_i}$.



	general equation	C1 = C2 = C	C1 = C2 = C R2 << R1
Resonance frequency $\omega_r =$	$\frac{1}{\sqrt{\frac{R1 \cdot R2}{R1 + R2} \cdot R3 \cdot C1 \cdot C2}}$	$\frac{1}{C\sqrt{\frac{R1 \cdot R2}{R1 + R2} \cdot R3}}$	$\frac{1}{C\sqrt{R2 \cdot R3}}$
Gain at $\omega = \omega_r$ $-G_{vr} =$	$\frac{C2}{C1 + C2} \cdot \frac{R3}{R1}$	$\frac{1}{2} \cdot \frac{R3}{R1}$	$\frac{1}{2} \cdot \frac{R3}{R1}$
Quality $Q =$	$\sqrt{\frac{C1 \cdot C2}{C1 + C2}} \cdot \sqrt{\frac{R3\,(R1 + R2)}{R1 \cdot R2}}$	$\frac{1}{2}\sqrt{\frac{R3\,(R1 + R2)}{R1 \cdot R2}}$	$\frac{1}{2} \cdot \frac{R3}{R2}$

Recommended components

C1, C2 and R1, R2, R3	metallized polycarbonate film (MKC) capacitors; ± 5% metal film (MR) resistors; ± 2%
or	
C1, C2 and R1, R2, R3	metallized polyester film (MKT) capacitors; ± 5% carbon film (CR) resistors; ± 2%

TRAFFIC CONTROL MESSAGES AND WARNING TONE CIRCUIT

The TDA1589 is for evaluation of operating signals and logic control signals of a traffic control (TC) message decoder.

Features

- mute of non-traffic control stations
- restriction to traffic-control message reception
- LED display driver for MUTE indication
- control output for TC messages minimum volume
- delayed start of warning tone signal on failure of TC transmission. Also to be used to control a start of search tuning
- warning tone generator with automatic level control increasing volume in five steps
- interruption of cassette playback with motor stop during TC messages
- warning tone indicating failure of TC transmission also during cassette playback

QUICK REFERENCE DATA

Supply voltage (pin 10)	V_P		7,5 to 16 V
		typ.	8,5 V
Supply current	I_P	typ.	4,5 mA
Warning tone maximum voltage	$V_{o(p-p)}$	typ.	4,3 V
Output LED driver current (pin 3)	I_3	typ.	30 mA
motor stop current (pin 5)	I_5	typ.	30 mA
motor stop current (pin 6)	I_6	typ.	2 mA
MUTE display current (pin 8)	I_8	typ.	2 mA
start warning tone current (pin 13)	I_{13}	typ.	2 mA
Saturation voltage at output for minimum volume-on (pin 7)	$V_{7\,sat}$	<	0,1 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

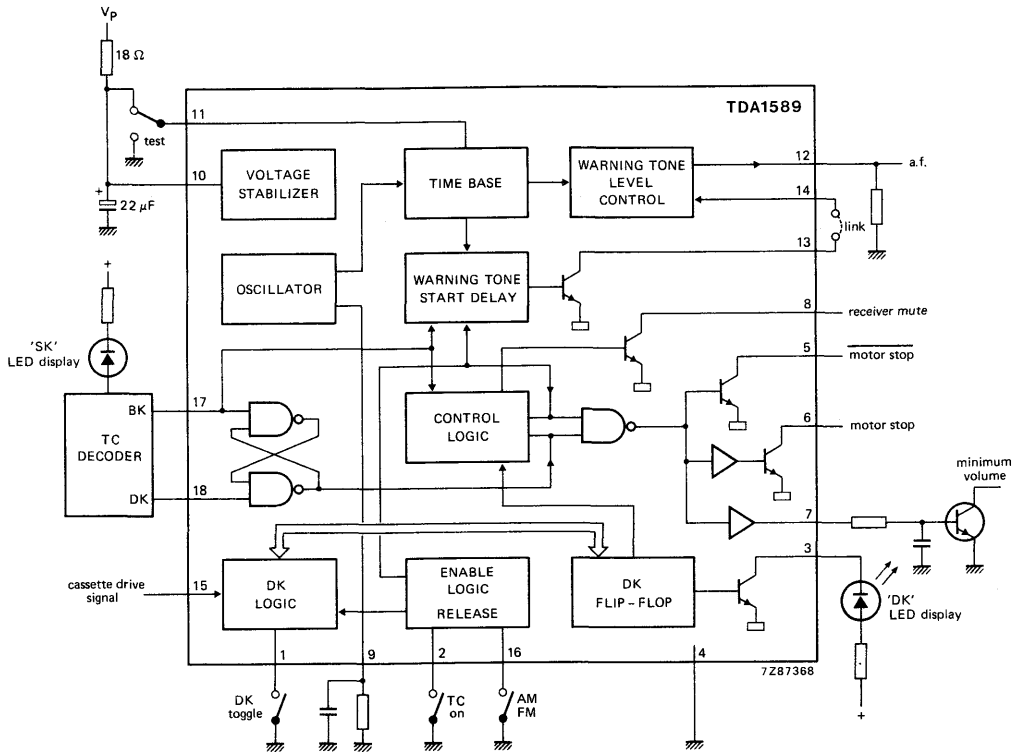
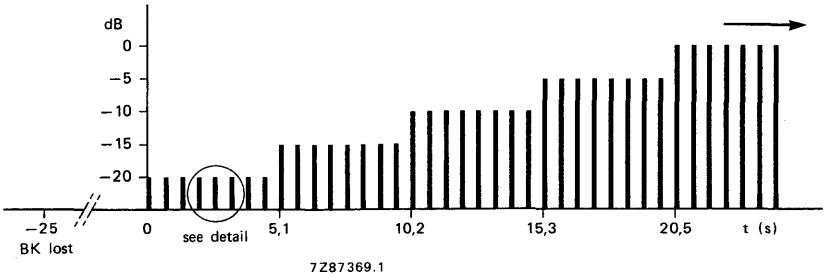


Fig. 1 Block diagram with external components; used as test circuit.

BK = TC area identification code (BereichsKennung)
DK = TC message identification code (DurchsageKennung)
SK = TC station identification code (SenderKennung)



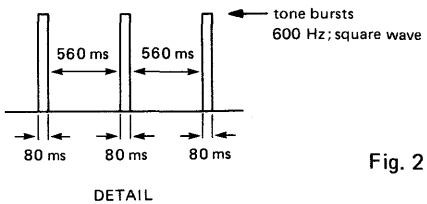


Fig. 2 Intermittent step pulse warning signal.

FUNCTIONAL DESCRIPTION

The automatic evaluation of traffic control signals is only possible during FM reception. The enable circuit will be active when pin 16 (FM on) is LOW. If traffic control messages are desired, pin 2 (TC on) must be switched to LOW.

FM radio mode

By operating the DK-toggle switch at pin 1 the DK flip-flop is set. This is displayed by a LED connected to pin 3. In the position "TC off" (pin 2 HIGH) it is not possible to set the DK flip-flop. Non-traffic control stations are muted. If a message is transmitted on the tuned TC station the minimum volume at pin 7 is exposed.

In case of BK-signal failure pin 13 changes to LOW after a delay of about 25 seconds. If pins 13 and 14 are then connected, an intermittent warning signal will be supplied at pin 12. The level increases automatically from −20 dB to 0 dB in 5 steps. (See Fig. 2.)

Cassette mode

If a TC message is delivered when TC is switched on (pin 16 and pin 2 LOW) and the DK flip-flop is set, the motor of the cassette player is stopped and the receiver automatically cuts in. The minimum volume is also set at the same time.

In case of BK-signal failure, the warning tone will be mixed into the cassette playback.

Protection

To avoid faulty switching, an internal latch will be set only if both DK (pin 18) and BK (pin 17) are HIGH. The latch will be reset if DK is changed to LOW independent of BK.

Reset of the DK-toggle flip-flop:
- by operating the DK-toggle (pin 1) twice
- by opening the TC-switch (pin 2)
- by switching to AM reception (pin 16)
- by switching off the cassette-player (pin 15)
- by switching power off or on.

Transmission monitoring

At reception failure of a TC-station BK at pin 17 will become LOW. After about 25 seconds the output (pin 13) will be set LOW to start the warning signal via the jumper between pins 13 and 14. In the meantime the search-tuning can also be started. The warning tone stage gives a graduated signal with a level increasing in five steps from −20 dB to 0 dB in about 20 seconds. The frequency of the warning signal is about 600 Hz; tone period ≈ 80 ms; pause ≈ 560 ms.

If now another TC-message transmitter has been tuned the input BK (pin 17) becomes HIGH and the warning tone is stopped. Also when switching TC-off (pin 2 HIGH) or switching to AM reception (pin 16 HIGH) the warning tone will stop. The BK-signal has to be stable for more than 1 second to reset the just started 25-second-timer.

mode	inputs pin numbers						outputs pin numbers					
	16	2	15	1	17	18	7	5	6	8	13	3
AM RADIO	H	X	X	X	X	X	H	H	L	H	H	H
FM RADIO TC off	L	H	X	X	X	X	H	H	L	H	H	H
FM-TC on station without TC	L	L	X	X	L	X	L	L	H	L	L*	L
FM-TC on station with BK	L	L	X	H	H	L	H	H	L	H	H	H
FM-TC on station with BK, DK	L	L	X	H	H	H	L	L	H	H	H	H
FM-TC on station with BK DK-toggle operated MUTE	L	L	X		H	L	H	H	L	L	H	↘
FM-TC on station with BK, DK incoming message	L	L	X	H	H	↗	↘	↘	↗	↗	H	L
FM-TC on station with BK DK-toggle operated twice	L	L	X	⊓	H	L	H	H	L	⊓	H	⊓
FM-TC on and cassette station with BK, DK cassette switched on	L	L	↗	X	H	H	L	L	H	H	H	H
FM-TC on and cassette station with BK cassette switched on	L	L	↗	X	H	L	H	H	L	H	H	H
FM-TC on and cassette station with BK cassette switched off	L	L	↘	X	H	L	H	H	L	↗	H	↗
function and state	AM/FM HIGH/LOW	TC on on = LOW	cassette off = H→L	DK toggle active = LOW	BK on = HIGH	DK on = HIGH	min. volume on = LOW	motor stop stop = LOW	motor stop stop = HIGH	MUTE on = LOW	warning tone on = LOW	DK display on = LOW

* After about 25 seconds.

Positive logic:
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
↗ = positive-going transition
↘ = negative-going transition

Functions of the control inputs

DK toggle operated chatter-proof by internal delay of 10 to 20 ms	pin 1	active	= LOW
TC (traffic control) released	pin 2	on	= LOW
Test condition clock rate 24 times faster	pin 11	on	= to ground
		off	= to V_P or open
Start warning signal	pin 14	on	= LOW
Reset of DK flip-flop by cassette player	pin 15	reset	= HIGH to LOW transition
Reset of DK flip-flop by tuning AM band	pin 16	reset	= HIGH
BK input*	pin 17	on	= HIGH
DK input*	pin 18	on	= HIGH
Minimum volume	pin 7	on	= LOW
Motor stop (30 mA)	pin 5	stop	= LOW
Motor stop (2 mA)	pin 6	stop	= HIGH
MUTE (volume off)	pin 8	on	= LOW
Warning tone	pin 13	on	= LOW
DK display	pin 3	on	= LOW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 10)	V_P	max.	16	V
Input voltages pins 1, 2, 11, 14, 15, 16, 17 and 18	V_i		0 to V_P	V
Output voltages pins 3, 5, 6, 8, 13	V_o	max.	23	V
Currents				
inputs 1, 2, 11, 14, 15, 16, 17 and 18	I_i	max.	10	mA
outputs 6, 8, 13	I_o	max.	10	mA
outputs 3 and 5	I_o	max.	50	mA
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 80	°C

* Open collector output of TC-decoder.

CHARACTERISTICS

V_P typ. 8,5 V; T_{amb} = 25 °C; unless otherwise specified (see Fig. 1)

Supply voltage range	V_P	7,5 to 16	V
Supply current	I_P	typ. 4,5 < 6	mA mA

Control inputs

Pins 1, 2, 11, 14, 15, 16, 17 and 18

Input voltage HIGH	V_{IH}	3,5 V to V_P	
Input voltage LOW	V_{IL}	< 2	V
Input current HIGH V_i = 16 V	I_{IH}	< 1	μA
Input current LOW V_i = 0 V	$-I_{IL}$	25 to 200	μA
Input resistance V_i = 0 V	R_i	< 10	kΩ

Control outputs

DK-LED display and $\overline{\text{motor stop}}$ open collector outputs 3 and 5

Output voltage LOW I_{OL} = 20 mA	V_{OL}	typ. 1 < 1,5	V V
Output current LOW	I_{OL}	typ. 30	mA
Output voltage HIGH (open collector) I_{OH} < 10 μA	V_{OH}	< 23	V

LF-MUTE, motor stop and warning signal start pins 8, 6 and 13

Output voltage LOW I_{OL} = 1 mA	V_{OL}	< 0,35	V
Output current LOW	I_{OL}	= 2	mA
Output voltage HIGH (open collector) I_{OH} < 1 μA	V_{OH}	= 16	V

Minimum voltage (pin 7) (R_S = 800 Ω, R_L = ∞)

Output voltage LOW (for volume HIGH)	$V_{7\text{-}4}$	< 0,1	V
Output voltage HIGH (for volume LOW)	$V_{7\text{-}4}$	typ. 5	V

Warning signal (pin 12)

f = 600 Hz; square-wave pulsed; R_S = 300 Ω

Switching time on	t_{on}	typ. 80	ms
Switching time off	t_{ogf}	typ. 560	ms
Output voltage during t_{on} at maximum peak (R_L = 1 kΩ)	$V_{12\text{-}4}$	typ. 4,3	V
during T_{off}	$V_{12\text{-}4}$	typ. 0	V

Automatic level control			
Duration per level	t_p	typ. 5	s
Output level swing (in 5 steps)	ΔV_{12-4}	−20 to 0	dB
Output current peak value	$-I_{12M}$	typ. 6	mA
Oscillator (pin 9)			
Frequency	f	typ. 2400	Hz
Filter resistance	R_o	typ. 100	kΩ
Filter capacitance	C_o	typ. 4,7	nF
Oscillator frequency tolerance	$\Delta f/f$	−10 to + 10	%

IF AMPLIFIER/DEMODULATOR FOR FM RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1596 provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for both mono and stereo reception. It may also be applied to common front-ends, stereo decoders and AM receiver circuits.

Features

- Simulates behaviour of a ratio detector (internal field strength and detuning-dependent voltage for dynamic AF signal muting)
- Mono/stereo blend and field strength indication control voltage
- Three-state mode switch for FM, mute-on / FM, mute-off / FM-off
- Internal compensation of AF signal total harmonic distortion (THD)
- Two open collector stop pulse outputs for microcomputer tuning control (can be one stop pulse output by wired-ANDing)
- Internal reference voltage source
- Built-in hum and ripple rejection circuits

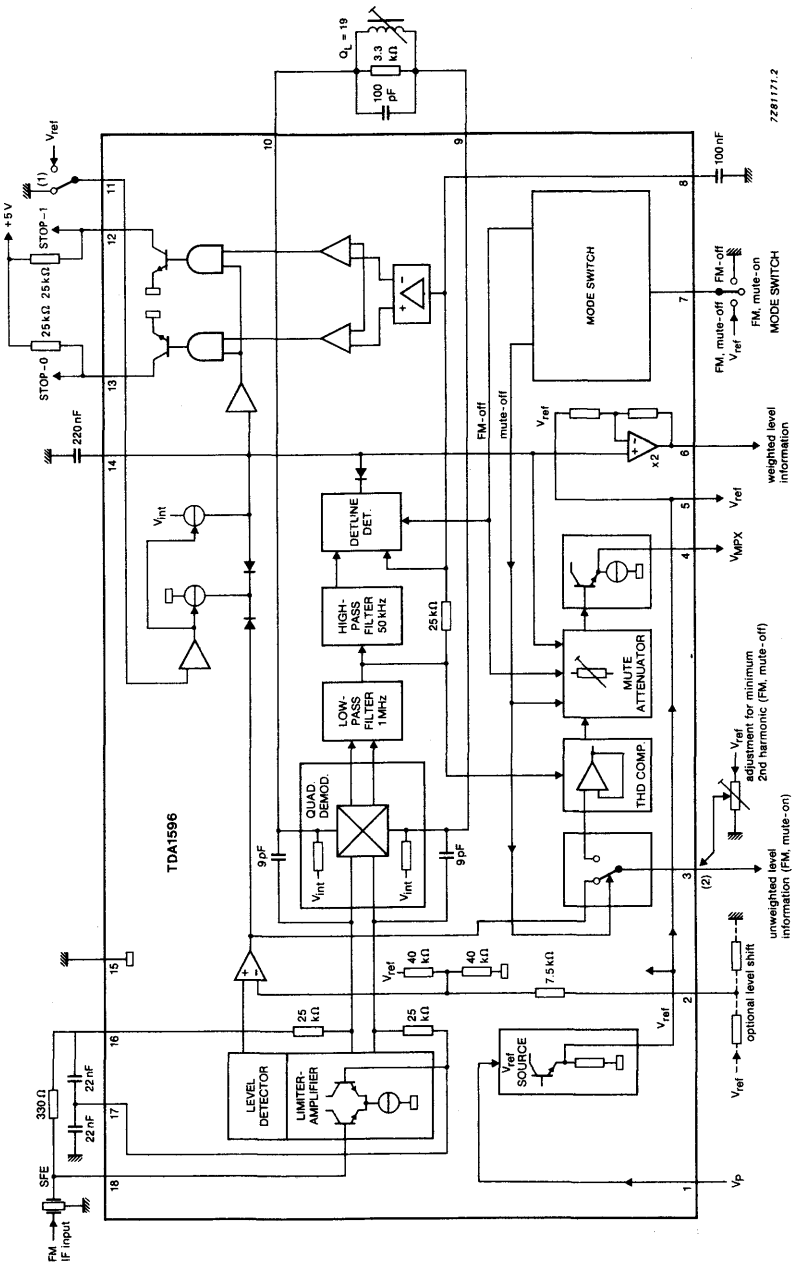
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 1)		V_P	7.5	8.5	12.0	V
Supply current (pin 1)	V_P = 8.5 V; $I_2 = I_7$ = 0 mA	I_P	–	20	26	mA
AF output voltage (RMS value)	$V_{18(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Signal-to-noise ratio	$V_{18(rms)}$ = 10 mV; f_m = 400 Hz; Δf = 75 kHz	S/N	–	82	–	dB
Total harmonic distortion	$V_{18(rms)}$ = 10 mV; f_m = 1 kHz; I_7 = 0 mA; Δf = 75 kHz; FM mute on; without de-emphasis; without detuning	THD	–	0.1	0.3	%
Operating ambient temperature range		T_{amb}	−40	–	+ 85	°C

SEE ALSO DATA SHEET FOR TDA1596T

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Two different time constants can be chosen for the multipath detection network by connecting pin 11 to ground or to V_{ref}.
(2) In the FM, mute-on condition the unweighted level detector output is available from pin 3. In the FM, mute-off condition the variable resistor at pin 3 can be adjusted for minimum 2nd harmonic distortion at pin 4.

Fig. 1 Block diagram and application circuit.

PINNING

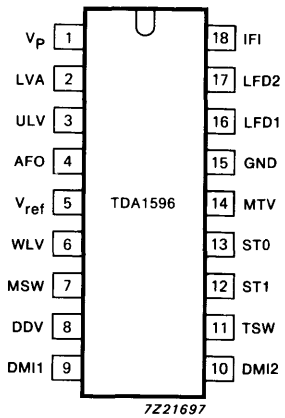


Fig. 2 Pinning diagram.

1	V_P	supply voltage
2	LVA	level voltage adjustment
3	ULV	unweighted level output/K2 adjustment
4	AF0	AF output
5	V_{ref}	reference voltage output
6	WLV	weighted level voltage output
7	MSW	mode switch
8	DDV	detune detector voltage
9	DMI1	demodulator input 1
10	DMI2	demodulator input 2
11	TSW	tau switch
12	ST1	stop pulse output 1
13	ST0	stop pulse output 0
14	MTV	mute voltage
15	GND	ground
16	LFD1	IF limiter feedback 1
17	LFD2	IF limiter feedback 2
18	IFI	IF input

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Limiter-amplifier

This has five stages of IF amplification using balanced differential limiter-amplifiers with emitter-follower coupling. Decoupling of the stages from the voltage supply lines and an internal high-ohmic DC feed-back loop give a very stable IF performance. The amplifier gain is virtually independent from temperature changes.

FM demodulator

The demodulator is fully balanced and comprises two cross-coupled differential amplifiers. Quadrature detection of the FM signal is performed by feeding one differential amplifier directly from the limiter-amplifier output, and the other via an external 90° phase-shifting network. The demodulator has good stability and its zero cross-over shift is small. The bandwidth of the demodulator output is restricted to approximately 1 MHz by an internal low-pass filter.

THD compensation

This circuit compensates non-linearities introduced by demodulation. For this to operate correctly the demodulator circuit between pins 9 and 10 must have a loaded Q-factor of 19. Consequently there is no need for the demodulator tuned circuit to be adjusted for minimum THD, instead the adjustment criterium is for a symmetrical stop pulse.

Mute attenuator and AF output

The control voltage for the mute attenuator at pin 14 is generated from the values of the level detector and the detuning detector outputs. The mute attenuator has a fast attack and a slow decay which is determined by the capacitor at pin 14. The AF signal is passed via the mute attenuator to the output at pin 4.

A weighted control voltage, available from pin 6, is obtained from the mute attenuator control voltage via a buffer-amplifier which introduces an additional voltage shift and gain.

Level detector

The level detector generates a voltage output which is proportional to the field strength of the input signal. The unweighted level detector output is available when the mode switch is operating in the FM, mute-on condition.

Tuning-stop outputs

The open collector outputs STOP-0 and STOP-1 (from pins 13 and 12 respectively) are voltages derived from the detuning level and the field strength of the input signal. If only one tuning-stop output is required, pins 12 and 13 may be tied together.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 1)	$V_P = V_{1-15}$	−0.3	+ 16	V
Reference voltage range (pin 5)	V_{5-15}	−0.3	+ 10	V
Level adjustment range (pin 2)	V_{2-15}	−0.3	+ 10	V
Mode switch voltage range (pin 7)	V_{7-15}	−0.3	+ 16	V
Control input voltage range (pin 11)	V_{11-15}	−0.3	+ 6	V
THD compensation/unweighted field strength voltage range (pin 3)	V_{3-15}	−0.3	+ 16	V
Tuning-stop output voltage range				
STOP-0 (pin 13)	V_{13-15}	−0.3	+ 16	V
STOP-1 (pin 12)	V_{12-15}	−0.3	+ 16	V
Tuning-stop output current				
STOP-0 (pin 13)	I_{13}	−	2	mA
STOP-1 (pin 12)	I_{12}	−	2	mA
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Electrostatic handling*				
all pins except pins 5 and 6	V_{es}	−2000	+ 2000	V
pin 5	V_{es}	−2000	+ 900	V
pin 6	V_{es}	−2000	+ 1600	V

DEVELOPMENT DATA

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

f = 10.7 MHz; $V_P = V_{1-15} = 8.5$ V; $V_I = V_{18(rms)} = 1$ mV; $T_{amb} = 25$ °C; measured in the circuit of Fig. 3; tuned circuit at pins 9, 10 aligned for symmetrical stop pulses; all voltages are referred to ground (pin 15); unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	$V_P = V_1$	7.5	8.5	12.0	V
Supply current at $I_2 = I_7 = 0$ mA	I_1	–	20	26	mA
FM demodulator					
Input impedance	R_{9-10}	25	40	55	kΩ
	C_{9-10}	–	6	–	pF
DC output voltage (no-signal condition) at $V_{9, 10(p-p)} \leqslant 100\ \mu V$; $V_{18(rms)} \leqslant 5\ \mu V$	V_4	2.75	3.10	3.45	V
Output impedance	R_{4-15}	–	400	–	Ω
Mute attenuator control voltage					
Control voltage (pin 14)					
at $V_{18(rms)} \leqslant 5\ \mu V$	V_{14}	–	2.0	–	V
at $V_{18(rms)} = 1$ mV	V_{14}	–	3.45	–	V
Output impedance (pin 14)	R_{14-15}	–	–	2.0	MΩ
Level shift input (pin 2)					
internal bias voltage at $I_2 = 0$ mA	V_2	–	1.4	–	V
input impedance	R_{2-15}	15	–	–	kΩ
Internal muting (Fig. 4)					
Internal attenuation of signals ± 22.5 kHz $\leqslant$ detuning $\leqslant \pm 80$ kHz $A = 20\log[\Delta V_4(\text{FM mute-off})/\Delta V_4(\text{FM})]$					
at $V_{14} \geqslant 1\ V_5$	A	–	0	–	dB
at $V_{14} = 0.77\ V_5$	A	1.5	3.0	4.5	dB
at $V_{14} = 0.55\ V_5$	A	–	20	–	dB

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Attack and decay times (pin 14)					
Pin 11 connected to ground					
charge current	$+I_{14}$	–	8	–	μA
discharge current	$-I_{14}$	–	120	–	μA
Pin 11 connected to V_{ref}					
charge current	$+I_{14}$	–	100	–	μA
discharge current	$-I_{14}$	–	120	–	μA
Level detector					
Dependence of output voltage on temperature	$\frac{\Delta V_6}{V_6 \Delta T}$	–	3.3	–	mV/VK
Output impedance	R_6	–	–	500	Ω
Dependence of output voltage (pin 6) on input voltage (pin 18) (Fig. 5):					
$V_{18(rms)} \leqslant 5$ μV; $I_2 = I_7 = 0$ mA	V_6	0.1	0.7	1.3	V
$V_{18(rms)} = 1$ mV; $I_2 = I_7 = 0$ mA	V_6	3.0	3.6	4.2	V
Slope of output voltage (pin 6) for input voltage range $V_{18(rms)} \geqslant 50$ μV to $V_{18(rms)} \leqslant 50$ mV	$\frac{\Delta V_6}{20 \Delta \log V_{18}}$	1.4	1.7	2.0	V/20 dB
Dependence of output voltage (pin 6) on detuning (Fig. 6) at input voltage $V_{18(rms)} = 10$ mV:					
detuning $\leqslant \pm 45$ kHz	ΔV_6	–	–	0.2	V
detuning = for $V_6 = 1.8$ V	$\pm \Delta f$	90	–	160	kHz
detuning = ± 200 kHz	V_6	0.5	0.7	0.9	V
Slope of output voltage with detuning = 125 ± 20 kHz at $V_{18(rms)} = 10$ mV	$\lvert \Delta V_6 / \Delta f \rvert$	–	35	–	mV/kHz
Level shift control (pin 2) (Fig. 7)					
adjustment range	$\pm \Delta V_6$	1.6	2.0	–	V
adjustment gain	$-(\Delta V_6 / \Delta V_2)$	–	1.7	–	V
output voltage at $V_2 = V_5$; $V_{18(rms)} \leqslant 5$ μV	V_6	–	–	0.3	V
Low-pass filter at pin 8					
Output voltage at $I_7 = 0$ mA; $V_{18(rms)} \leqslant 5$ μV	V_8	–	2.2	–	V
Internal resistance	$R_{8(int)}$	12	25	50	kΩ

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning-stop detector (Figs 8 and 9)					
Stop-0: detuning at $V_{18(rms)}$ = 10 mV					
for $V_{13} \geq 3.5$ V	$+\Delta f$	–	–	10	kHz
for $V_{13} \leq 0.3$ V	$+\Delta f$	18	–	–	kHz
Stop-1: detuning at $V_{18(rms)}$ = 10 mV					
for $V_{12} \geq 3.5$ V	$-\Delta f$	–	–	10	kHz
for $V_{12} \leq 0.3$ V	$-\Delta f$	18	–	–	kHz
Dependence of STOP-0, STOP-1 on input voltage (pin 18)					
input voltage (RMS value) for $V_{12} = V_{13} \geq 3.5$ V	$V_{18(rms)}$	250	–	–	μV
input voltage (RMS value) for $V_{12} = V_{13} \leq 0.3$ V	$V_{18(rms)}$	–	–	50	μV
Output voltage when $I_{12} = I_{13}$ = 1 mA	$V_{12, 13}$	–	–	0.3	V
Mode switch and pin 3 (Fig. 10)					
FM-off position					
Control voltage for 60 dB muting depth	V_7	–	–	1.4	V
FM, mute-on position (pin 3 = output)					
Internal bias voltage at $R_{7\text{-}15} \geq 10$ MΩ	V_7	–	2.8	–	V
Input current	$\|I_7\|$	–	–	2.5	μA
Output voltage with $R_{3\text{-}15}$ = 10 kΩ; $C_{3\text{-}15} \geq 1$ nF*	V_3	–	2	–	V
Output impedance for $V_{18} = \leq 5\ \mu$V; $I_3 = 500\ \mu$A	$R_{3\text{-}15}$	–	–	100	Ω
FM, mute-off position (pin 3 = input)					
Control voltage	V_7	$0.9\ V_5$	–	–	V
Input current at $V_7 = V_5$	I_7	–	–	15	μA
Input resistance	$R_{3\text{-}15}$	1	–	–	MΩ
Reference voltage source					
Output voltage at $I_5 = -1$ mA	V_5	3.3	3.7	4.1	V
Output impedance at $I_5 = -1$ mA	$\Delta V_5/\Delta I_5$	–	40	80	Ω
Temperature coefficient	TC	–	3.3	–	mV/K

* Without input voltage.

OPERATING CHARACTERISTICS

f = 10.7 MHz; $V_{18(rms)}$ = 1 mV; deviation (Δf) = 22.5 kHz; modulation frequency (f_m) = 400 Hz; de-emphasis (pin 4) = 50 μs; test circuit as per Fig. 3; tuned circuit (Q_L = 19) aligned for symmetrical stop pulses; T_{amb} = + 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
AF output voltage (RMS value) at $V_{18(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Start of limiting (FM, mute-off); (RMS value) (Fig. 11)	$V_{18(rms)}$	14	22	35	μV
Dependence of signal-to-noise ratio (in noise frequency band 250 Hz to 15 kHz, unweighted) on input voltage					
for S/N = 26 dB	$V_{18(rms)}$	–	15	–	μV
for S/N = 46 dB	$V_{18(rms)}$	–	60	–	μV
at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz	S/N	–	82	–	dB
THD (FM, mute-on) at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; without detuning; without de-emphasis; I_7 = 0 mA	THD	–	0.1	0.3	%
Dynamic mute attenuation (Fig. 12) $\alpha_D = 20\log \frac{V_4 \text{ (FM mute-off)}}{V_4 \text{ (FM, mute-on)}}$ with f_m = 100 kHz; Δf = 75 kHz	α_D	–	16	–	dB
Slope of attenuation curve	$\alpha_D \Delta f$	–	0.8	–	dB/kHz
THD (FM, mute-on) at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; detuning $\leqslant \pm$ 25 kHz without de-emphasis; I_7 = 0 mA (Fig. 13)	THD	–	–	0.6	%
THD (FM, mute-off and compensated via pin 3) at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; $V_7 = V_5$	THD	–	0.07	0.25	%
Voltage range at pin 3 for THD compensation	V_3	0	–	V_5	V
AM suppression (FM, mute-off) with amplitude modulation at 30%; input voltage range V_{18} = 300 μV to 100 mV (Fig. 14)		–	65	–	dB
Power supply ripple rejection = 20log [$\Delta V_1/\Delta V_4$]		33	36	–	dB
Mute attenuation (FM-off) = 20log [$V_{4(FM\text{-}on}/V_{4(FM\text{-}off)}$]		60	–	–	dB

DEVELOPMENT DATA

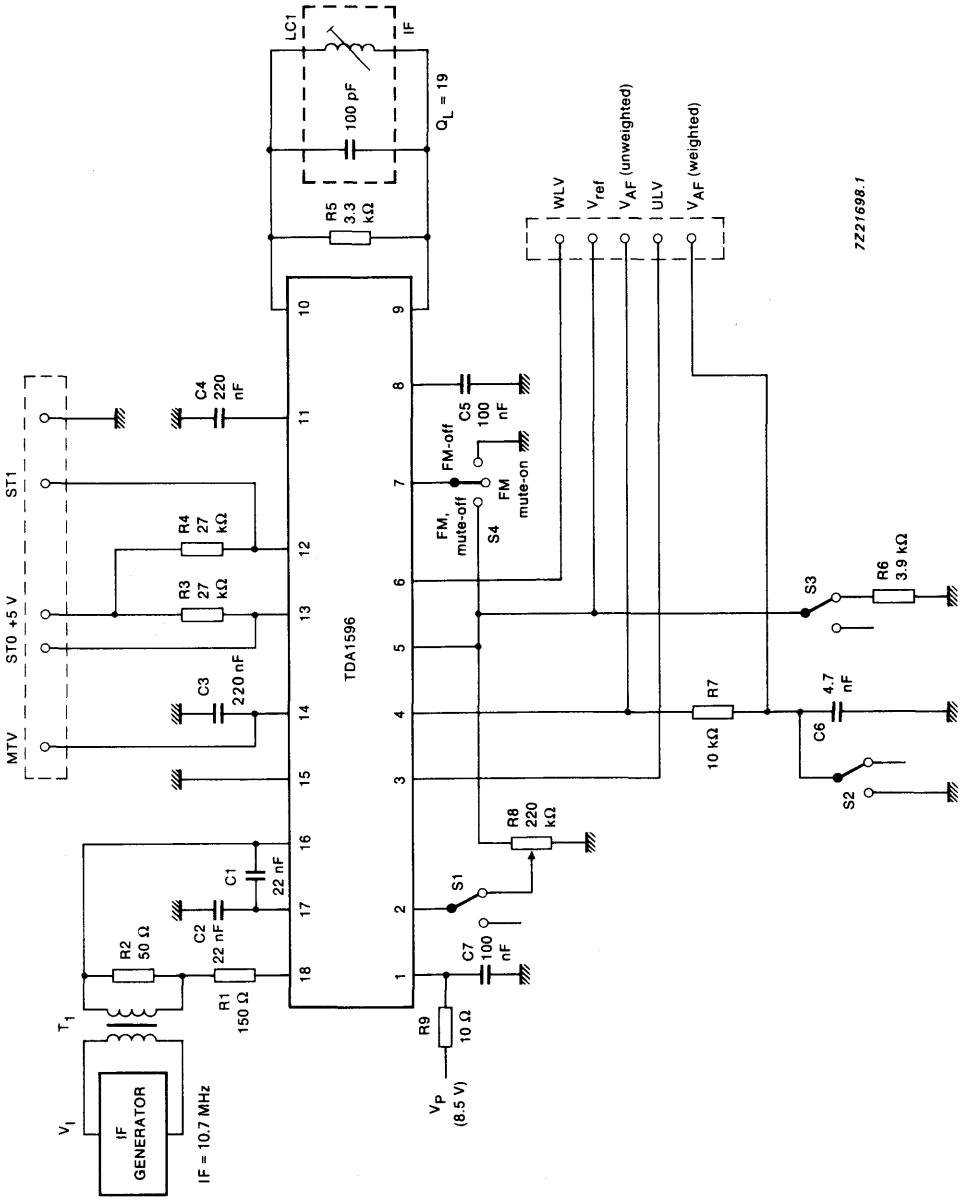


Fig. 3 Test circuit.

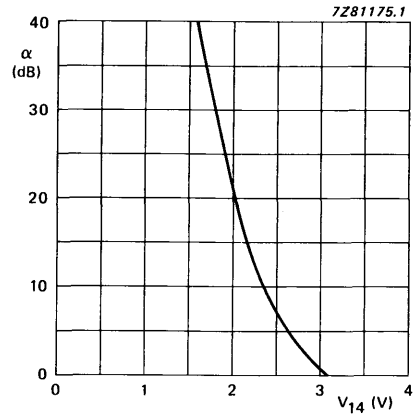


Fig. 4 Typical curve of internal attenuation showing the relationship between the mute attenuator control voltage (pin 14) and mute attenuation, $I_2 = I_7 = 0$ mA.

DEVELOPMENT DATA

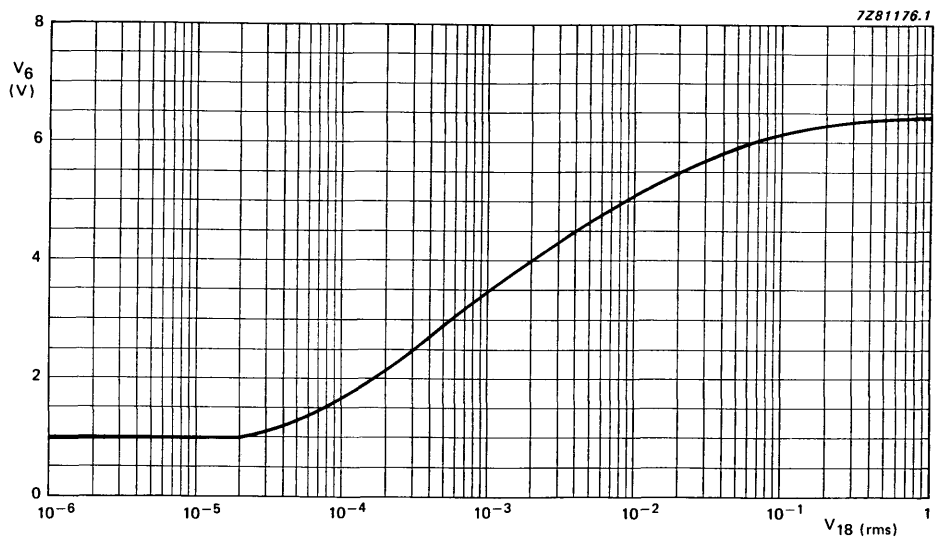


Fig. 5 Weighted field strength output voltage (pin 6) as a function of input voltage (pin 18); $R_{6\text{-}15} \geqslant 10$ kΩ; $I_2 = I_7 = 0$ mA.

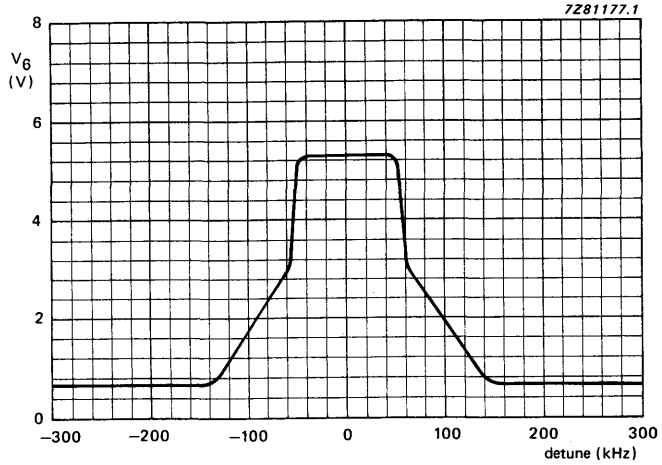


Fig. 6 Weighted field strength output voltage (pin 6) as a function of detuning; $R_{6\text{-}15} \geqslant 10\ k\Omega$; $I_2 = I_7 = 0\ mA$; $V_{18} = 10\ mV$.

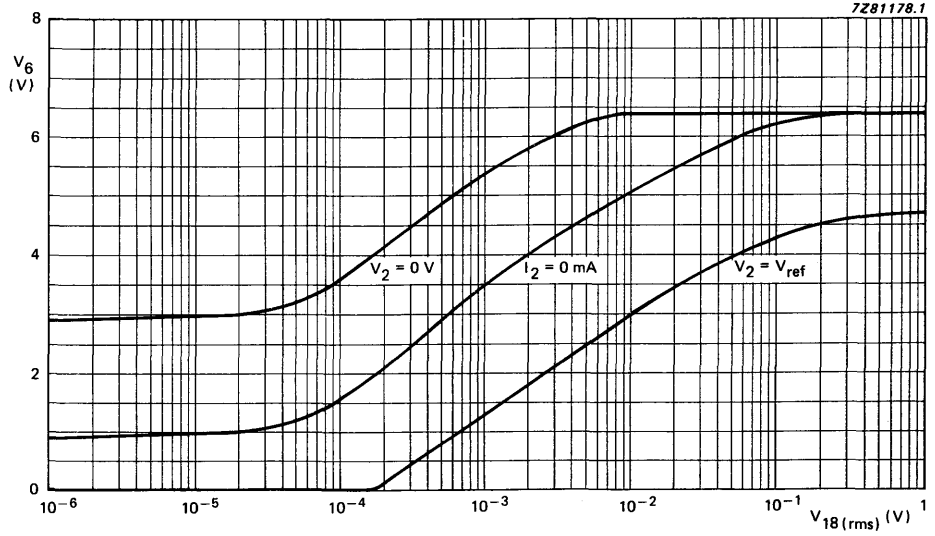
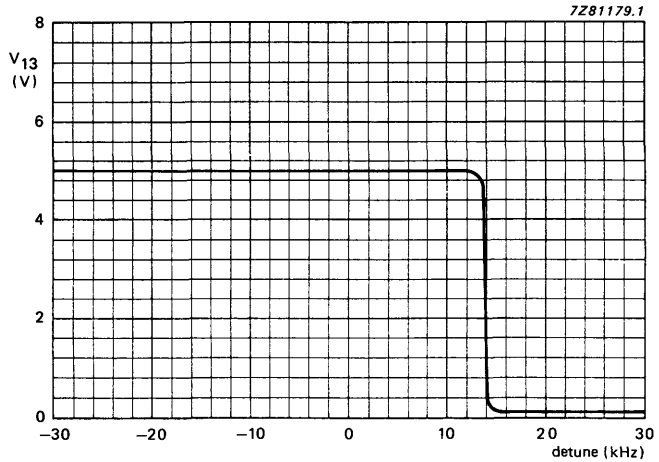
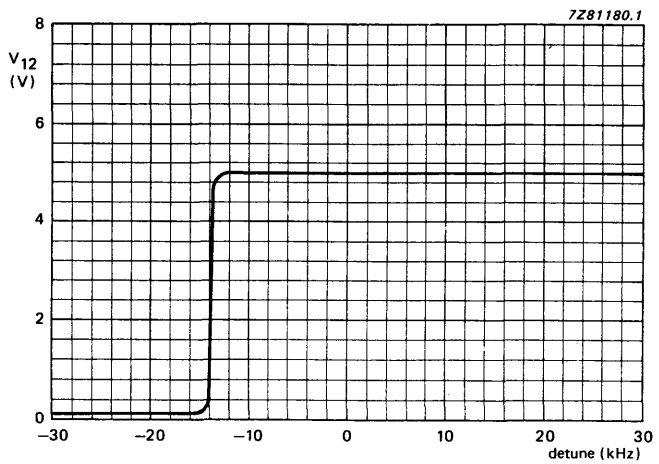


Fig. 7 Adjustment range of weighted field strength output voltage (pin 6) with level shift control (pin 2); $R_{6\text{-}15} \geqslant 10\ k\Omega$; $I_7 = 0\ mA$.



(a) STOP-0.



(b) STOP-1

Fig. 8 STOP-0 and STOP-1 output voltages as a function of detuning, measured at V_{18} = 10 mV.

DEVELOPMENT DATA

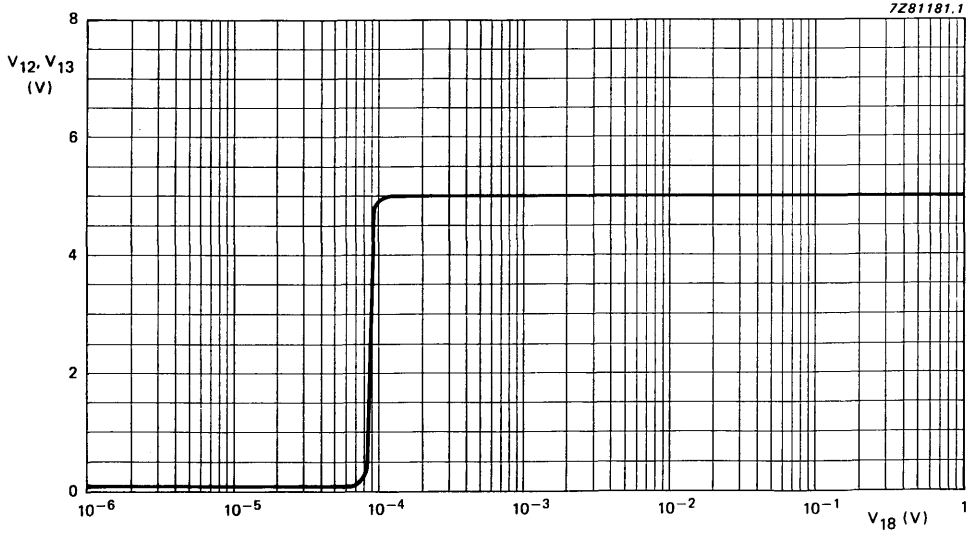


Fig. 9 STOP-0 or STOP-1 output voltages as a function of input voltage at pin 18.

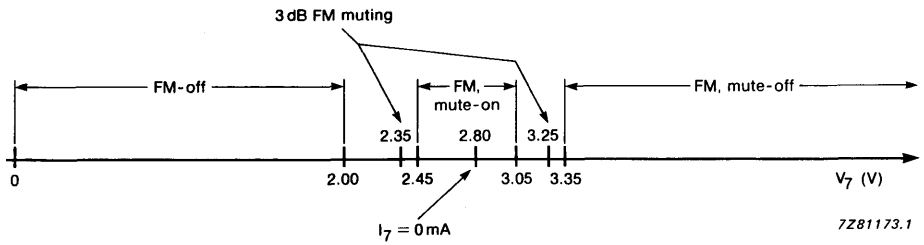
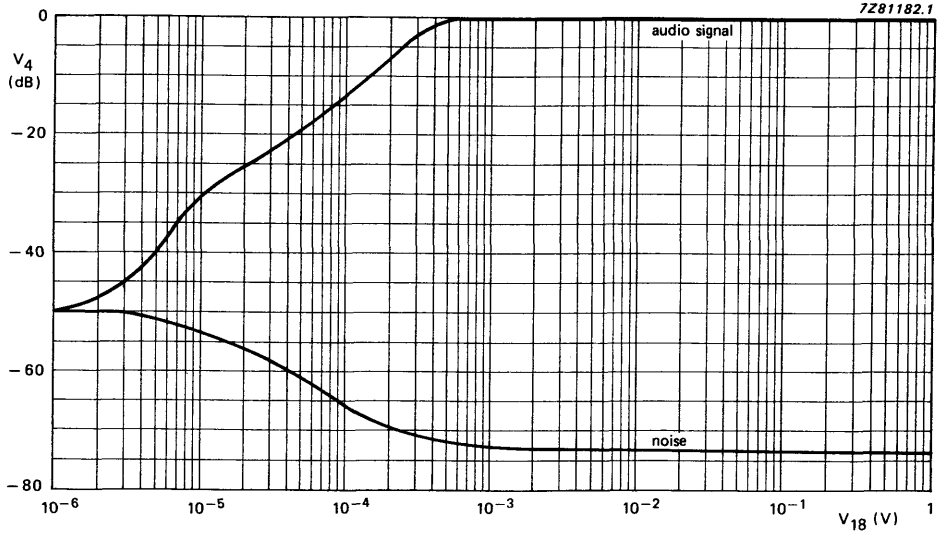
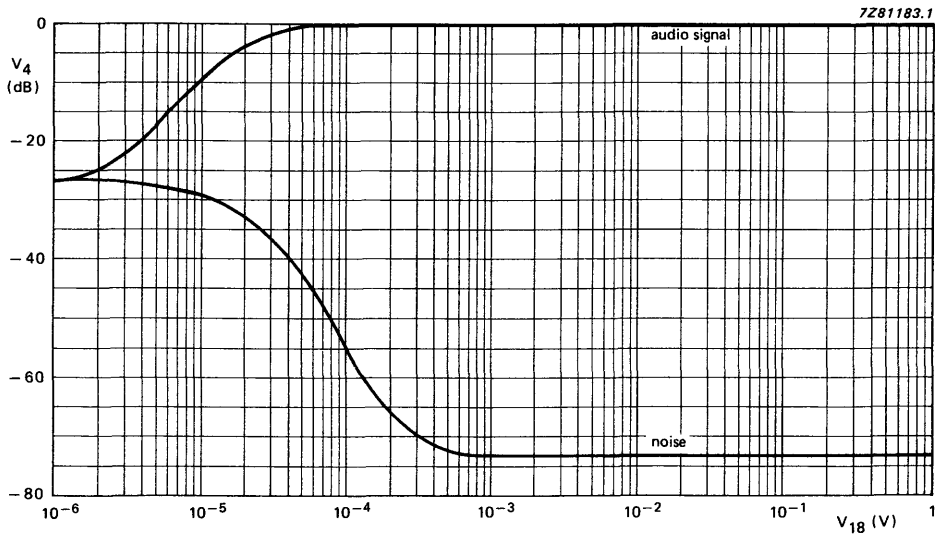


Fig. 10 Switch levels at pin 7.



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 11 Audio signal (Δf = 22.5 kHz; f_m = 1 kHz) and noise as functions of input voltage at pin 18; measured with 50 μs de-emphasis.

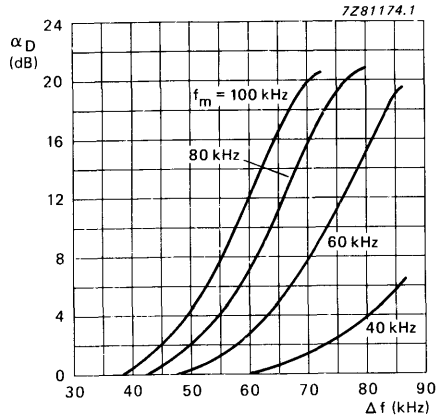


Fig. 12 Dynamic mute attenuation as a function of frequency deviation for modulation frequencies of 40, 60, 80 and 100 kHz.

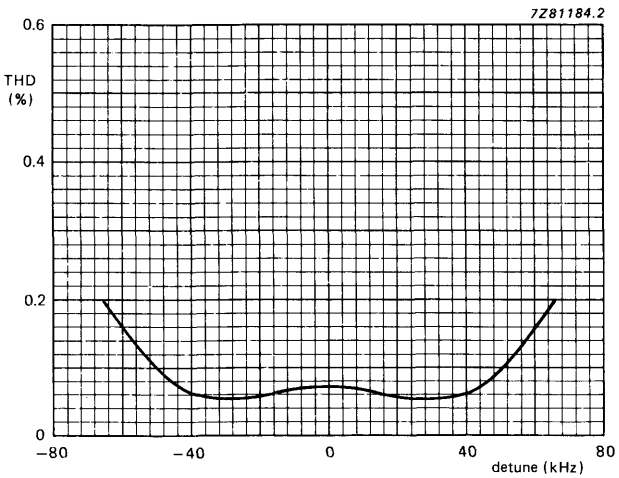
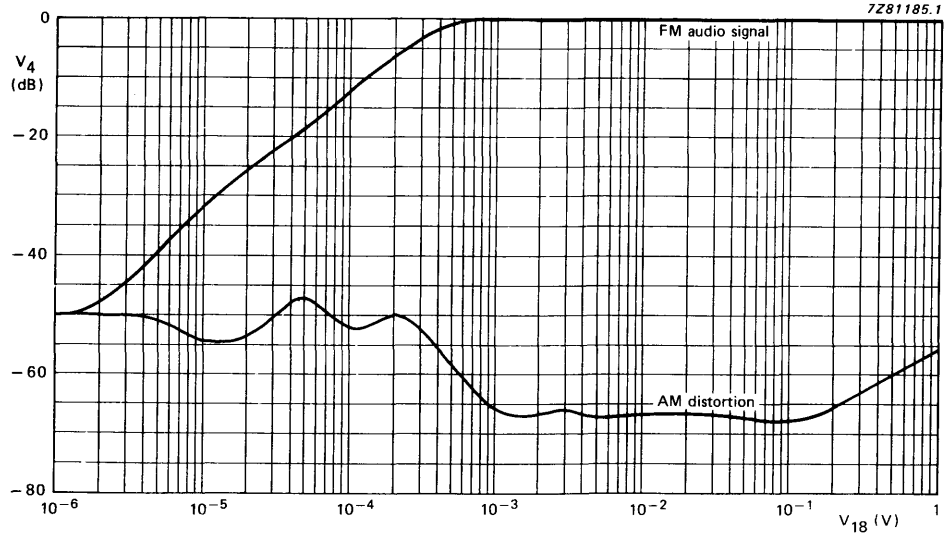
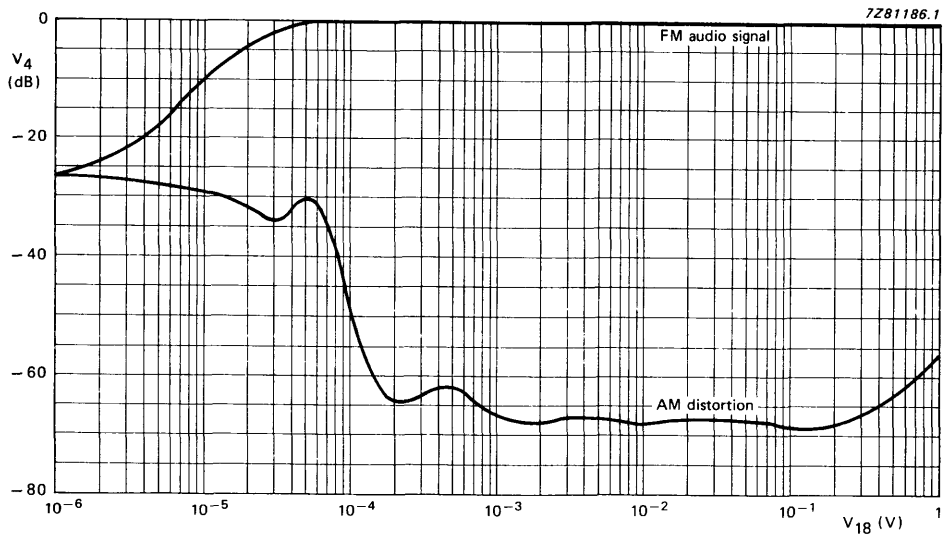


Fig. 13 THD as a function of detuning; mode switch at FM, mute-on position; Δf = 75 kHz; f_m = 1 kHz; $V_{18(rms)}$ = 10 mV.



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 14 Typical curves showing AM suppression for an input signal having frequency modulation at Δf = 22.5 kHz and f_m = 1 kHz, and amplitude modulation of 30% at a frequency of 400 Hz; de-emphasis time = 50 μs and bandwidth = 250 Hz to 15 kHz.

IF AMPLIFIER/DEMODULATOR FOR FM RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1596T provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for both mono and stereo reception. It may also be applied to common front-ends, stereo decoders and AM receiver circuits.

Features

- Simulates behaviour of a ratio detector (internal field strength and detuning-dependent voltage for dynamic AF signal muting)
- Mono/stereo blend and field strength indication control voltage
- Three-state mode switch for FM, mute-on / FM, mute-off / FM-off
- Internal compensation of AF signal total harmonic distortion (THD)
- Two open collector stop pulse outputs for microcomputer tuning control (can be one stop pulse output by wired-ANDing)
- Internal reference voltage source
- Built-in hum and ripple rejection circuits

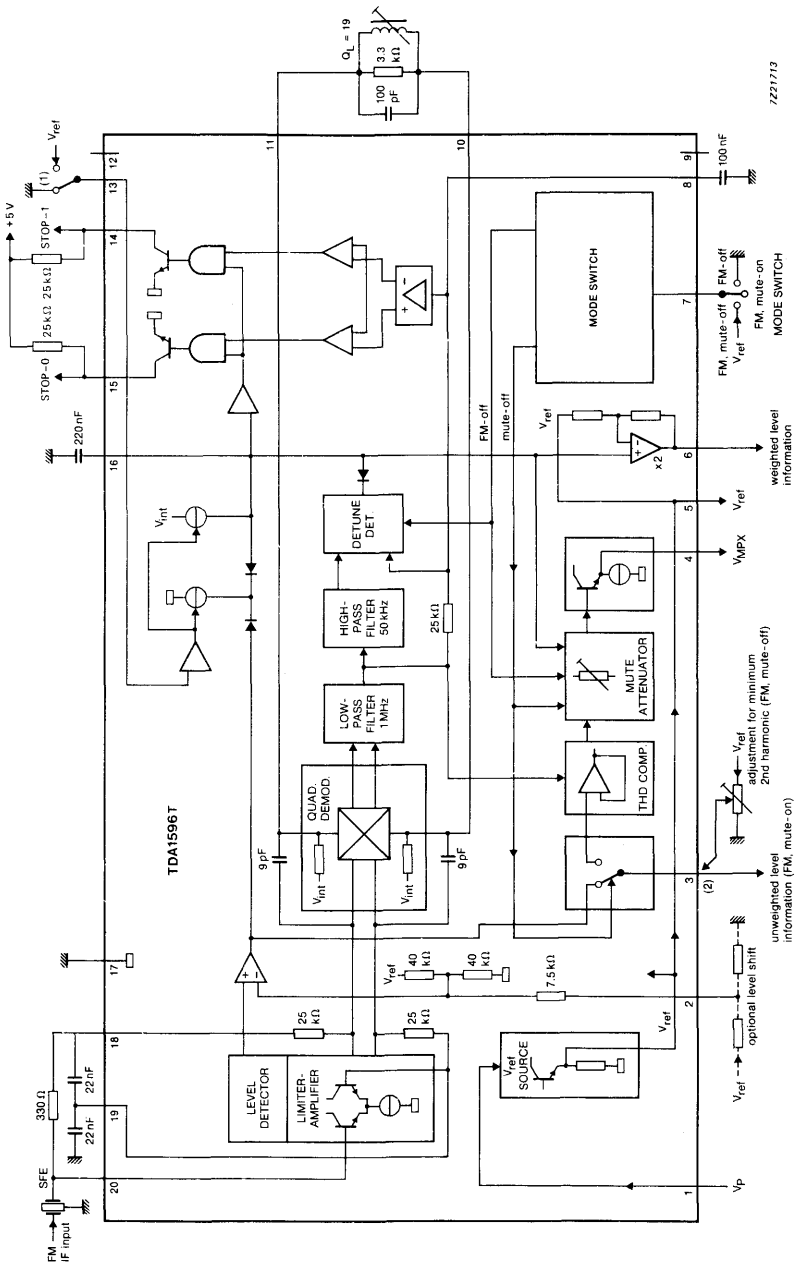
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 1)		V_P	7.5	8.5	12.0	V
Supply current (pin 1)	V_P = 8.5 V; $I_2 = I_7$ = 0 mA	I_P	–	20	26	mA
AF output voltage (RMS value)	$V_{20(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Signal-to-noise ratio	$V_{20(rms)}$ = 10 mV; f_m = 400 Hz; Δf = 75 kHz	S/N	–	82	–	dB
Total harmonic distortion	$V_{20(rms)}$ = 10 mV; f_m = 1 kHz; I_7 = 0 mA; Δf = 75 kHz; FM mute on; without de-emphasis; without detuning	THD	–	0.1	0.3	%
Operating ambient temperature range		T_{amb}	−40	–	+ 85	°C

SEE ALSO DATA SHEET FOR TDA1596

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).



(1) Two different time constants can be chosen for the multipath detection network by connecting pin 13 to ground or to V_{ref}.
(2) In the FM, mute-on condition the unweighted level detector output is available from pin 3. In the FM, mute-off condition the variable resistor at pin 3 can be adjusted for minimum 2nd harmonic distortion at pin 4.

Fig. 1 Block diagram and application circuit.

DEVELOPMENT DATA

PINNING

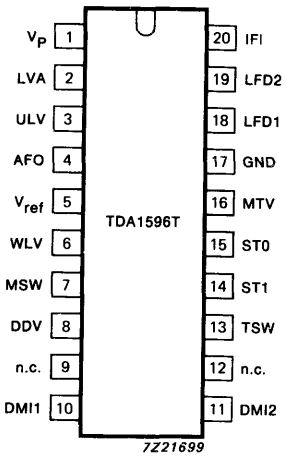


Fig. 2 Pinning diagram.

1	V_P	supply voltage
2	LVA	level voltage adjustment
3	ULV	unweighted level output/K2 adjustment
4	AF0	AF output
5	V_{ref}	reference voltage output
6	WLV	weighted level voltage output
7	MSW	mode switch
8	DDV	detune detector voltage
9	n.c.	not connected
10	DMI1	demodulator input 1
11	DMI2	demodulator input 2
12	n.c.	not connected
13	TSW	tau switch
14	ST1	stop pulse output 1
15	ST0	stop pulse output 0
16	MTV	mute voltage
17	GND	ground
18	LFD1	IF limiter feedback 1
19	LFD2	IF limiter feedback 2
20	IFI	IF input

FUNCTIONAL DESCRIPTION

Limiter-amplifier

This has five stages of IF amplification using balanced differential limiter-amplifiers with emitter-follower coupling. Decoupling of the stages from the voltage supply lines and an internal high-ohmic DC feed-back loop give a very stable IF performance. The amplifier gain is virtually independent from temperature changes.

FM demodulator

The demodulator is fully balanced and comprises two cross-coupled differential amplifiers. Quadrature detection of the FM signal is performed by feeding one differential amplifier directly from the limiter-amplifier output, and the other via an external 90° phase-shifting network. The demodulator has good stability and its zero cross-over shift is small. The bandwidth of the demodulator output is restricted to approximately 1 MHz by an internal low-pass filter.

THD compensation

This circuit compensates non-linearities introduced by demodulation. For this to operate correctly the demodulator circuit between pins 10 and 11 must have a loaded Q-factor of 19. Consequently there is no need for the demodulator tuned circuit to be adjusted for minimum THD, instead the adjustment criterium is for a symmetrical stop pulse.

Mute attenuator and AF output

The control voltage for the mute attenuator at pin 16 is generated from the values of the level detector and the detuning detector outputs. The mute attenuator has a fast attack and a slow decay which is determined by the capacitor at pin 16. The AF signal is passed via the mute attenuator to the output at pin 4.

A weighted control voltage, available from pin 6, is obtained from the mute attenuator control voltage via a buffer-amplifier which introduces an additional voltage shift and gain.

Level detector

The level detector generates a voltage output which is proportional to the field strength of the input signal. The unweighted level detector output is available when the mode switch is operating in the FM, mute-on condition.

Tuning-stop outputs

The open collector outputs STOP-0 and STOP-1 (from pins 15 and 14 respectively) are voltages derived from the detuning level and the field strength of the input signal. If only one tuning-stop output is required, pins 14 and 15 may be tied together.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 1)	$V_P = V_{1-17}$	−0.3	+16	V
Reference voltage range (pin 5)	V_{5-17}	−0.3	+10	V
Level adjustment range (pin 2)	V_{2-17}	−0.3	+10	V
Mode switch voltage range (pin 7)	V_{7-17}	−0.3	V_P	V
Control input voltage range (pin 13)	V_{13-17}	−	+6	V
THD compensation/unweighted field strength voltage range (pin 3)	V_{3-17}	−0.3	V_P	V
Tuning-stop output voltage range				
STOP-0 (pin 15)	V_{15-17}	−0.3	V_P	V
STOP-1 (pin 14)	V_{14-17}	−0.3	V_P	V
Tuning-stop output current				
STOP-0 (pin 15)	I_{15}	−	2	mA
STOP-1 (pin 14)	I_{14}	−	2	mA
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	−40	+85	°C
Electrostatic handling*				
all pins except pins 5 and 6	V_{es}	−2000	+2000	V
pin 5	V_{es}	−2000	+900	V
pin 6	V_{es}	−2000	+1600	V

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a\ (max.)} = 95$ K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

f = 10.7 MHz; $V_P = V_{1-17} = 8.5$ V; $V_I = V_{20(rms)} = 1$ mV; $T_{amb} = 25$ °C; measured in the circuit of Fig. 3; tuned circuit at pins 10, 11 aligned for symmetrical stop pulses; all voltages are referred to ground (pin 17), unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	$V_P = V_1$	7.5	8.5	12.0	V
Supply current at $I_2 = I_7 = 0$ mA	I_1	–	20	26	mA
FM demodulator					
Input impedance	R_{10-11}	25	40	55	kΩ
	C_{10-11}	–	6	–	pF
DC output voltage (no-signal condition) at $V_{10, 11(p-p)} \leqslant 100\ \mu V$; $V_{20(rms)} \leqslant 5\ \mu V$	V_4	2.75	3.10	3.45	V
Output impedance	R_{4-17}	–	400	–	Ω
Mute attenuator control voltage					
Control voltage (pin 16)					
at $V_{20(rms)} \leqslant 5\ \mu V$	V_{16}	–	2.0	–	V
at $V_{20(rms)} = 1$ mV	V_{16}	–	3.45	–	V
Output impedance (pin 16)	R_{10-17}	–	–	2.0	MΩ
Level shift input (pin 2)					
internal bias voltage at $I_2 = 0$ mA	V_2	–	1.4	–	V
input impedance	R_{2-17}	15	–	–	kΩ
Internal muting (Fig. 6)					
Internal attenuation of signals ± 22.5 kHz $\leqslant$ detuning $\leqslant \pm 80$ kHz $A = 20\log[\Delta V_4(\text{FM mute-off})/\Delta V_4(\text{FM})]$					
at $V_{16} \geqslant 1\ V_5$	A	–	0	–	dB
at $V_{16} = 0.77\ V_5$	A	1.5	3.0	4.5	dB
at $V_{16} = 0.55\ V_5$	A	–	20	–	dB

parameter	symbol	min.	typ.	max.	unit
Attack and decay (pin 16)					
Pin 13 connected to ground					
charge current	$+I_{16}$	–	8	–	μA
discharge current	$-I_{16}$	–	120	–	μA
Pin 13 connected to V_{ref}					
charge current	$+I_{16}$	–	100	–	μA
discharge current	$-I_{16}$	–	120	–	μA
Level detector					
Dependence of output voltage on temperature	$\frac{\Delta V_6}{V_6 \Delta T}$	–	3.3	–	mV/VK
Output impedance	R_6	–	–	500	Ω
Dependence of output voltage (pin 6) on input voltage (pin 20) (Fig. 7):					
$V_{20(rms)} \leqslant 5$ μV; $I_2 = I_7 = 0$ mA	V_6	0.1	0.7	1.3	V
$V_{20(rms)} = 1$ mV; $I_2 = I_7 = 0$ mA	V_6	3.0	3.6	4.2	V
Slope of output voltage (pin 6) for input voltage range					
$V_{20(rms)} \geqslant 50$ μV to $V_{20(rms)} \leqslant 50$ mV	$\frac{\Delta V_6}{20 \Delta \log V_{20}}$	1.4	1.7	2.0	V/20 dB
Dependence of output voltage (pin 6) on detuning (Fig. 8) at input voltage $V_{20(rms)} = 10$ mV:					
detuning $\leqslant \pm 45$ kHz	ΔV_6	–	–	0.2	V
detuning for $V_6 = 1.8$ V	$\pm \Delta f$	90	–	160	kHz
detuning = ±200 kHz	V_6	0.5	0.7	0.9	V
Slope of output voltage with detuning = 125 ± 20 kHz at $V_{20(rms)} = 10$ mV	$\lvert \Delta V_6 / \Delta f \rvert$	–	35	–	mV/kHz
Level shift control (pin 2) (Fig. 9)					
adjustment range	$\pm \Delta V_6$	1.6	2.0	–	V
adjustment gain	$-(\Delta V_6 / \Delta V_2)$	–	1.7	–	V
output voltage at $V_2 = V_5$; $V_{20(rms)} \leqslant 5$ μV	V_6	–	–	0.3	V
Low-pass filter at pin 8					
Output voltage at $I_7 = 0$ mA; $V_{20(rms)} \leqslant 5$ μV	V_8	–	2.2	–	V
Internal resistance	$R_{8(int)}$	12	25	50	kΩ

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning-stop detector (Figs 10 and 11)					
Stop-0: detuning at $V_{20(rms)}$ = 10 mV					
for $V_{15} \geqslant 3.5$ V	$+\Delta f$	–	–	10	kHz
for $V_{15} \leqslant 0.3$ V	$+\Delta f$	18	–	–	kHz
Stop-1: detuning at $V_{20(rms)}$ = 10 mV					
for $V_{14} \geqslant 3.5$ V	$-\Delta f$	–	–	10	kHz
for $V_{14} \leqslant 0.3$ V	$-\Delta f$	18	–	–	kHz
Dependence of STOP-0, STOP-1 on input voltage (pin 20)					
input voltage (RMS value) for $V_{14} = V_{15} \geqslant 3.5$ V	$V_{20(rms)}$	250	–	–	μV
input voltage (RMS value) for $V_{14} = V_{15} \leqslant 0.3$ V	$V_{20(rms)}$	–	–	50	μV
Output voltage when $I_{14} = I_{15} = 1$ mA	$V_{14, 15}$	–	–	0.3	V
Mode switch and pin 3 (Fig. 12)					
FM-off position					
Control voltage for 60 dB muting depth	V_7	–	–	1.4	V
FM, mute-on position (pin 3 = output)					
Internal bias voltage at $R_{7\text{-}17} \geqslant 10$ MΩ	V_7	–	2.8	–	V
Input current	$\lvert I_7 \rvert$	–	–	2.5	μA
Output voltage with $R_{3\text{-}17} = 10$ kΩ; $C_{3\text{-}17} \geqslant 1$ nF*	V_3	–	2	–	V
Output impedance for $V_{20} = \leqslant 5$ μV; $I_3 = 500$ μA	$R_{3\text{-}17}$	–	–	100	Ω
FM, mute-off position (pin 3 = input)					
Control voltage	V_7	$0.9\,V_5$	–	–	V
Input current at $V_7 = V_5$	I_7	–	–	15	μA
Input resistance	$R_{3\text{-}17}$	1	–	–	MΩ
Reference voltage source					
Output voltage at $I_5 = -1$ mA	V_5	3.3	3.7	4.1	V
Output impedance at $I_5 = -1$ mA	$\Delta V_5/\Delta I_5$	–	40	80	Ω
Temperature coefficient	TC	–	3.3	–	mV/K

* Without input voltage.

DEVELOPMENT DATA

OPERATING CHARACTERISTICS

f = 10.7 MHz; $V_I = V_{20(rms)}$ = 1 mV; deviation (Δf) = 22.5 kHz; modulation frequency (f_m) = 400 Hz; de-emphasis (pin 4) = 50 μs; test circuit as per Fig. 3; tuned circuit (Q_L = 19) aligned for symmetrical stop pulses; T_{amb} = + 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
AF output voltage (RMS value) at $V_{20(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Start of limiting (FM, mute-off); (RMS value) (Fig. 13)	$V_{20(rms)}$	14	22	35	μV
Dependence of signal-to-noise ratio (in noise frequency band 250 Hz to 15 kHz, unweighted) on input voltage					
for S/N = 26 dB	$V_{18(rms)}$	–	15	–	μV
for S/N = 46 dB	$V_{18(rms)}$	–	60	–	μV
at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz	S/N	–	82	–	dB
THD (FM, mute-on) at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; without detuning; without de-emphasis; I_7 = 0 mA	THD	–	0.1	0.3	%
Dynamic mute attenuation (Fig. 14) $\alpha_D = 20\log \frac{V_4 \text{ (FM mute-off)}}{V_4 \text{ (FM, mute-on)}}$ with f_m = 100 kHz; Δf = 75 kHz	α_D	–	16	–	dB
Slope of attenuation curve	$\alpha_D \Delta f$	–	0.8	–	dB/kHz
THD (FM, mute-on) at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; detuning $\leqslant \pm$ 25 kHz without de-emphasis; I_7 = 0 mA (Fig. 15)	THD	–	–	0.6	%
THD (FM, mute-off and compensated via pin 3) at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; $V_7 = V_5$	THD	–	0.07	0.25	%
Voltage range at pin 3 for THD compensation	V_3	0	–	V_5	V
AM suppression (FM, mute-off) with amplitude modulation at 30%; input voltage range V_{20} = 300 μV to 100 mV (Fig. 16)		–	65	–	dB
Power supply ripple rejection = 20log [$\Delta V_1/\Delta V_4$]		33	36	–	dB
Mute attenuation (FM-off) = 20log [$V_{4(FM\text{-}on}/V_{4(FM\text{-}off)}$]		60	–	–	dB

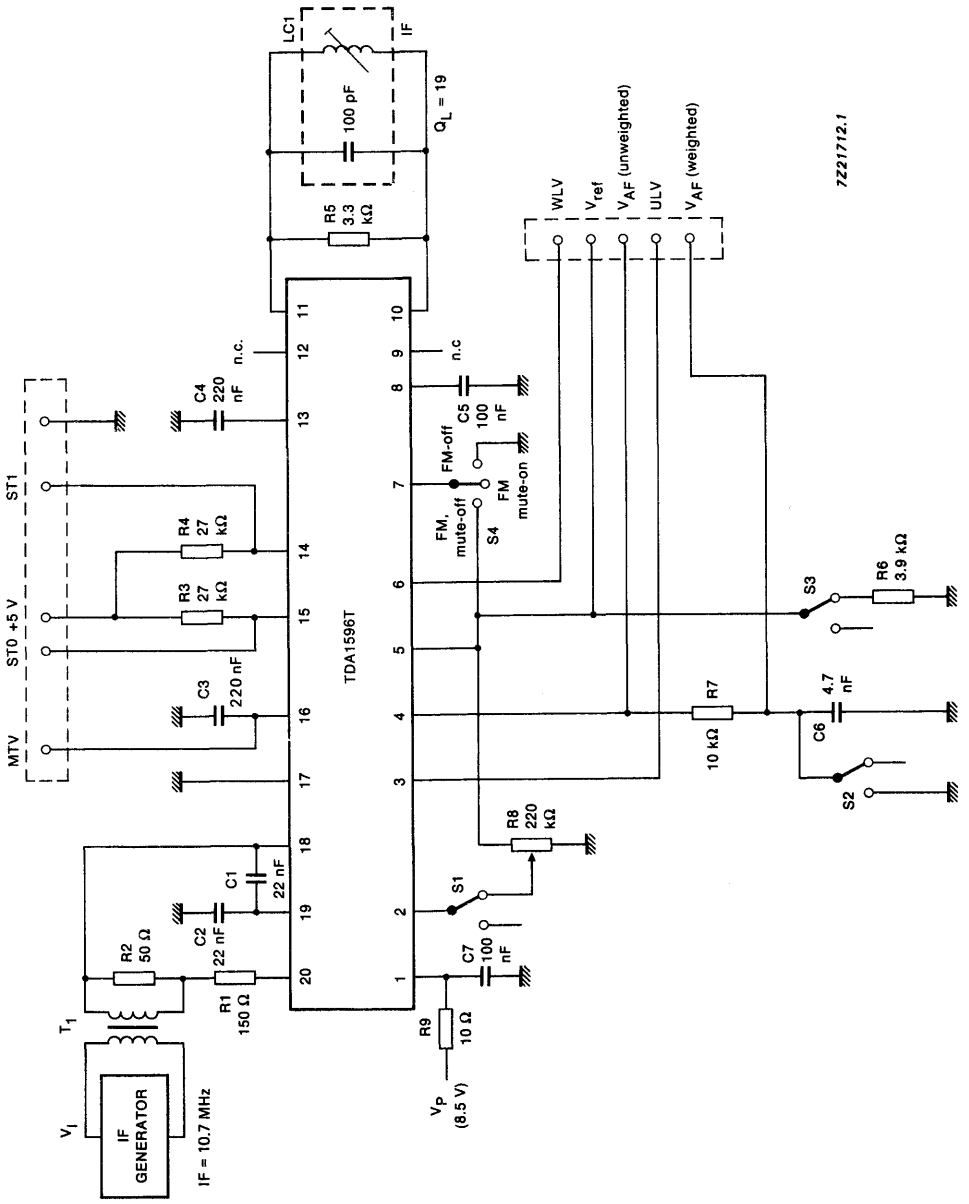


Fig. 3 Test circuit.

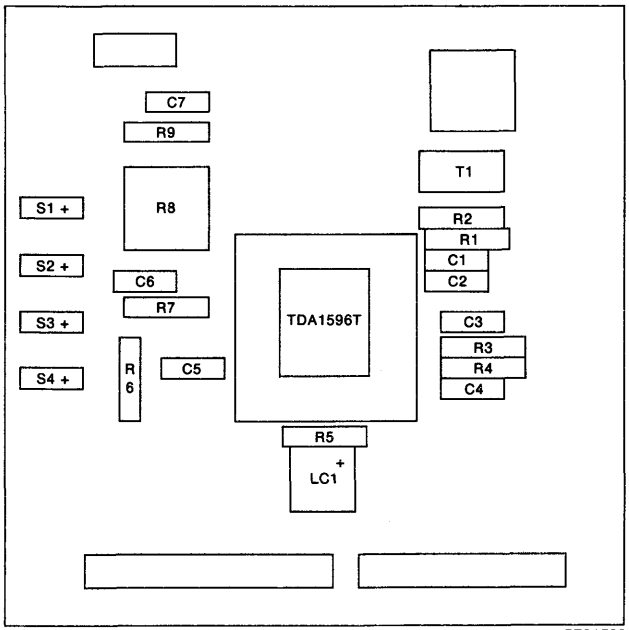


Fig. 4 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 3.

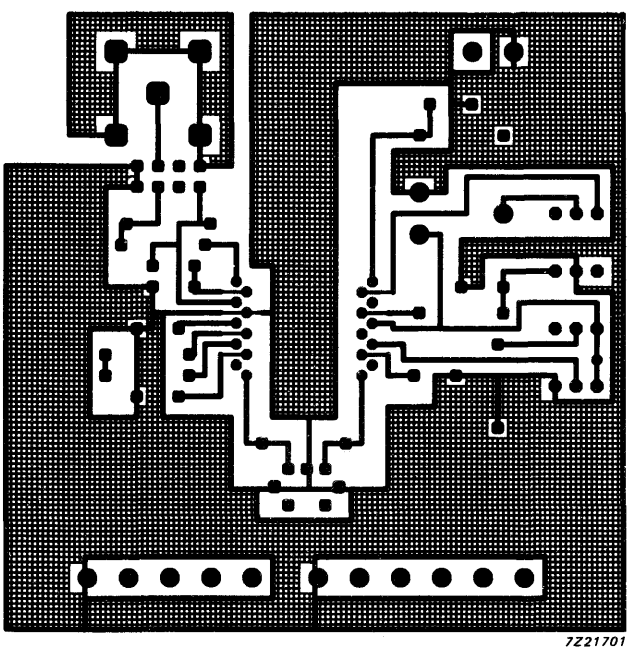


Fig. 5 Printed-circuit board showing track side.

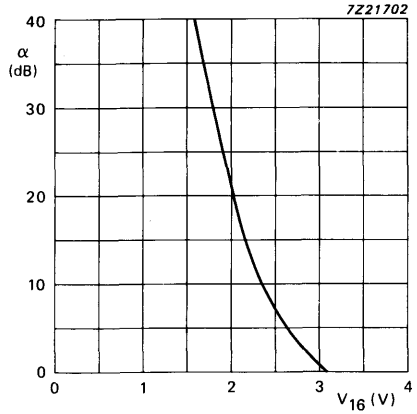


Fig. 6 Typical curve of internal attenuation showing the relationship between the mute attenuator control voltage (pin 16) and mute attenuation; $I2 = I7 = 0$ mA.

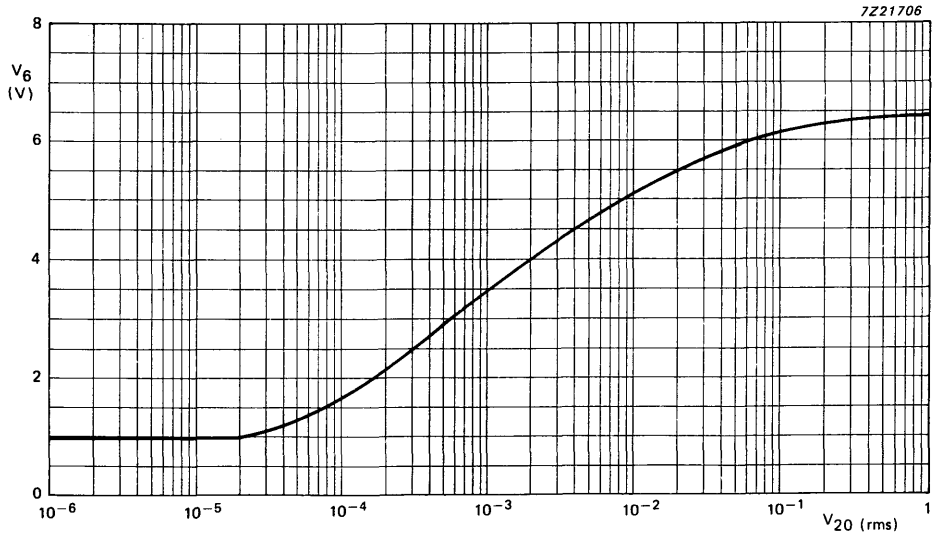


Fig. 7 Weighted field strength output voltage (pin 6) as a function of input voltage (pin 20); $R_{6\text{-}17} \geqslant 10$ kΩ; $I_2 = I_7 = 0$ mA.

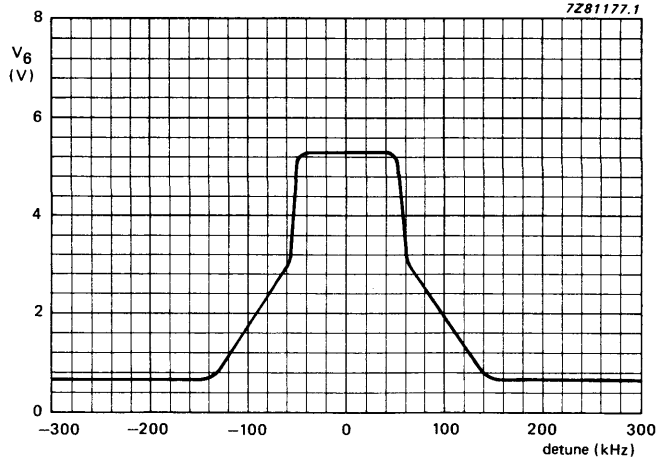


Fig. 8 Weighted field strength output voltage (pin 6) as a function of detuning; $R_{6\text{-}17} \geqslant 10\ k\Omega$; $I_2 = I_7 = 0\ mA$; $V_{20} = 10\ mV$.

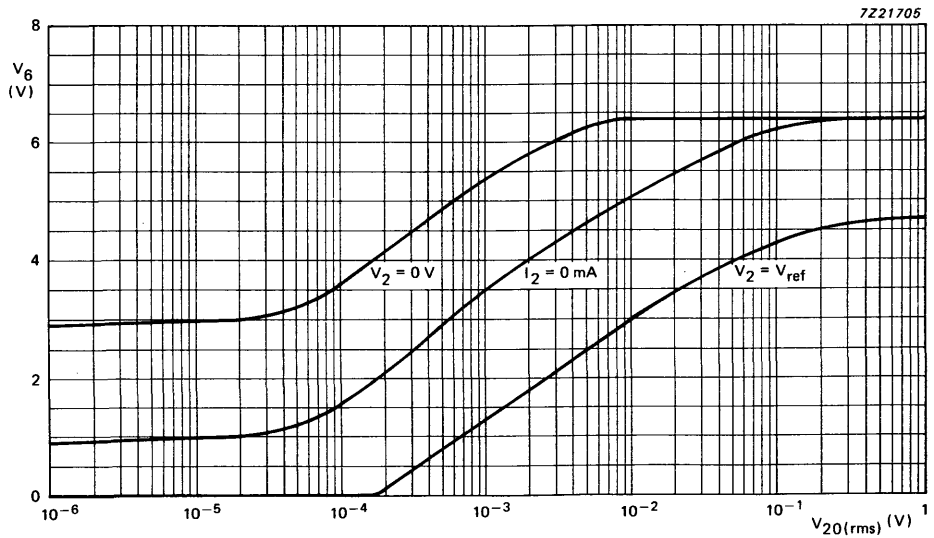
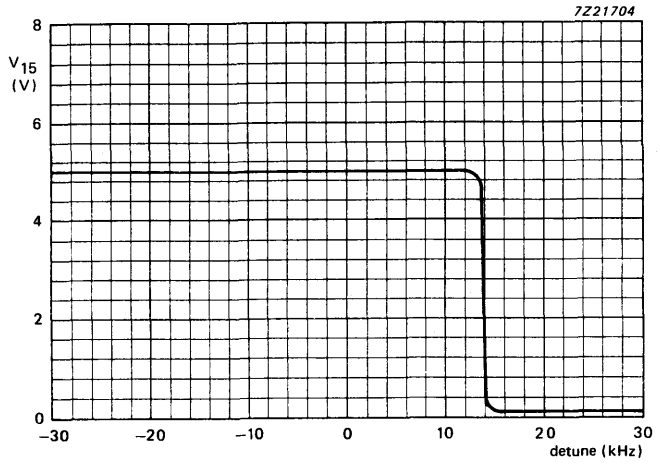
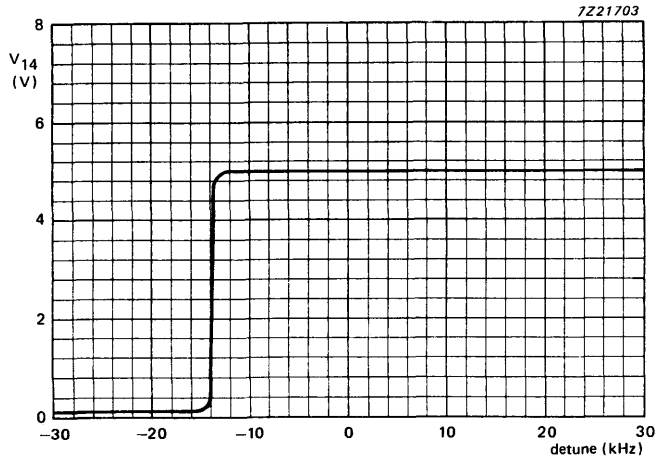


Fig. 9 Adjustment range of weighted field strength output voltage (pin 6) with level shift control (pin 2); $R_{6\text{-}17} \geqslant 10\ k\Omega$; $I_7 = 0\ mA$.

DEVELOPMENT DATA



(a) STOP-0.



(b) STOP-1.

Fig. 10 STOP-0 and STOP-1 output voltages as a function of detuning, measured at V_{20} = 10 mV.

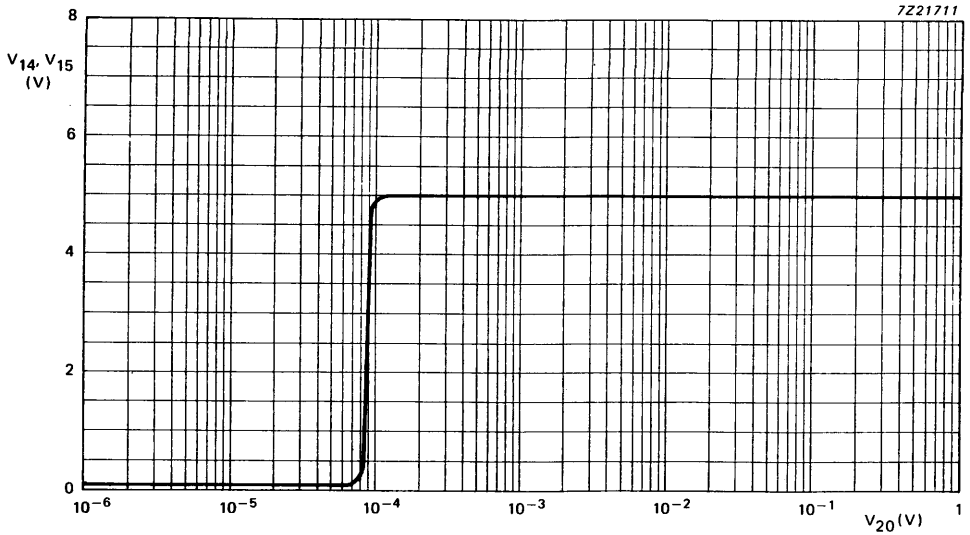


Fig. 11 STOP-0 or STOP-1 output voltages as a function of input voltage at pin 20.

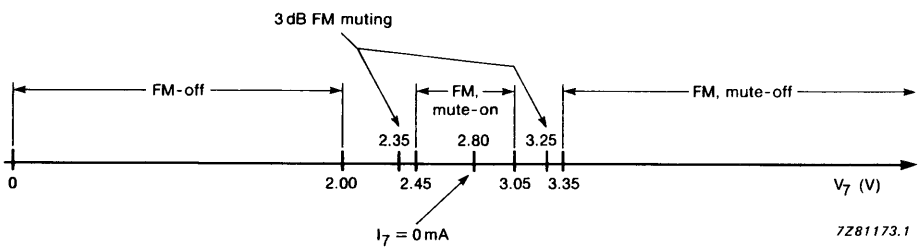
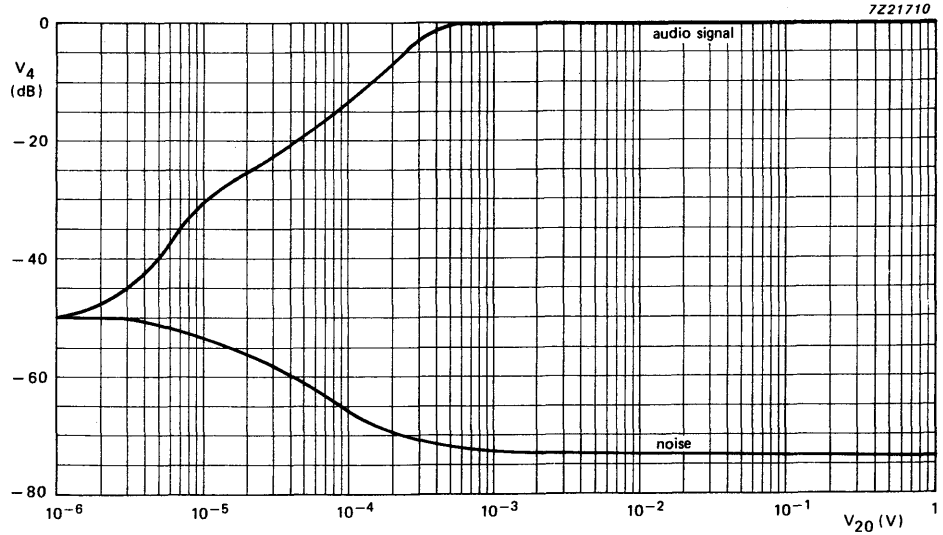
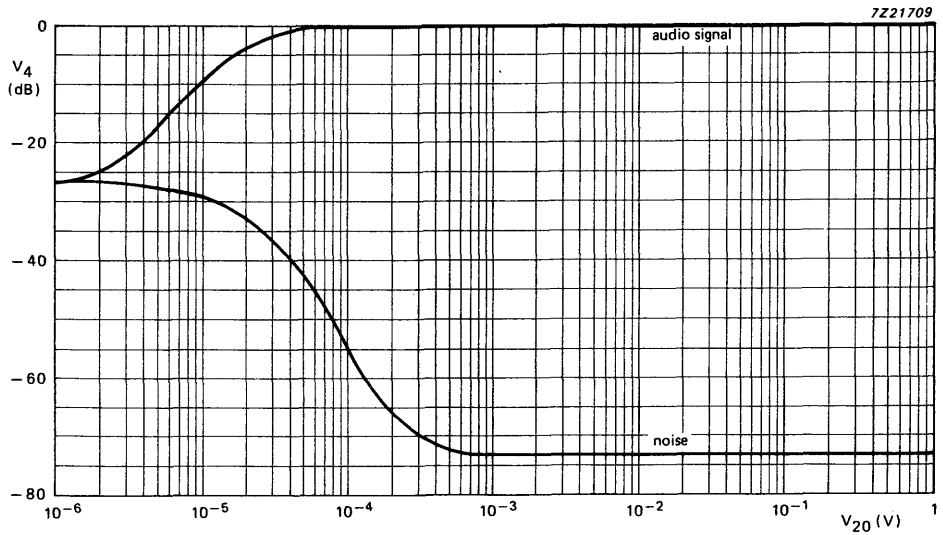


Fig. 12 Switch levels at pin 7.

DEVELOPMENT DATA



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 13 Audio signal (Δf = 22.5 kHz; f_m = 1 kHz) and noise as functions of input voltage at pin 20; measured with 50 μs de-emphasis.

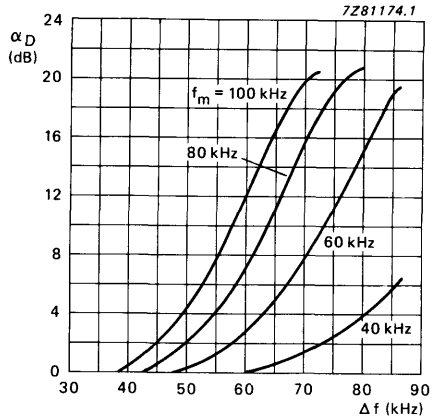


Fig. 14 Dynamic mute attenuation as a function of frequency deviation for modulation frequencies of 40, 60, 80 and 100 kHz.

DEVELOPMENT DATA

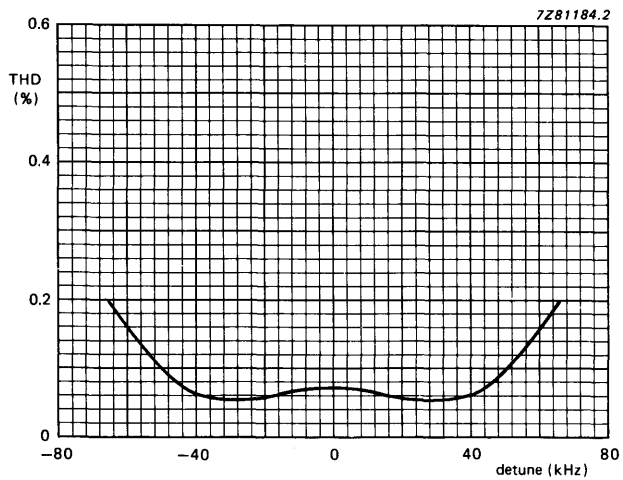
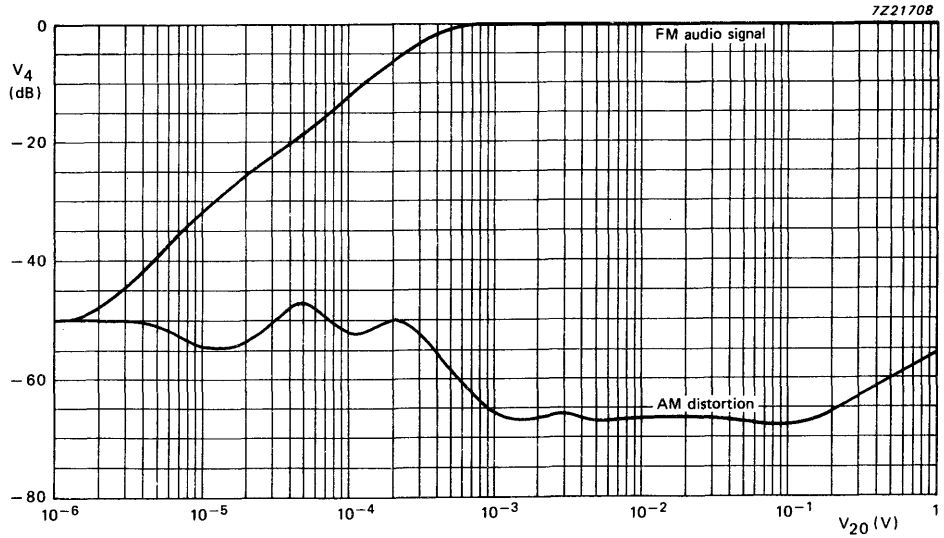
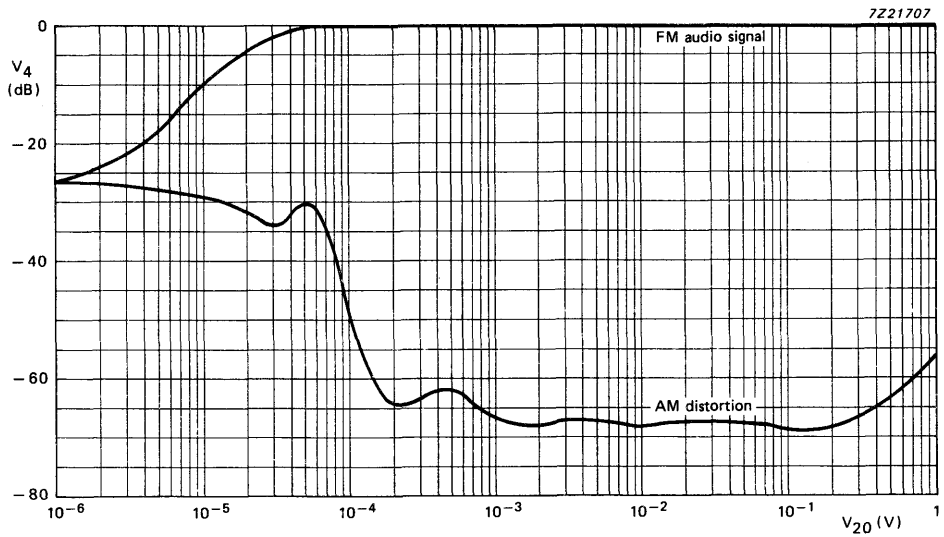


Fig. 15 THD as a function of detuning, mode switch at FM, mute-on position; Δf = 75 kHz; f_m = 1 kHz; $V_{20(rms)}$ = 10 mV.



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 16 Typical curves showing AM suppression for an input signal having frequency modulation at Δf = 22.5 kHz and f_m = 1 kHz, and amplitude modulation of 30% at a frequency of 400 Hz; de-emphasis time = 50 μs and bandwidth = 250 Hz to 15 kHz.

TIME MULTIPLEX PLL STEREO DECODER

GENERAL DESCRIPTION

The TDA1598 is a PLL stereo decoder based on the time-division multiplex principle.

Features

- Selectable input and output voltage levels
- Automatic mono/stereo switching
- Analogue control of mono/stereo change over (stereo blend)
- Pilot indicator driver
- Oscillator with decoupled frequency measurement output
- Internal smoothing of supply voltage

QUICK REFERENCE DATA

Supply voltage, pin 8	$V_P = V_{8-7}$	typ.	8,5	V
Supply current, pin 8	$I_P = I_8$	typ.	17	mA
Multiplex input signal (selectable)	$V_{MUX(p-p)}$	typ.	0,5	V
Input resistance (selectable)	R_i	typ.	47	kΩ
AF output voltage (R = 15 kΩ)	$V_{o(rms)}$	typ.	0,75	V
Output resistance	R_o	low-ohmic		
Spread in gain	Δ	<	1	dB
Channel separation	α	typ.	50	dB
Total harmonic distortion	THD	<	0,5	%
Signal plus noise-to-noise ratio	(S+N)/N	typ.	90	dB
Carrier and harmonic suppression				
pilot signal; f = 19 kHz	α_{19}	typ.	32	dB
subcarrier; f = 38 kHz	α_{38}	typ.	50	dB
f = 57 kHz	α_{57}	typ.	45	dB
f = 76 kHz	α_{76}	typ.	60	dB
Traffic radio (VF); f = 57 kHz	$\alpha_{57(VF)}$	typ.	70	dB
SCA (Subsidiary Communications Authorization); f = 67 kHz	α_{67}	typ.	70	dB
ACI (Adjacent Channel Interference); f = 114 kHz	α_{114}	typ.	80	dB
Operating ambient temperature range	T_{amb}	−40 to + 80		°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

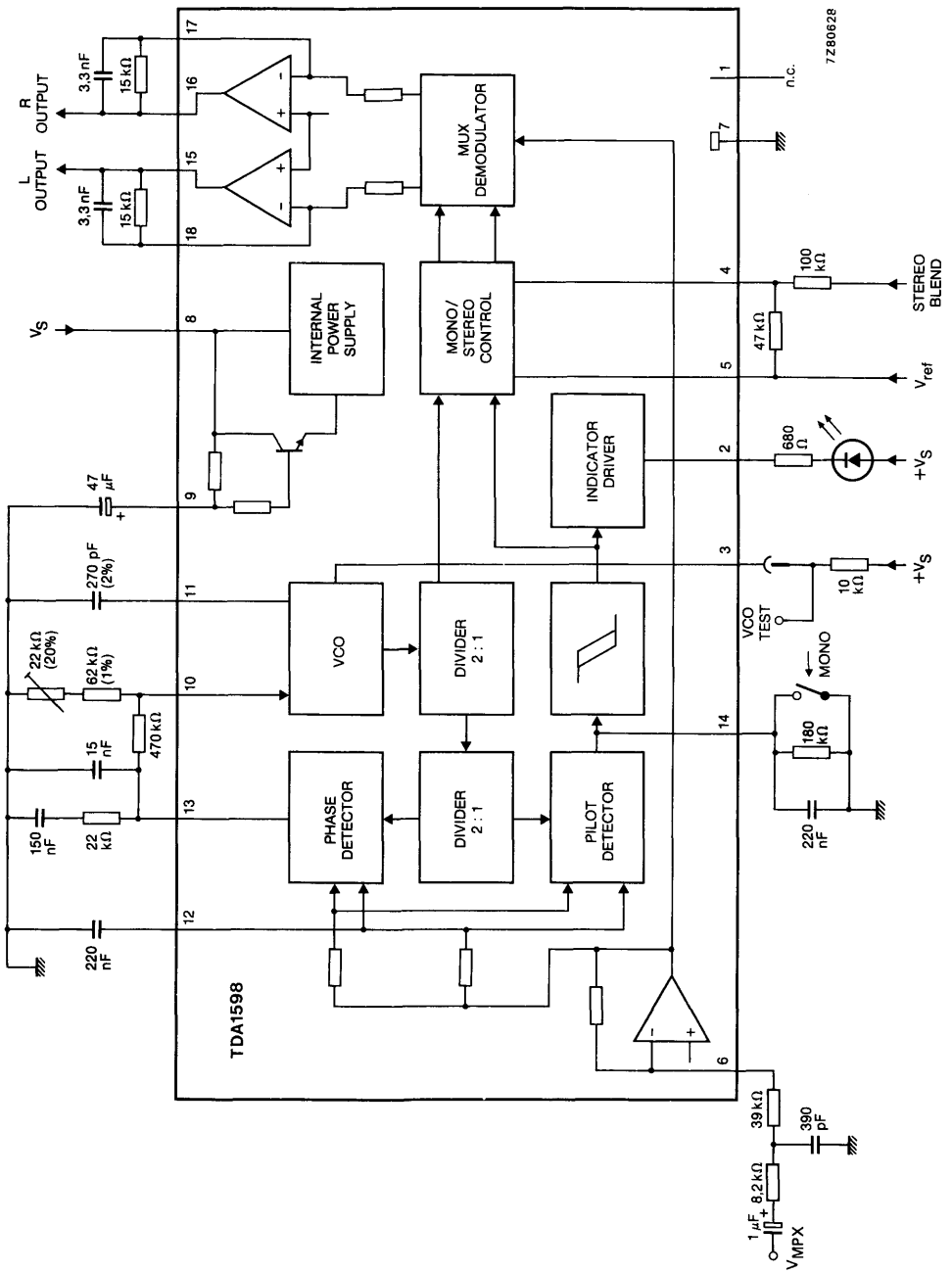


Fig. 1 Block diagram and test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, pin 8	$V_P = V_{8-7}$	max.	16	V
Input voltages, pins 4, 5 and 6	$V_{4;5;6-7}$	max.	V_P	*
Input voltage, pin 3	V_{3-7}	max.	V_P	
Indicator driver voltage	V_{2-7}	max.	18	V
Indicator driver current	I_2	max.	20	mA
Total power dissipation at T_{amb} = 25 °C	P_{tot}	max.	1,2	W
Storage temperature range	T_{stg}	−55 to	+ 150	°C
Operating ambient temperature range	T_{amb}	−40 to	+ 80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ c-a}$	=	80	K/W

DEVELOPMENT DATA

* Not greater than 12 V.

CHARACTERISTICS (measured in Fig. 1)

V_P = 8,5 V; input signal: m = 100%; (Δf = ± 75 kHz); pilot signal: m = 9% (Δf = ± 6,75 kHz); f_m: 1 kHz; V_{4-5} = 0 V; de-emphasizing time: t = 50 μs; oscillator adjusted to f_{osc} at pilot voltage V_i = 0 V; T_{amb} = 25 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage range, pin 8	V_P	7,5	8,5	15	V
Supply current	I_P	–	17	–	mA
Nominal multiplex input voltage (peak-to-peak)	$V_{MUX(p-p)}$	–	0,55	–	V
Input headroom at THD = 1%		3	6	–	dB
AF output voltage (r.m.s. value; mono without pilot)					
$R_{15-18} = R_{16-17}$ = 15 kΩ	$V_{o(rms)}$	–	0,75	–	V
$R_{15-18} = R_{16-17}$ = 24 kΩ	$V_{o(rms)}$	–	1,2	–	V
Spread in output voltage levels	$\lvert\Delta V_o/V_o\rvert$	–	–	1	dB
Difference of output voltage levels	$\lvert\Delta V_{15-16}/V_o\rvert$	–	–	1	dB
Output resistance	R_o		low ohmic		
Available output current pins 15 and 16	$\lvert I_o\rvert$	–	4	–	mA
Modulation range at output (unloaded)	$V_{15;\,16-7}$	1	–	V_{9-7-1}	V
Output voltage DC	$V_{15;\,16-7}$	–	4,5	–	V
Current DC, pins 17 and 18	$-I_{17;\,18}$	–	30	–	μA
Channel separation	α	30	50	–	dB
Total harmonic distortion	THD	–	0,1	0,5	%
Signal plus noise-to-noise ratio f = 20 Hz to 16 kHz	(S+N)/N	–	90	–	dB
Carrier and harmonic suppression at the output					
pilot signal; f = 19 kHz	α_{19}	–	32	–	dB
subcarrier; f = 38 kHz	α_{38}	30	50	–	dB
f = 57 kHz	α_{57}	–	45	–	dB
f = 76 kHz	α_{76}	–	60	–	dB
Intermodulation (note 1) f_m = 10 kHz; spurious signal f_s = 1 kHz					
PLL-filter, Fig. 1	α_2	–	50	–	dB
PLL-filter, Fig. 2	α_2	–	70	–	dB
f_m = 13 kHz; spurious signal f_s = 1 kHz	α_3	–	60	–	dB
Traffic radio (VF); f = 57 kHz (note 2)	$\alpha_{57(VF)}$	–	70	–	dB

parameter	symbol	min.	typ.	max.	unit
Mono/stereo control					
Pilot threshold voltages (peak-to-peak values)					
for stereo 'ON'	$V_{i(p-p)}$	–	21	34	mV
for mono 'ON'	$V_{i(p-p)}$	5,5	16	–	mV
Switch hysteresis V_{iON}/V_{iOFF}	ΔV_i	–	2,5	–	dB
External mono/stereo control (see Fig. 8)					
Switching voltage for external mono control	V_{14-7}	–	–	0,7	V
Control voltage for channel separation; α = 6 dB	$-V_{4-5}$	–	110	–	mV
separation variation	$\lvert\Delta V_{4-5}\rvert$	–	–	20	mV
separation; α = 26 dB	$-V_{4-5}$	–	70	–	mV
Control inputs					
Recommended voltage range	$V_{4;\,5-7}$	0	–	4	V
Input bias current	$I_{4;\,5}$	–	10	100	nA
Output saturation voltage at I_2 = 20 mA	V_{2-7sat}	–	0,5	1,0	V
Output leakage current at V_{2-7} = 18 V	I_2	–	–	20	μA
VCO					
Oscillator frequency (adjustable with R_{10-7})	f_{osc}	–	76	–	kHz
Free-running frequency dependancy (note 5) on temperature	TC	–	1	–	10^{-4}/K
Capture and holding range for pilot input voltages V_{pil} = 0,5 x V_{pil} nom	$\lvert\Delta f/f\rvert$	2	–	–	%
Voltage DC at pin 10 (3,2 x V_{BE})	V_{10-7}	–	2,1	–	V
VCO test point; internal switching threshold	V_{3-7}	6	–	–	V
Output voltage (peak-to-peak value) at pin 3; (R = 10 kΩ to V_P)	$V_{3-7(p-p)}$	–	420	–	mV
Output resistance	R_{3-7}	–	5	–	kΩ
SCA (Subsidiary Communications Authorization); f = 67 kHz (note 4)	α_{67}	–	70	–	dB
ACI (Adjacent Channel Interference) (note 3); f = 114 kHz	α_{114}	–	80	–	dB
f = 190 kHz	α_{190}	–	52	–	dB
Ripple rejection at the output; f = 100 Hz; $V_{P(rms)}$ = 100 mV, pin 18	RR_{100}	40	43	–	dB
Source resistance	R_{9-8}	6	8	10	kΩ

DEVELOPMENT DATA

Notes to the characteristics

1. Intermodulation suppression (BFC: Beat-Frequency Components)

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz}}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})}\ ;\ f_s = (2 \times 10\text{ kHz}) - 19\text{ kHz}$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})}\ ;\ f_s = (3 \times 13\text{ kHz}) - 38\text{ kHz}$$

measured with: 91% mono signal; f_m = 10 or 13 kHz; 9% pilot signal.

2. Traffic radio (VF) suppression.

$$\alpha_{57(VF)} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz} \pm 23\text{ Hz})}$$

measured with: 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 kHz, f_m = 23 Hz AM, m = 60%).

3. ACI (Adjacent Channel Interference)

$$\alpha_{114} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 4\text{ kHz})}\ ;\ f_s = 110\text{ kHz} - (3 \times 38\text{ kHz})$$

measured with: 90% mono signal; f_m = 1 kHz; 9% pilot signal; 1% spurious signal (f_s = 110 kHz or 186 kHz, unmodulated).

4. SCA (Subsidiary Communications Authorization)

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 9\text{ kHz})}\ ;\ f_s = (2 \times 38\text{ kHz}) - 67\text{ kHz}$$

measured with: 81% mono signal; f_m = 1 kHz; 9% pilot signal; 10% SCA-subcarrier (f_s = 67 kHz, unmodulated).

5. The effects of external components are not taken into account.

APPLICATION NOTES

1. When mono-stereo control is not used, pins 4 and 5 have to be grounded.
2. In a receiver, channel separation can be adjusted by:
   a. RC or LC filter at the input: frequency response compensation (V_G = f(w)).
   b. Feeding the output signals of the output amplifier to the inputs of the other channel.
3. PLL-filter for reduced intermodulation (a_2); see Fig. 2.
4. External mono 'ON' switch; see Fig. 3.
5. Switching 'OFF' the oscillator; see Fig. 4.

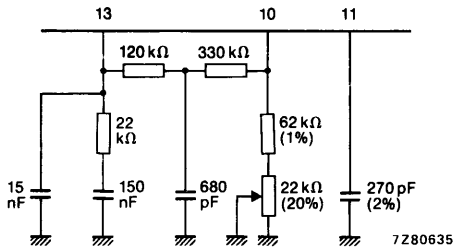


Fig. 2 PLL-filter for α_2 = 70 dB (see also Fig. 1).

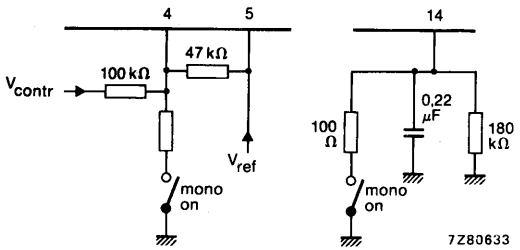


Fig. 3 (a) At pin 4; $-V_{4-5} > 300$ mV; (b) at pin 14.

DEVELOPMENT DATA

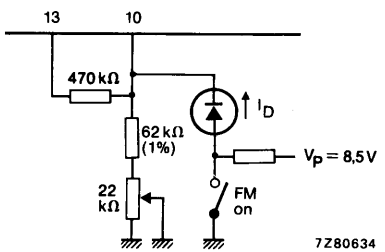


Fig. 4 The oscillator is switched-off when: $I_D > 50\ \mu A$ and $I_D < 1$ mA.

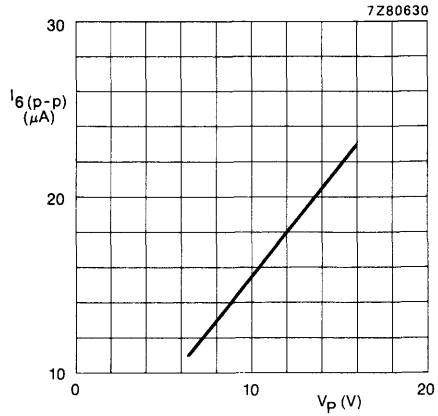


Fig. 5 Signal handling range at the input for I_{6nom} (± 75 kHz); $V_{9-7} = V_P$.

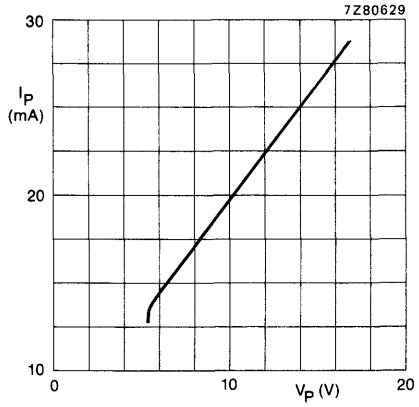


Fig. 6 Supply current consumption at $V_{9-7} = V_P$.

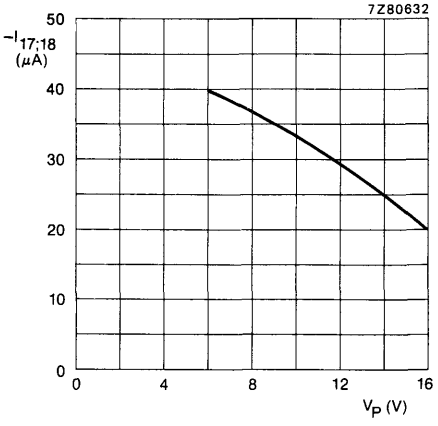


Fig. 7 DC current in the feedback loop of the output amplifier.

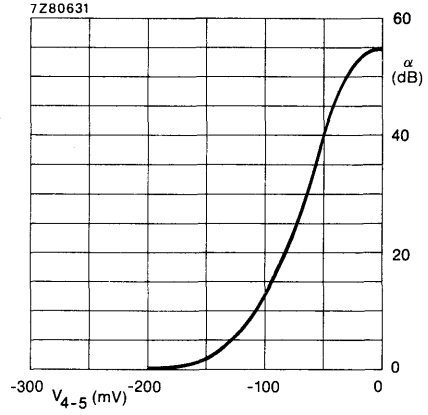


Fig. 8 Mono/stereo control at f_m = 1 kHz; α is the channel separation. V_P = 8,5 V.

MULTI-FUNCTION OSCILLATOR SWITCH FOR AN AUDIO CASSETTE RECORDER

GENERAL DESCRIPTION

The TDA1600 is a bipolar circuit designed for high fidelity cassette recorders. This device contains several functions (see 'features') which can be selected by external d.c. voltage levels or via a microprocessor. The TDA1600 operates from a mains-fed asymmetrical power supply. For application purposes the voltage output can be either ½ V_P asymmetrical or ½ V_P symmetrical. The output of all the functions are current protected.

Features

- Stereo playback amplifier
- Electronic switch for playback equalization
- Electronic head-switch (two times)
- Erase and bias oscillator
- LED driver
- Tape selector
- Reference voltage source (½ V_P)
- Logic part

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	10	–	20	V
Playback amplifier						
Open loop gain		Go	–	106	–	dB
Minimum closed loop gain		Gc	–	30	–	dB
S/N ratio	V_O = 50 mV	S/N	–	65	–	dB
Total harmonic distortion	V_O = 50 mV	THD	–	–60	–	dB
Head-switch						
Maximum voltage (peak-to-peak value)		V_{OM}	–	–	120	V
Oscillator						
Frequency range		f_o	60	–	120	kHz
Maximum output current (peak value)		I_{OM}	–	–	80	mA
Maximum output voltage (peak value)		V_{OM}	–	–	40	V
LED driver						
Maximum d.c. output current		I_{OM}	–	–	± 15	mA
Reference voltage						
Output voltage		V_{REF}	–	½ V_P	–	V
Maximum load current		$I_{L\,max}$	–	–	± 18	mA
Logic part						
Input current		I_I	–	–1	–	μA

PACKAGE OUTLINE

24-lead DIL; plastic, with internal heatspreader (SOT101B).

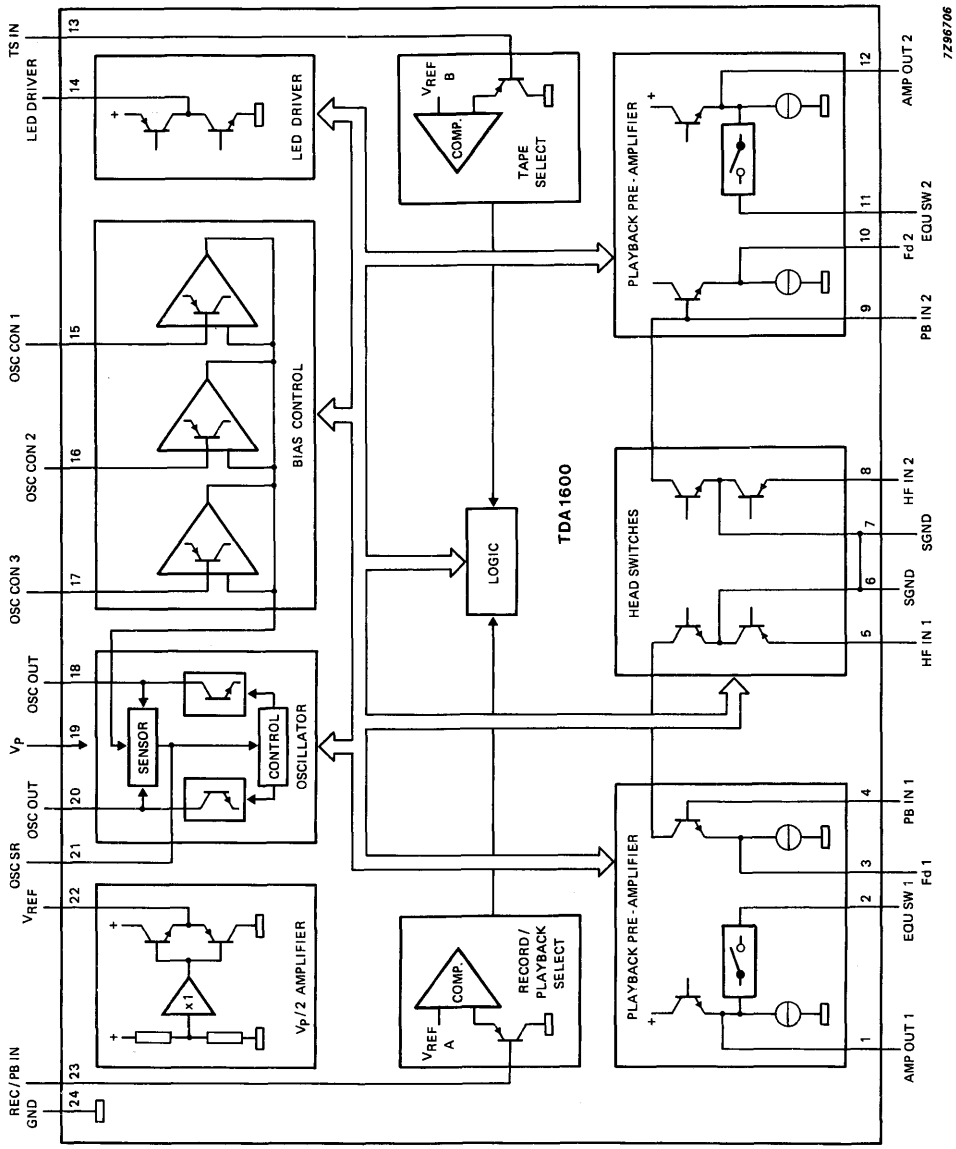


Fig. 1 Block diagram.

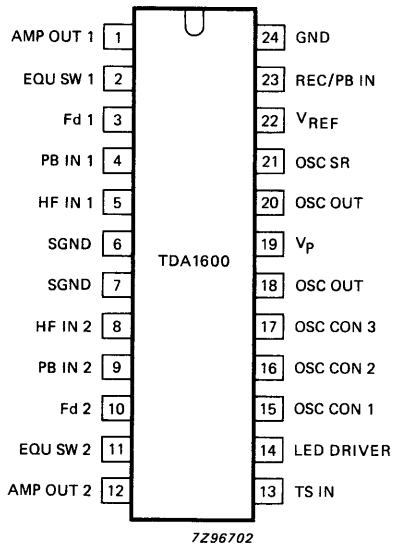


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

PINNING

1	AMP OUT 1	pre-amplifier 1 output
2	EQU SW 1	equalization switching for pre-amplifier 1
3	Fd 1	feedback to pre-amplifier 1
4	PB IN 1	input to pre-amplifier 1 from playback side of head
5	HF IN 1	H.F. input from recording side of head
6	SGND	signal ground
7	SGND	signal ground
8	HF IN 2	H.F. input from recording side of head
9	PB IN 2	input to pre-amplifier 2 from playback side of head
10	Fd 2	feedback to pre-amplifier 2
11	EQU SW 2	equalization switching for pre-amplifier 2
12	AMP OUT 2	pre-amplifier 2 output
13	TS IN	tape select input
14	LED DRIVER	LED driver output
15	OSC CON 1	control input for oscillator
16	OSC CON 2	control input for oscillator
17	OSC CON 3	control input for oscillator
18	OSC OUT	oscillator output
19	V_P	supply voltage
20	OSC OUT	oscillator output
21	OSC SR	smoothing oscillator regulator
22	V_{REF}	reference voltage
23	REC/PB IN	record/playback select input
24	GND	ground

FUNCTIONAL DESCRIPTION

Playback amplifier

The playback amplifier is a low noise pre-amplifier which is internally connected to the head-switch. The gain of the amplifier can be externally fixed, to provide an optimal output voltage for a noise reduction system (e.g. Dolby). The playback constants (70 μs and 120 μs) are determined by external components, while the switch over is controlled by the logic part of the circuit. In the record mode, the playback amplifier is switched OFF.

Head-switch

The electronic head-switch has two positions:

- record mode: the playback side of the head is switched to signal ground, while the recording side is opened to allow the bias and audio current to be fed to the head.
- playback mode: the recording side of the head is switched to signal ground, while the playback side is connected to the input of the playback amplifier.

Both of these positions are controlled by the logic part of the circuit.

Erase and bias oscillator

Every audio hi-fidelity cassette recorder contains a high frequency bias current for linearization of the magnetic recording process on the tape. The high frequency bias current is added to the audio current (from a recording amplifier) and fed into the recording head. The oscillator generates a voltage which is converted into a bias current by an external resistor. The oscillator output voltage is dependent upon the type of tape selected; Ferro (FeO_2), Chrome (CrO_2) or Metal. The selection of the voltage level is controlled by the logic part, while the ratio level is determined by four external resistors. The oscillator also provides the current necessary for erasing the tape. The bias oscillator is only activated during the record mode.

LED driver

This circuit provides the voltage which drives the LED tape indicator. The circuit has three output positions; 0, ½ V_P or V_P, all of which are controlled by the logic part of the device.

Reference voltage

The circuit delivers an output voltage which is half the supply voltage. By using this output as signal ground, a symmetrical power supply is available (+ ½ V_P and −½ V_P), which can be used for the overall recording system. This application allows some flexibility in the choice of other IC's and components for the overall system.

Logic part

The logic part converts the incoming information, from the tape selector switches and from the record/playback switch, into the necessary switching signals. The switching signals are required for the analogue parts of the circuit. This conversion is determined by the input signal level and is independent of the rise or fall-time of this signal.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_P	–	20	V
Logic input voltage	pins 13 and 23	V_I	0	V_P	V
Control input voltage	pins 15, 16 and 17	V_I	0	V_P	V
Head-switch voltage	pins 5 and 8	V_I	–60	+60	V
Total power dissipation	T_{amb} = +60 °C	P_{tot}	–	2,5	W
Storage temperature range		T_{stg}	–65	+150	°C
Junction temperature		T_j	–	+150	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 15 V; f = 315 Hz; T_{amb} = 25 °C, unless otherwise specified (see Fig. 6)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	10	15	20	V
Supply current	note 1,					
	playback mode	I_P	–	25	45	mA
	record mode	I_P	–	50	70	mA
Playback amplifier	position FeO_2					
Open loop gain		Go	86	106	–	dB
Closed loop gain	note 2, FeO_2	Gc	49	50	51	dB
Closed loop gain	CrO_2 and Metal	Gc	30	31	32	dB
Output voltage	V_I = 150 μV	V_O	–	50	–	mV
Total harmonic distortion	V_O = 50 mV	THD	–	–60	–55	dB
	V_O = 500 mV	THD	–	–50	–45	dB
S/N ratio	note 3;					
	weighted curve 20 Hz to 20 kHz at position CrO_2 and Metal	S/N	59	65	–	dB
	see Fig. 5, weighted curve A (IEC 179) at position CrO_2 and Metal	S/N	–	61	–	dB
	weighted curve 20 Hz to 20 kHz at position CrO_2 and Metal	S/N	–	54	–	dB
Frequency response			see Fig. 3			

parameter	conditions	symbol	min.	typ.	max.	unit
Channel separation	V_O = 50 mV		45	60	–	dB
Ripple rejection	V_{rip} = 100 mV, f = 100 Hz and R_S = 1 kΩ	RR	35	41	–	dB
Input impedance		Z_I	100	–	–	kΩ
Input bias current		I_{bias}	–	0,8	1,5	μA
D.C. output voltage w.r.t. $V_{6/7}$	pins 6 and 7	V_O	−1,1	−0,9	–	V
D.C. output voltage w.r.t. $V_{6/7}$	record mode pins 6 and 7	V_O	−1,1	−0,9	–	V
Input signal suppression	record mode, V_I = 20 mV, f = 85 kHz		–	65	–	dB
Head-switch						
Impedance ON	playback mode, (V_{23} = 2 V) between pins 5/8 and 6/7 at I = 100 μA (rms)	Zon	–	40	80	Ω
Impedance ON	record mode, (V_{23} = 13 V) between pins 4/9 and 6/7 at I = 1,5 mA (rms) f = 85 kHz	Zon	–	10	30	Ω
Leakage current	between pins 5/8 and 6/7 at V_{DC} = ± 60 V	$\|I_I\|$	–	1,0	2,5	μA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Erase and bias oscillator						
Oscillator frequency	note 4	f_o	–	85	–	kHz
Output current (peak value)		I_O	–	–	80	mA
Maximum output voltage (peak)	V_P = 20 V	V_{OM}	–	–	40	V
Control voltage range	pins 15, 16 and 17	V_O	−13	–	−2	V
Output voltage (peak) w.r.t. V_P	note 5, control voltage = −2 V	V_O	1,8	2,0	2,2	V
Output voltage (peak) w.r.t. V_P	note 5, control voltage = −13 V	V_O	12,8	13,0	13,2	V
Input current at control inputs		I_I	−4	–	–	μA
Distortion of output voltage	between pins 18 and 20, I_O = 80 mA	THD	–	−65	–	dB
LED driver						
Output voltage	V_{13} = 15 V, (FeO_2) and R_{load} = 10 kΩ	$\lvert V_{14\text{-}22}\rvert$	–	–	10	V
Output voltage loss	V_{13} = 7,5 V, (CrO_2) and I_O = −15 mA	$V_{14\text{-}24}$	1,5	2,0	2,5	V
Output voltage loss	V_{13} = 0 V, (Metal) and I_O = 15 mA	$V_{14\text{-}19}$	1,5	2,0	2,5	V
Output current limit		I_O	± 15	± 20	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage						
Output voltage	note 6, no external load	V_{22-24}	7,25	7,50	7,75	V
Output voltage deviation	ΔI_I = 15 mA	ΔV_O	–	30	90	mV
Load current		I_L	–	–	18	mA
Output current limit		I_{OI}	20	30	–	mA
Logic inputs						
Input for tape selection	pin 13					
Input current		I_I	–	–1	–20	μA
Input voltage	FeO_2	V_I	11	–	15	V
Input voltage	CrO_2	V_I	6	–	9	V
Input voltage	Metal	V_I	0	–	4	V
Input for record/playback mode selection	pin 23					
Input current		I_I	–	–1	–20	μA
Input voltage	see Fig. 4					
	playback mode	V_I	0	–	4	V
	record mode	V_I	11	–	15	V

DEVELOPMENT DATA

Notes to the characteristics

1. The supply current is measured in the test circuit without loading the LED driver or the additional load of the ½ V_P amplifier. In the record mode the tape selector is at Metal position.
2. The closed loop gain will be fixed by R_{FeO_2} in the FeO_2 position, by $R_{FeO_2}//R_{CrO_2}$ in the CrO_2 position and by $R_{FeO_2}//R_{CrO_2}$ in the Metal position. The gain of the amplifier must not be lower than 30 dB.
3. The S/N ratio is related to V_O = 50 mV (at f = 315 Hz) and R_S = 1 kΩ.
4. The oscillator frequency is determined by L and C_L and may be adjusted between 60 kHz and 120 kHz.
5. The voltage applied to the control inputs (pins 15, 16 and 17) is $-(V_P - 2\ V)$ min. and –2 V max. with respect to V_P.
6. The output voltage is independent of the operating mode (playback/record).

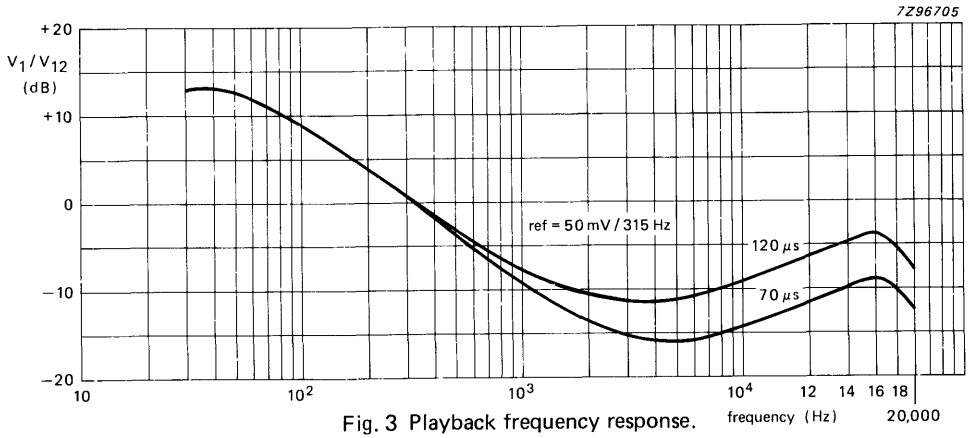


Fig. 3 Playback frequency response.

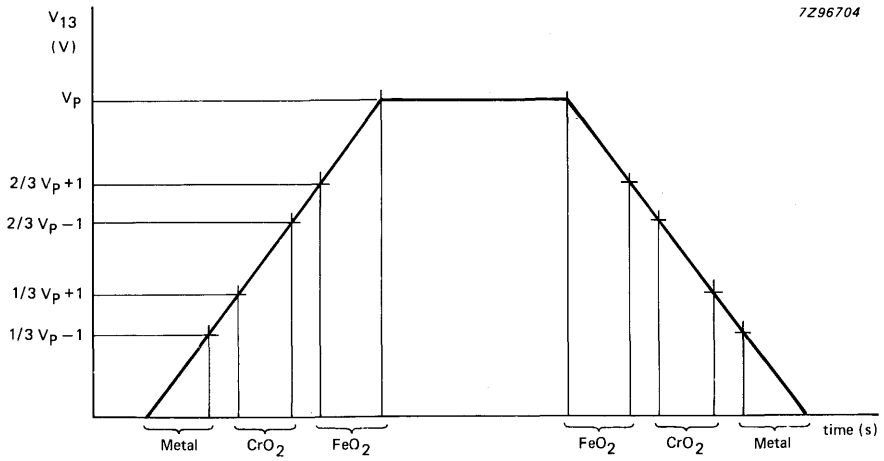


Fig. 4(a) Tape select input.

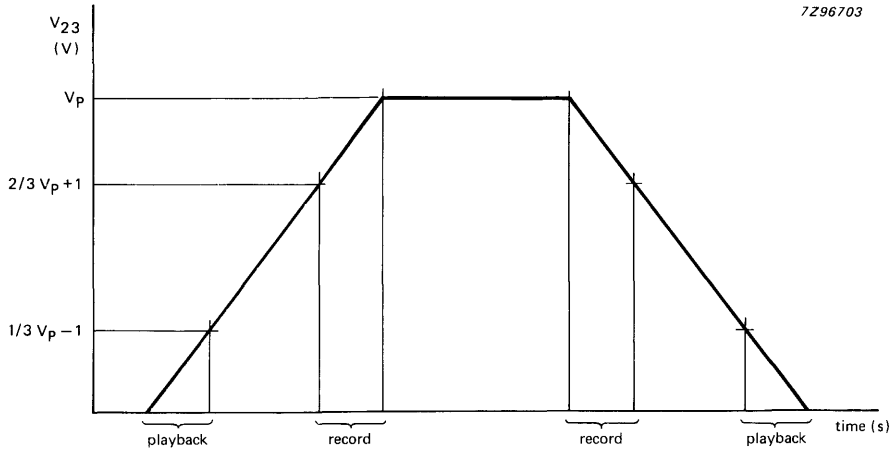


Fig. 4(b) Record/playback input.

APPLICATION INFORMATION

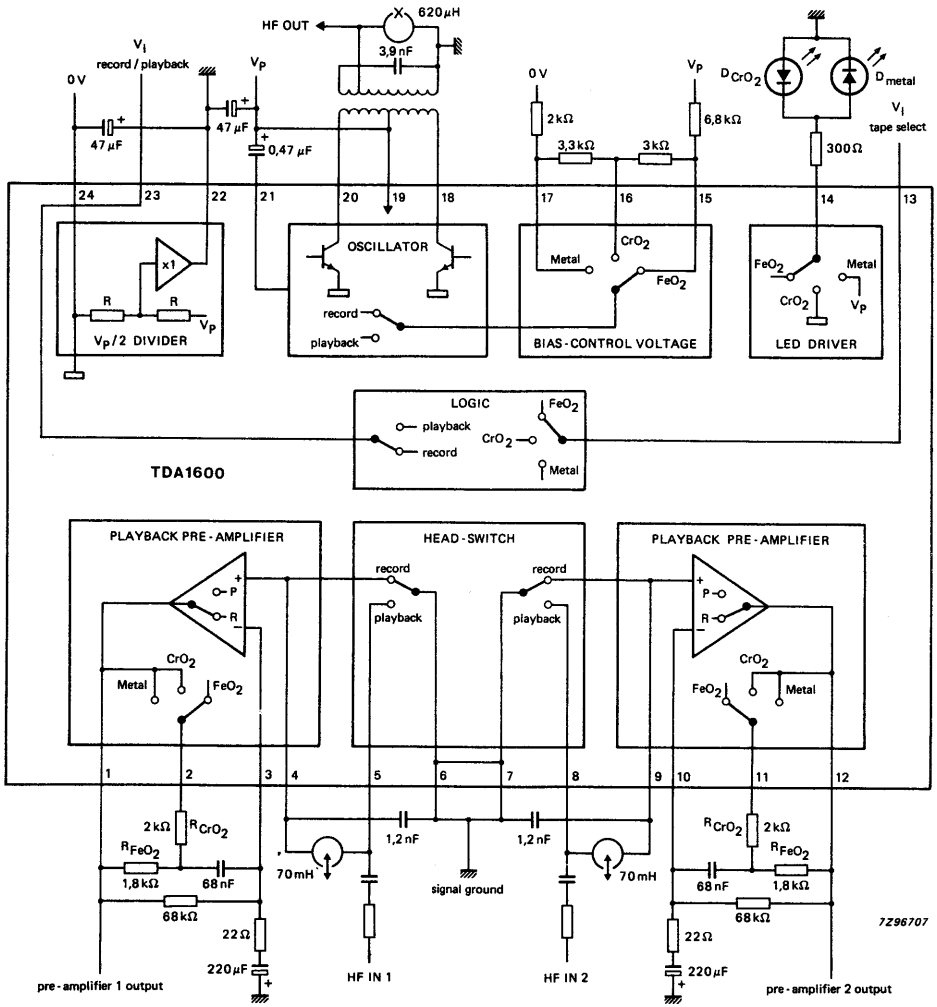


Fig. 5 Application diagram.

APPLICATION INFORMATION (continued)

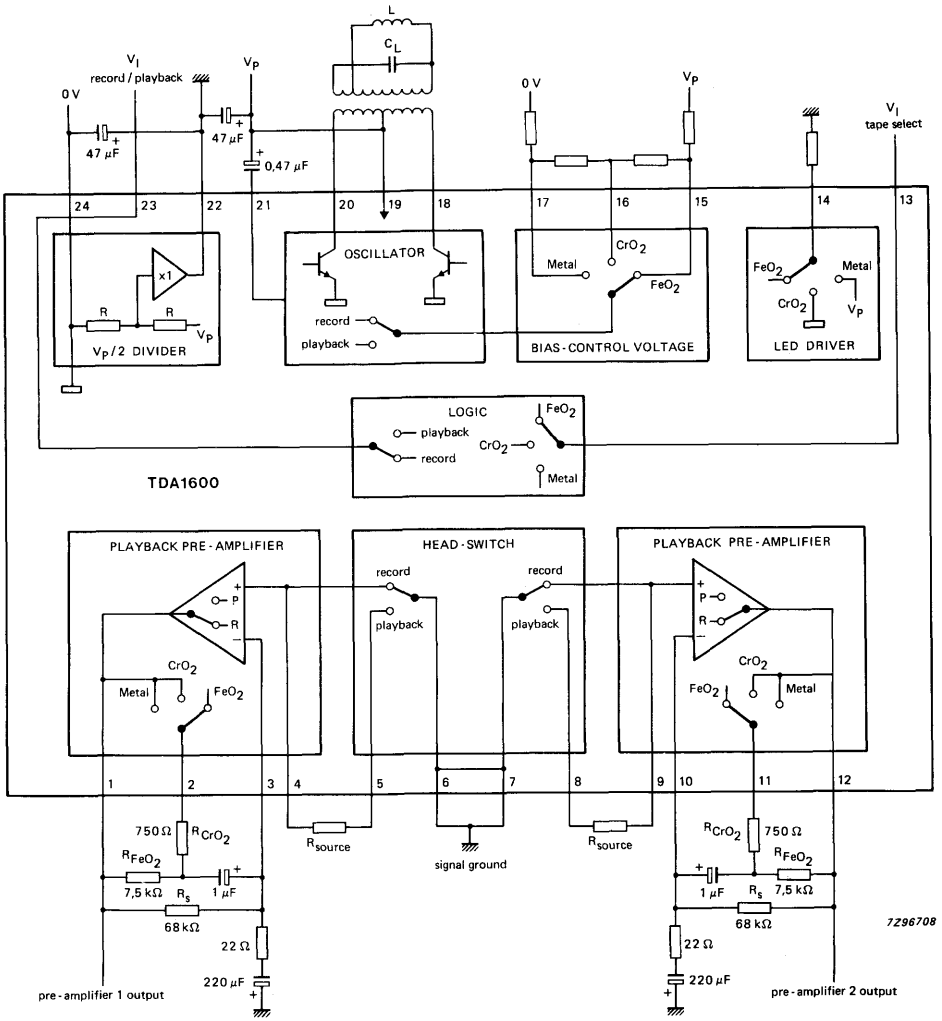


Fig. 6 Test circuit diagram.

5 W AUDIO POWER AMPLIFIER

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastic package with a high supply voltage audio amplifier. Special features are:

- **possibility for increasing the input impedance**
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 35 V
Repetitive peak output current	I_{ORM}	<	1,5 A
Output power at d_{tot} = 10%			
V_P = 18 V; R_L = 8 Ω	P_o	typ.	4,5 W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5 W
Total harmonic distortion at P_o < 2 W; R_L = 8 Ω	d_{tot}	typ.	0,3 %
Input impedance	$\lvert Z_i \rvert$	typ.	45 kΩ
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25 mA
Sensitivity for P_o = 2,5 W; R_L = 8 Ω	V_i	typ.	55 mV
Operating ambient temperature	T_{amb}		−25 to + 150 °C
Storage temperature	T_{stg}		−55 to + 150 °C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

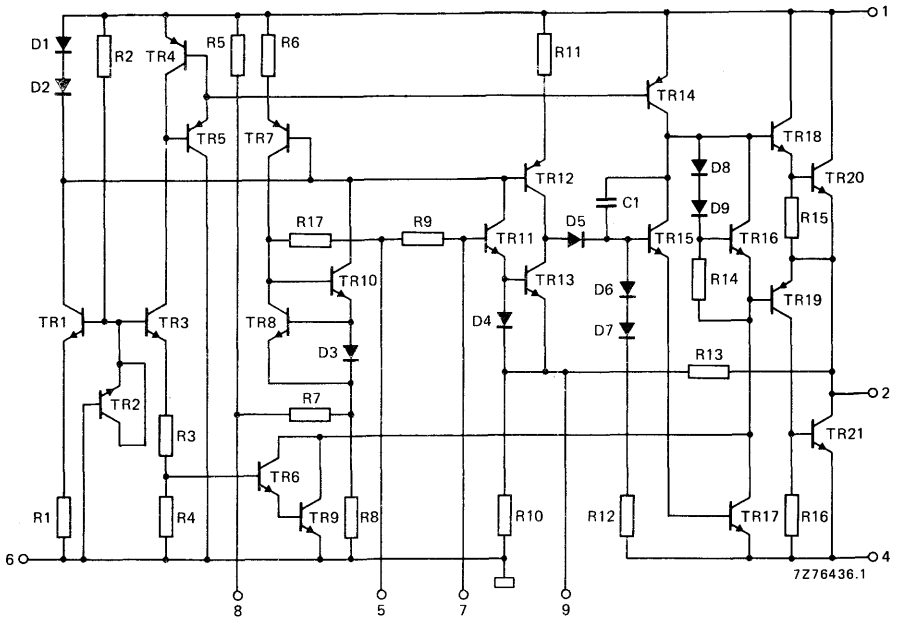


Fig. 1 Circuit diagram; pin 3 not connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Non-repetitive peak output current	I_{OSM}	max.	3 A
Repetitive peak output current	I_{ORM}	max.	1,5 A
Total power dissipation	see derating curves Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C

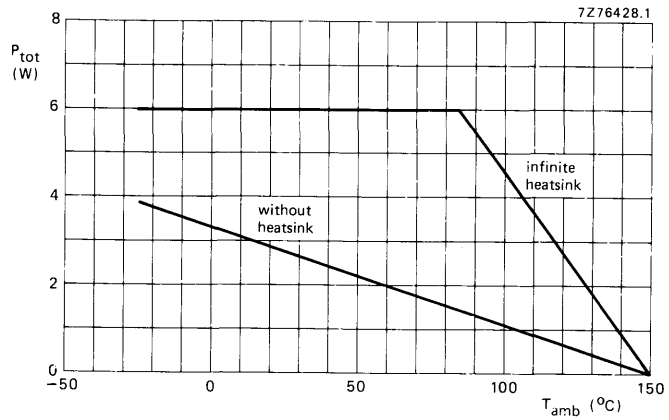


Fig. 2 Power derating curves.

HEATSINK EXAMPLE

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C maximum; T_j = 150 °C (max. for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,2 W).
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{2,2} = 41\ K/W.$$

Since $R_{th\ j\text{-}tab}$ = 11 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 41 − (11 + 1) = 29 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 35 V
Repetitive peak output current	I_{ORM}	<	1,5 A
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25 mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 18 V; R_L = 8 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3

A.F. output power at d_{tot} = 10%			
V_P = 18 V; R_L = 8 Ω	P_o	>	4 W
		typ.	4,5 W
V_P = 12 V; R_L = 8 Ω	P_o	typ.	1,7 W
V_P = 8,3 V; R_L = 8 Ω	P_o	typ.	0,65 W
V_P = 20 V; R_L = 8 Ω	P_o	typ.	6 W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5 W
Total harmonic distortion at P_o = 2 W	d_{tot}	typ.	0,3 %
		<	1 %
Frequency response		>	15 kHz
Input impedance	$\|Z_i\|$	typ.	45 kΩ *
Noise output voltage at R_S = 5 kΩ; B = 60 Hz to 15 kHz	V_n	typ.	0,2 mV
		<	0,5 mV
Sensitivity for P_o = 2,5 W	V_i	typ.	55 mV
			44 to 66 mV

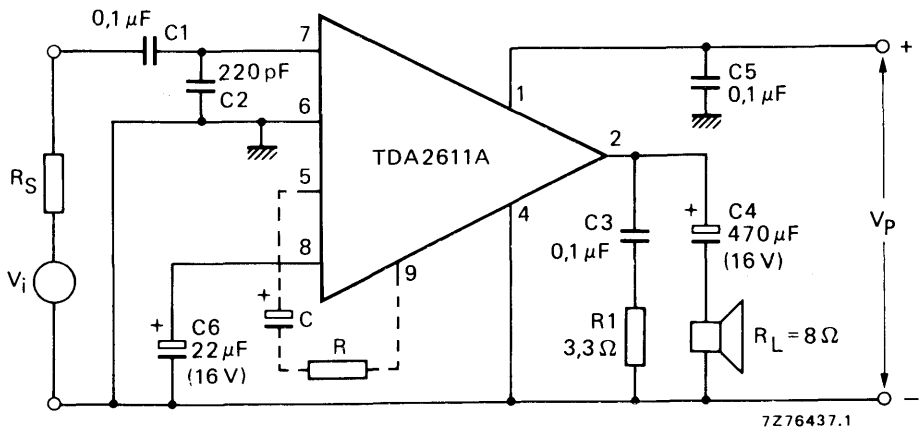


Fig. 3 Test circuit; pin 3 not connected.

* Input impedance can be increased by applying C and R between pins 5 and 9 (see also Figures 6 and 7).

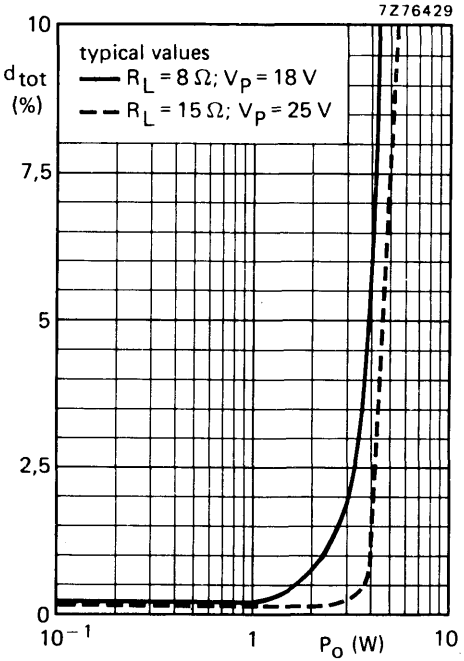


Fig. 4 Total harmonic distortion as a function of output power.

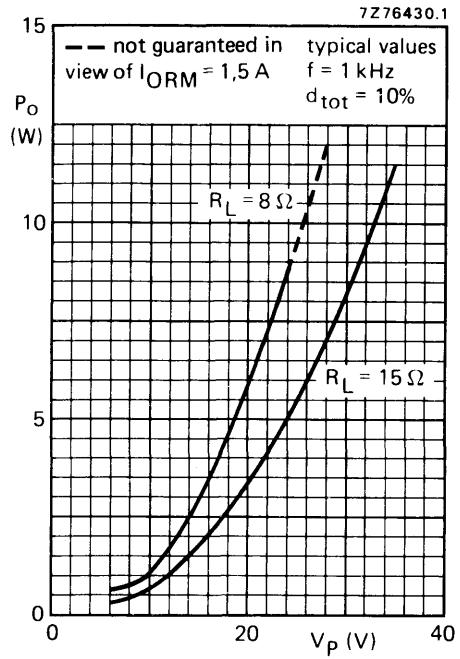


Fig. 5 Output power as a function of supply voltage.

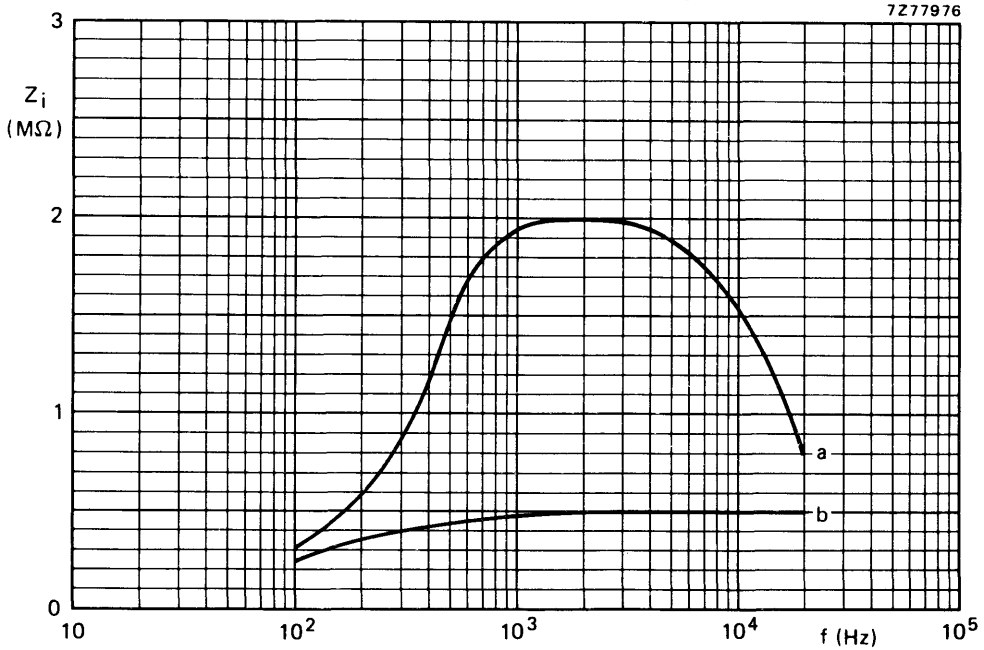


Fig. 6 Input impedance as a function of frequency; curve a for C = 1 μF, R = 0 Ω; curve b for C = 1 μF, R = 1 kΩ; circuit of Fig. 3; C2 = 10 pF; typical values.

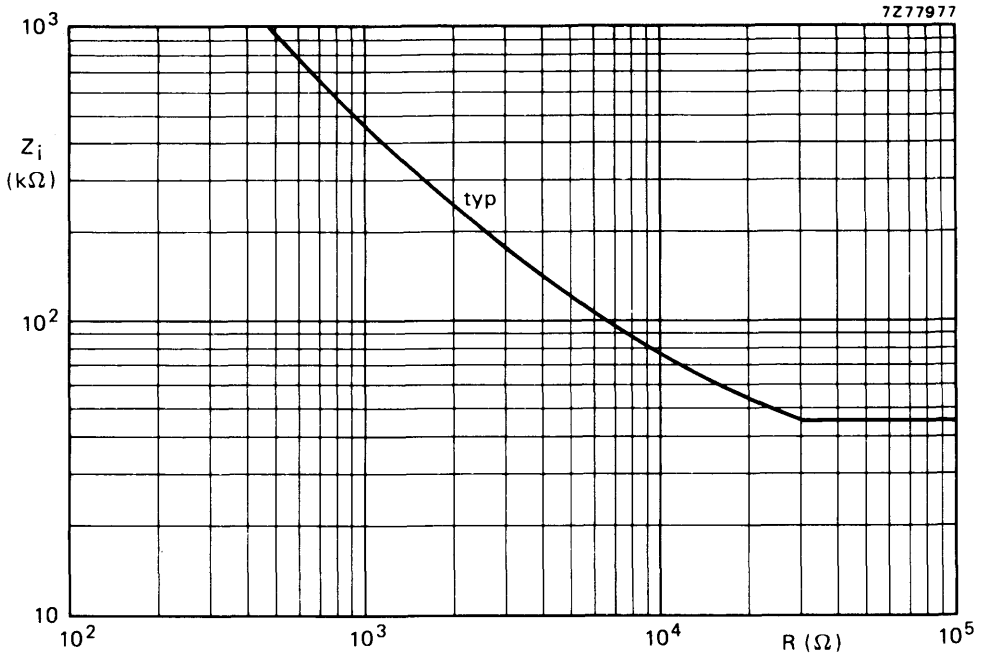


Fig. 7 Input impedance as a function of R in circuit of Fig. 3; C = 1 μF; f = 1 kHz.

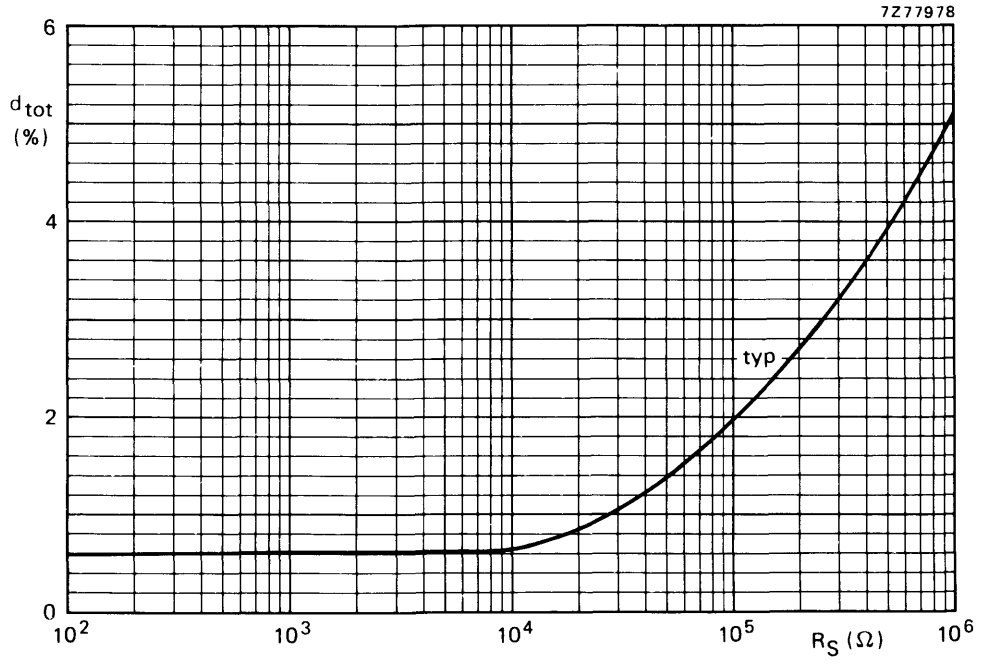


Fig. 8 Total harmonic distortion as a function of R_S in the circuit of Fig. 3; P_o = 3,5 W; f = 1 kHz.

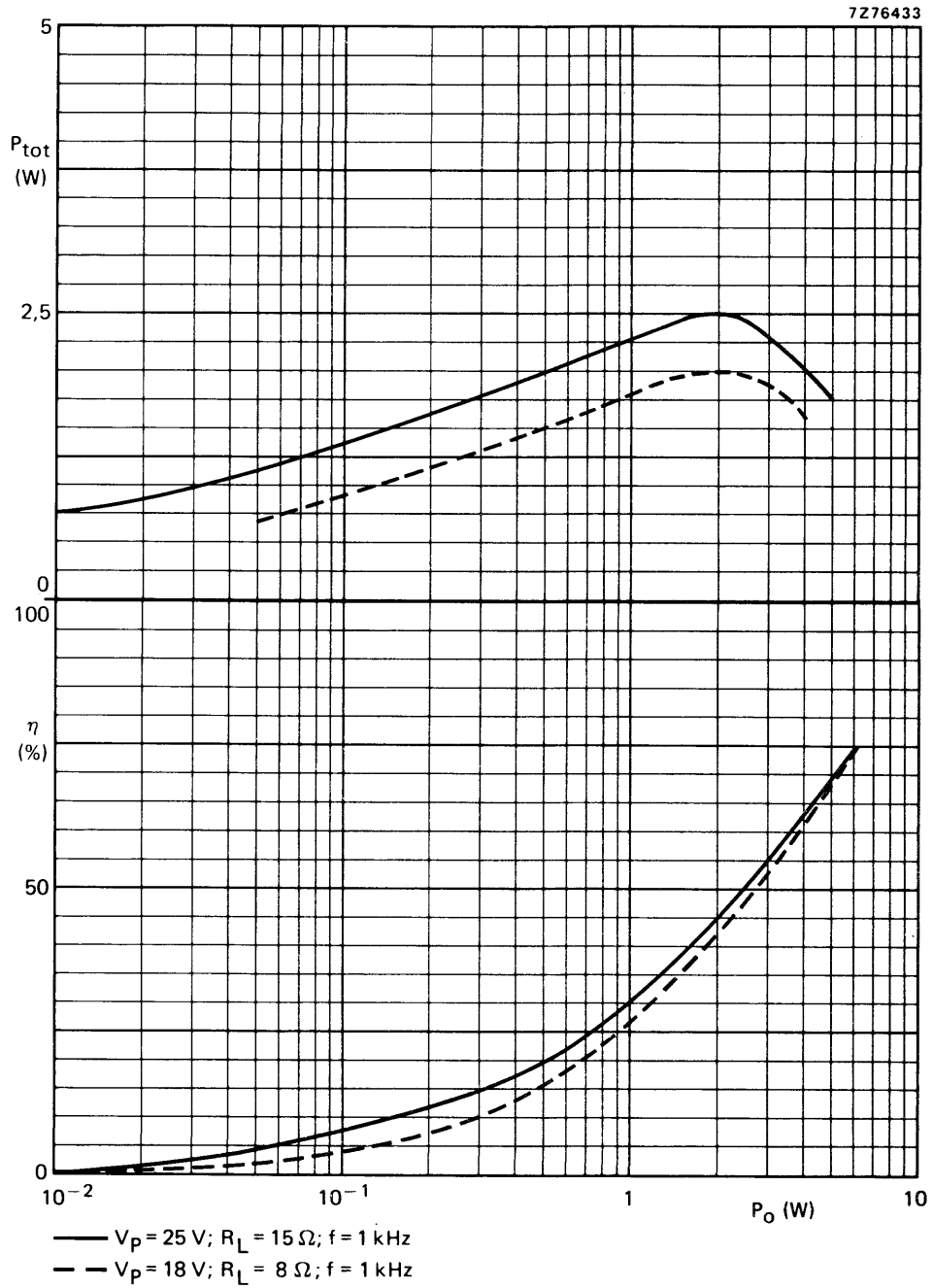


Fig. 9 Total power dissipation and efficiency as a function of output power.

APPLICATION INFORMATION

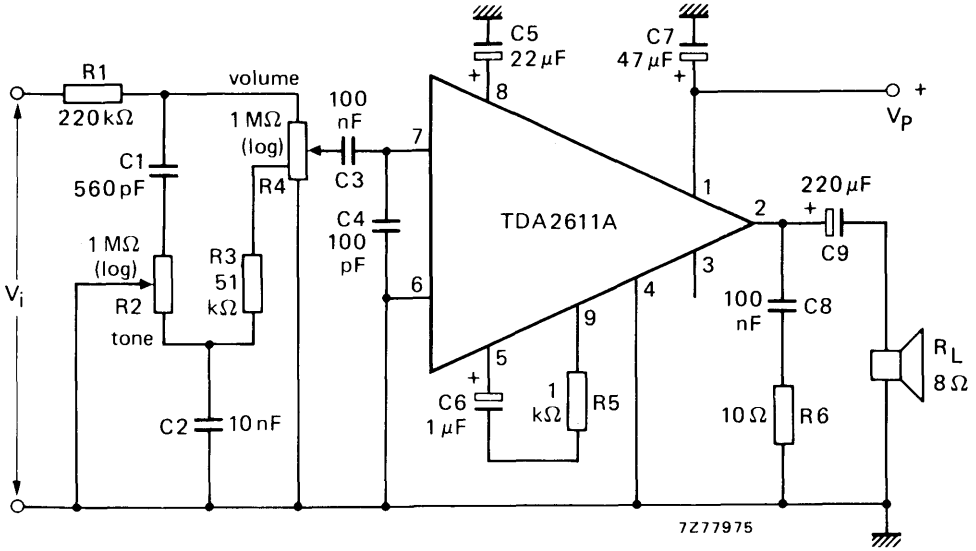


Fig. 10 Ceramic pickup amplifier circuit.

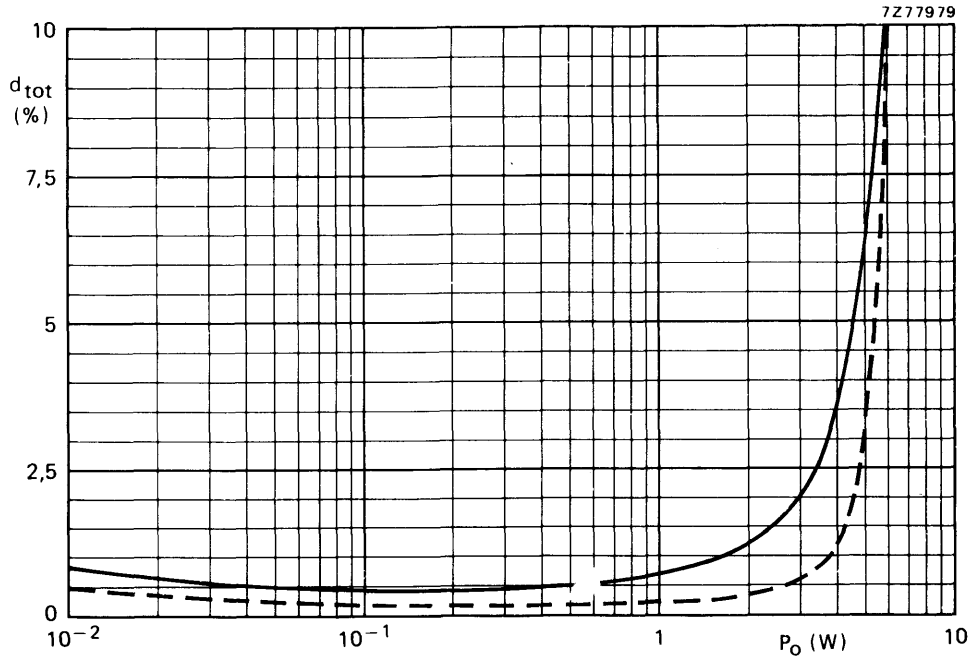


Fig. 11 Total harmonic distortion as a function of output power; —— with tone control; – – – without tone control; in circuit of Fig. 10; typical values.

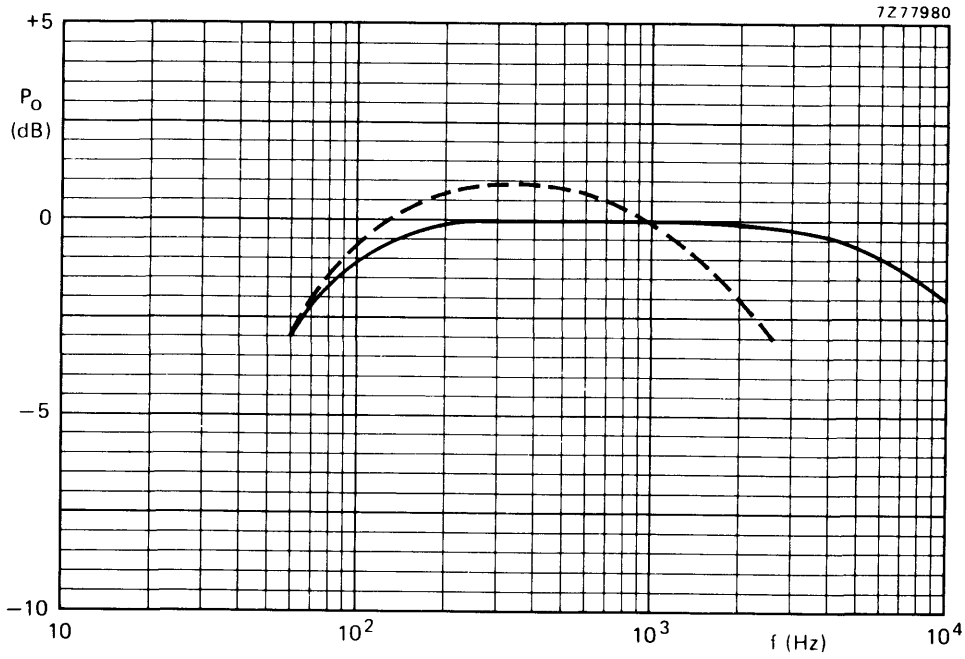


Fig. 12 Frequency characteristics of the circuit of Fig. 10; —— tone control max. high; – – – tone control min. high; P_o relative to 0 dB = 3 W; typical values.

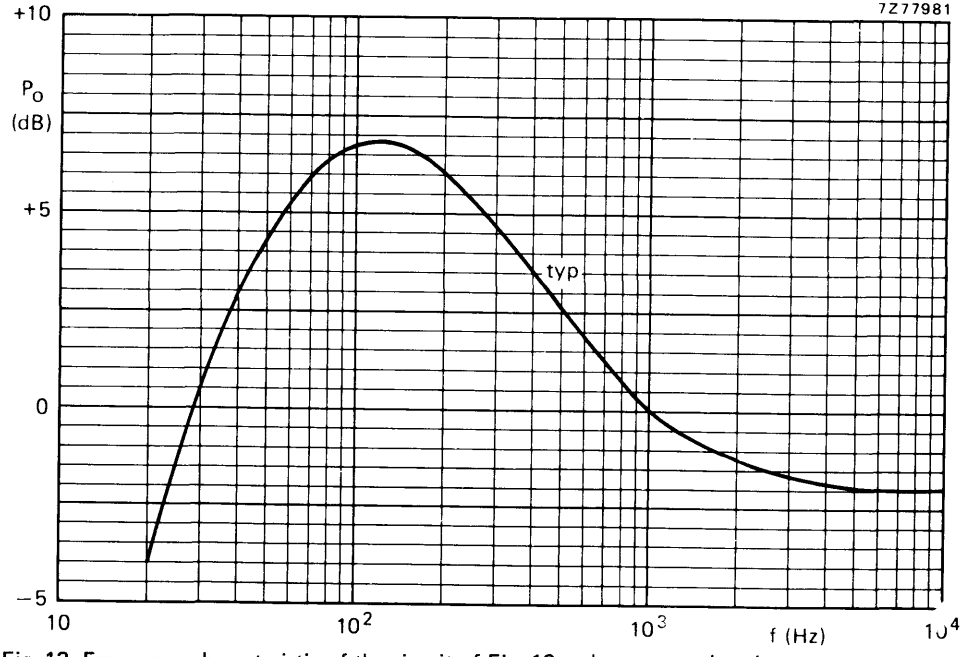


Fig. 13 Frequency characteristic of the circuit of Fig. 10; volume control at the top; tone control max. high.

6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA2613 is a hi-fi audio power amplifier encapsulated in a 9-lead SIL plastic power package. The device is especially designed for mains fed applications (e.g. tv and radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 40 V
Output power at THD = 0,5%, V_P = 24 V	P_o	typ.	6 W
Voltage gain	G_v	typ.	30 dB
Supply voltage ripple rejection	SVRR	typ.	60 dB
Noise output voltage	$V_{no(rms)}$	typ.	70 μV

PACKAGE OUTLINE

TDA2613: 9-lead SIL; plastic power (SOT110B).

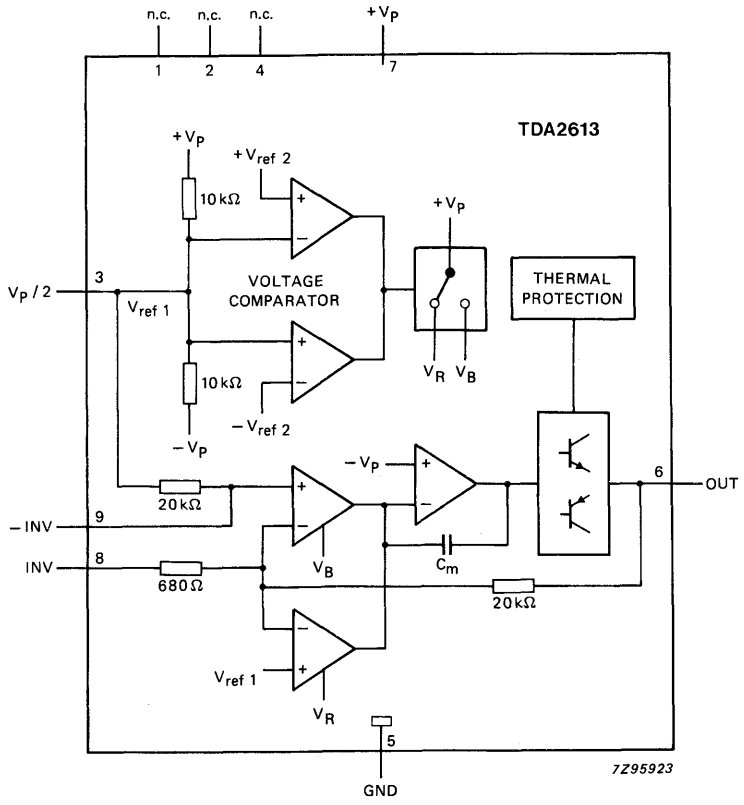


Fig. 1 Block diagram.

PINNING

1.	n.c.	not connected
2.	n.c.	not connected
3.	VP/2	½ VP (asymmetrical) ground (symmetrical)
4.	n.c.	not connected
5.	GND	ground (asymmetrical) negative supply (symmetrical)
6.	OUT	output
7.	+VP	positive supply
8.	INV	inverting input
9.	−INV	non-inverting input

FUNCTIONAL DESCRIPTION

This hi-fi power amplifier is designed for mains fed applications. The device is intended for asymmetrical power supplies, but a symmetrical supply may also be used. An output power of 6 watts (THD = 0,5%) can be delivered into an 8 Ω load with an asymmetrical power supply of 24 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread.

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 4, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifier remains in the DC operating mode but is isolated from the non-inverting input on pin 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	40	V
Non-repetitive peak output current		I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	−65	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note	t_{sc}	–	1	hour

Note to the Ratings

For asymmetrical power supplies (at short-circuiting of the load) the maximum supply voltage is limited to V_P = 28 V. If the total internal resistance of the supply (R_S) ≥ 4 Ω, the maximum unloaded supply voltage is increased to 32 V. For symmetrical power supplies the circuit is short-circuit proof to V_P = ± 20 V.

DEVELOPMENT DATA

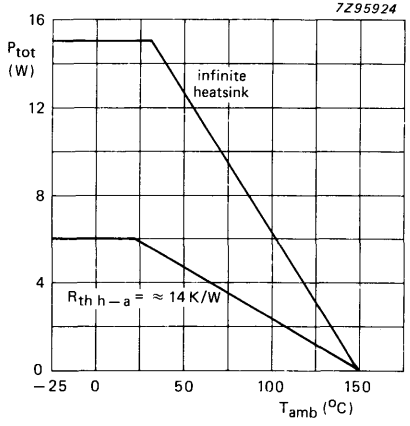


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j\text{-}c} = 8$ K/W

HEATSINK DESIGN EXAMPLE

With derating of 8 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = 24$ V, the measured maximum dissipation is 4,1 W; then, for a maximum ambient temperature of 60 °C, the required thermal resistance of the heatsink is:

$$R_{th\ h\text{-}a} = \frac{150 - 60}{4{,}1} - 8 \approx 14\ \text{K/W}$$

Note: The metal tab (heatsink) has the same potential as pin 5 (GND).

DEVELOPMENT DATA

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	15	24	40	V
input mute mode		V_P	4	–	10	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: asymmetrical power supply; test circuit as per Fig. 4; V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	10	20	35	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8,0	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5%; note 1	B	–	20 to 16 k	–	Hz
Voltage gain		G_v	29	30	31	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Supply voltage ripple rejection	note 2	SVRR	40	50	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to $V_P/2$	V_{os}	–	30	200	mV
Input mute mode: asymmetrical power supply; test circuit as per Fig. 4; V_P = 8 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	5	15	20	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Supply voltage ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to $V_P/2$	V_{os}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: symmetrical power supply; test circuit as per Fig. 3; $V_P = \pm 12$ V; $R_L = 8\ \Omega$; $T_{amb} = 25\ ^oC$; f = 1 kHz						
Total quiescent current		I_{tot}	10	20	35	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	$P_o = 4$ W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B	–	40 to 16 k	–	Hz
Voltage gain		G_v	29	30	31	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	$R_S = 2\ k\Omega$	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\lvert Z_i \rvert$	14	20	26	$k\Omega$
Supply voltage ripple rejection		SVRR	40	60	–	dB
DC output offset voltage	with respect to ground	V_{os}	–	30	200	mV

Notes to the characteristics

1. Power bandwidth at $P_{o\ max}$ −3 dB.
2. Ripple rejection at $R_S = 0\ \Omega$, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

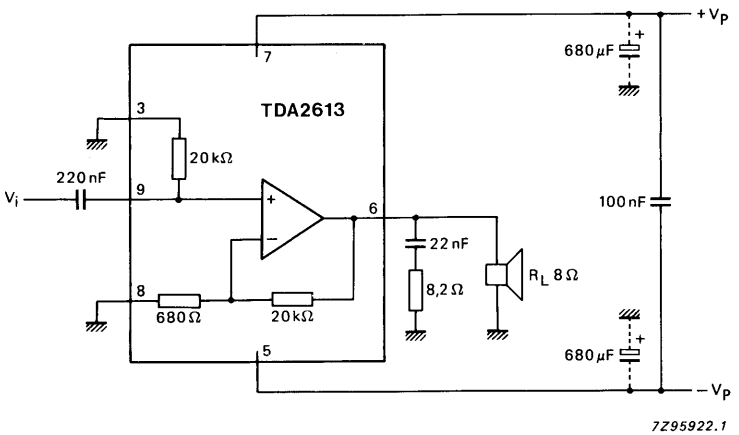


Fig. 3 Test and application circuit; symmetrical power supply.

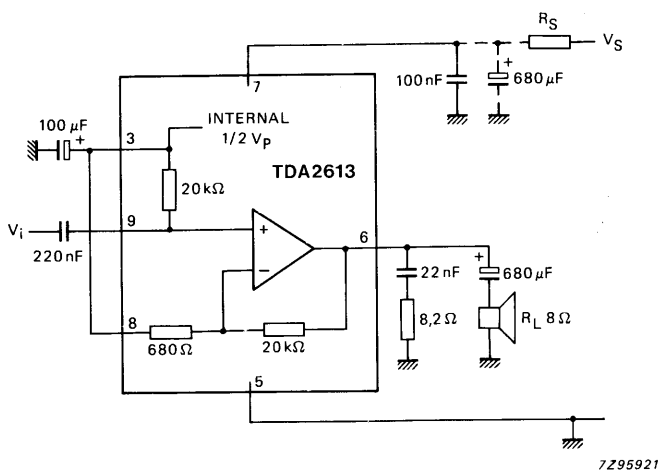


Fig. 4 Test and application circuit; asymmetrical power supply.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting input (pin 9) is disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 5).

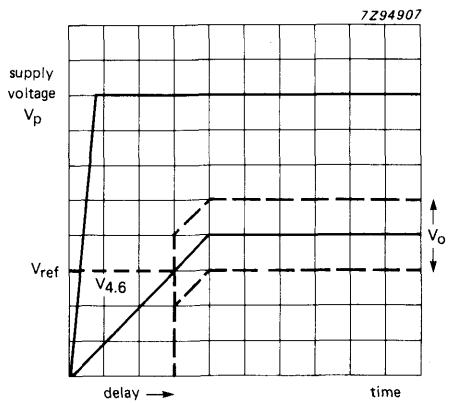


Fig. 5 Input mute circuit; time delay.

INFRARED RECEIVER

The TDA3047 is for infrared reception with low power consumption.
The difference between the TDA3047 and TDA3048 is the polarity of the output signal.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2\text{-}15(p\text{-}p)}$		0,03 to 200 mV
Output signal (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$	typ.	4,5 V

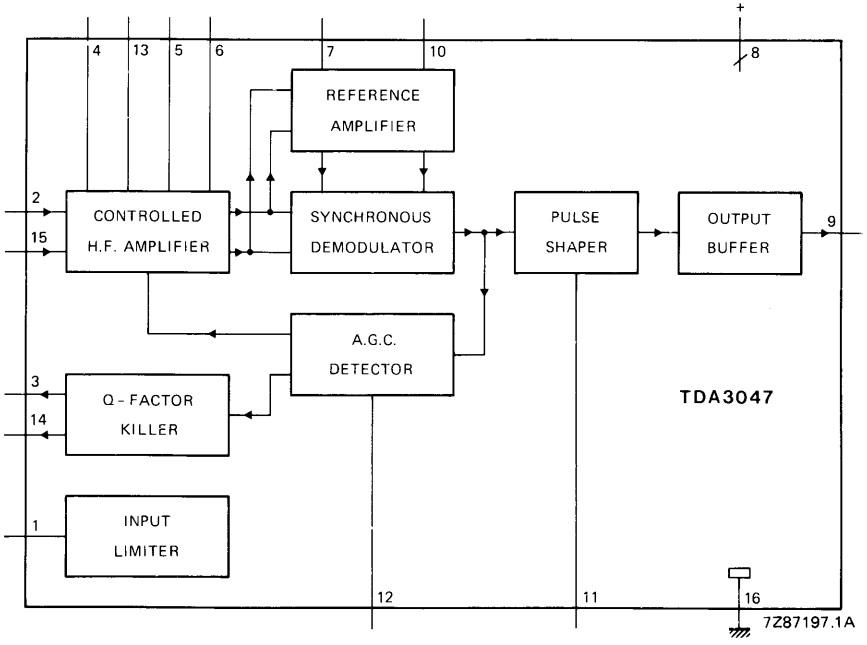


Fig. 1 Block diagram of TDA3047.

PACKAGE OUTLINES

TDA3047P: 16-lead DIL; plastic (SOT38).
TDA3047T: 16-lead mini-pack; plastic (SO16L; SOT162A).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of > 75 μA with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *high*.

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0,7 V. Limiting is 0,9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-16}$	max.	13,2 V
Output current pulse shaper (pin 11)	I_{11}	max.	10 mA
Voltages between pins*			
pins 2 and 15	V_{2-15}	max.	4,5 V
pins 4 and 13	V_{4-13}	max.	4,5 V
pins 5 and 6	V_{5-6}	max.	4,5 V
pins 7 and 10	V_{7-10}	max.	4,5 V
pins 9 and 11	V_{9-11}	max.	4,5 V
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 125 °C

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8-16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8-16}$	4,65	5,0	5,35	V
Supply current	$I_P = I_8$	1,2	2,1	3,0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2-15(p-p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2-15(p-p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2-15(p-p)}$	0,03	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0{,}5$ μA) (peak-to-peak value)	$V_{2-15(p-p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak value)	$V_{2-15(p-p)}$	28	–	–	mV
Q-killing range			see Fig. 2		
Inputs					
Input voltage (pin 2)	V_{2-16}	2,25	2,45	2,65	V
Input voltage (pin 15)	V_{15-16}	2,25	2,45	2,65	V
Input resistance (pin 2)	R_{2-15}	10	15	20	kΩ
Input capacitance (pin 2)	C_{2-15}	–	3	–	pF
Input limiting (pin 1) at I_1 = 3 mA	V_{1-16}	–	0,8	0,9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9 = 75$ μA	$-V_{9-8}$	–	0,1	0,5	V
Output voltage *low* (pin 9) at $I_9 = 75$ μA	V_{9-16}	–	0,1	0,5	V
Output current; output voltage *high*					
at V_{9-16} = 4,5 V	$-I_9$	75	120	–	μA
at V_{9-16} = 3,0 V	$-I_9$	75	130	–	μA
at V_{9-16} = 1,0 V	$-I_9$	75	140	–	μA
Output current; output voltage *low* at V_{9-16} = 0,5 V	$-I_9$	75	120	–	μA
Output resistance between pins 7 and 10	R_{7-10}	3,1	4,7	6,2	kΩ

Notes

1. Voltage pin 9 is *high*; $-I_9 = 75$ μA.
2. Voltage pin 9 remains *low*.
3. Undistorted output pulse with 100% AM input.

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*)	V_{11-16}	3,75	3,9	4,05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*)	V_{11-16}	3,4	3,55	3,7	V
Hysteresis of trigger levels	ΔV_{11-16}	0,25	0,35	0,45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3,4	5,0	6,6	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at V_{12-16} = 2 V	$-I_3$	2,5	7,5	20	μA
Output current (pin 14) at V_{12-16} = 2 V	$-I_{14}$	2,5	7,5	20	μA

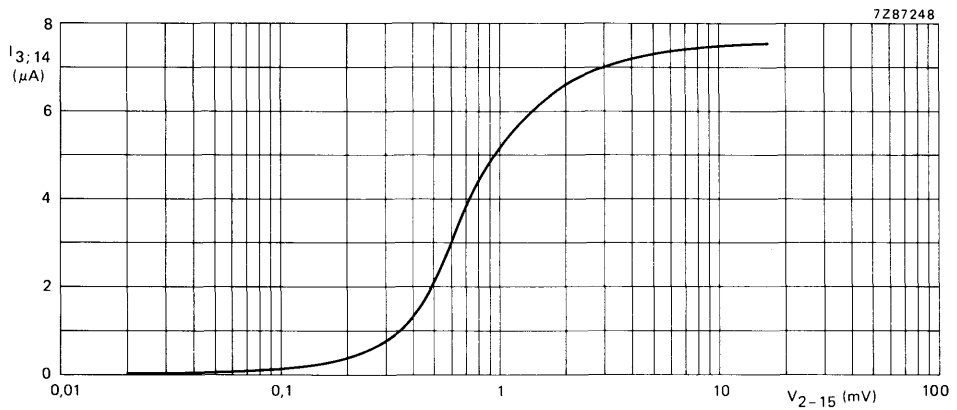
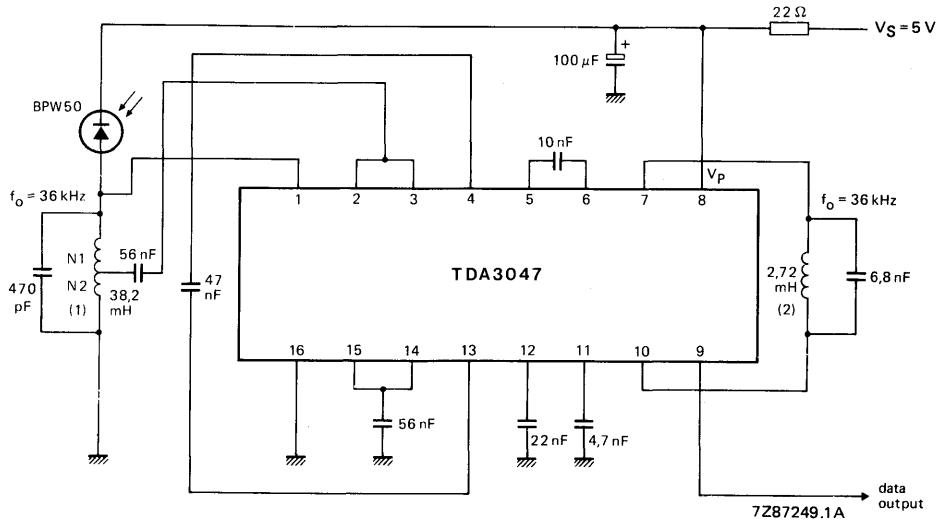


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage (V_{2-15}); $I_{3,14}$ is measured to ground, $V_{2-15(p-p)}$ is a symmetrical square wave. Measured in Fig. 4; V_P = 5 V.

APPLICATION INFORMATION



(1) N1 = 3,21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3047.

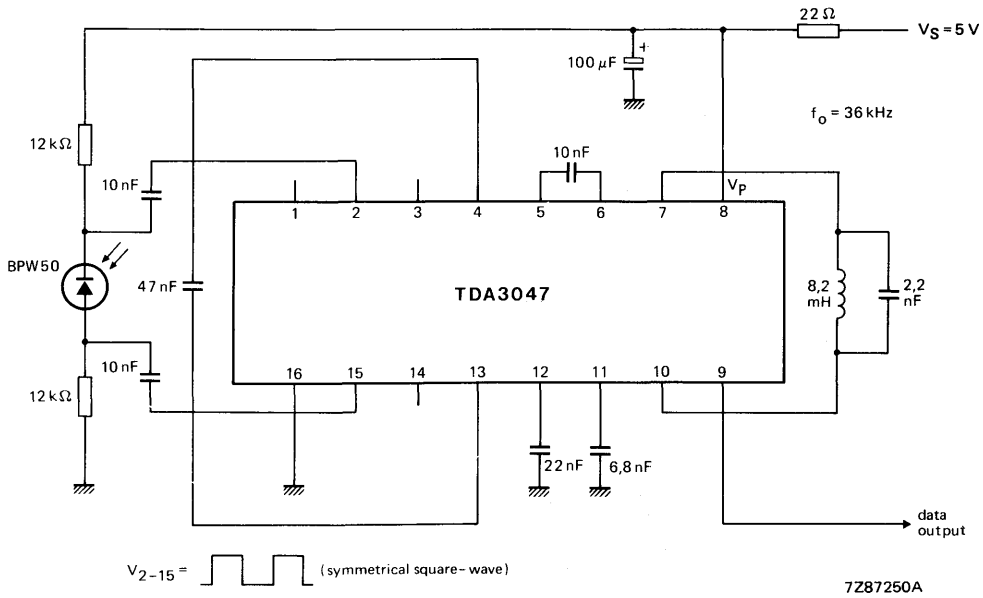


Fig. 4 Wide-band receiver with TDA3047.

For better sensitivity both 12 kΩ resistors may have a higher value.

INFRARED RECEIVER

The TDA3048 is for infrared reception with low power consumption.
The difference between the TDA3048 and TDA3047 is the polarity of the output signal.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2\text{-}15(p\text{-}p)}$		0,03 to 200 mV
Output signal (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$	typ.	4,5 V

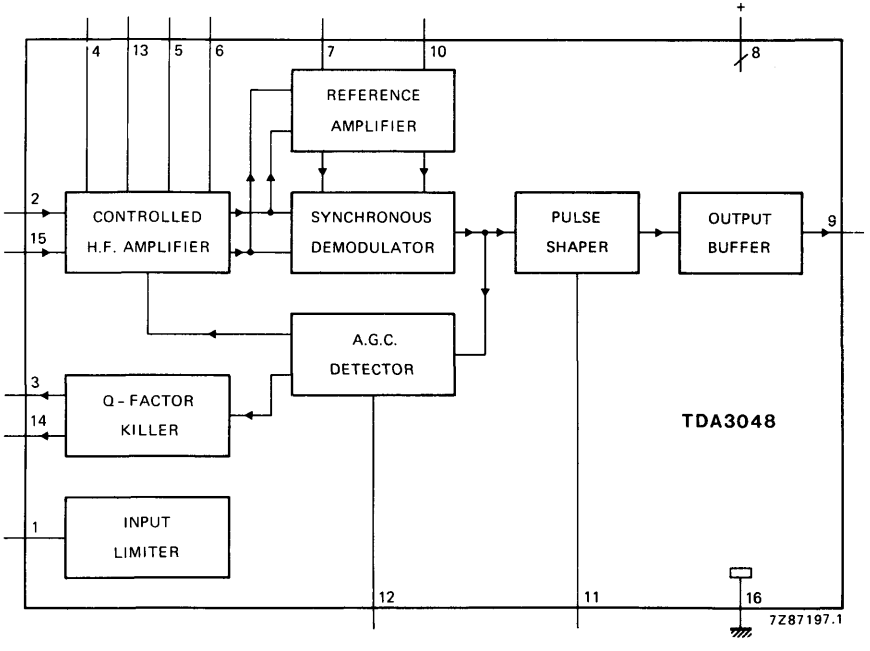


Fig. 1 Block diagram of TDA3048.

PACKAGE OUTLINES

TDA3048P: 16-lead DIL; plastic (SOT38).
TDA3048T: 16-lead mini-pack; plastic (SO16L; SOT162A).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of $> 75\ \mu A$ with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *low*.

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0,7 V. Limiting is 0,9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	max.	13,2 V
Output current pulse shaper (pin 11)	I_{11}	max.	10 mA
Voltages between pins*			
pins 2 and 15	$V_{2\text{-}15}$	max.	4,5 V
pins 4 and 13	$V_{4\text{-}13}$	max.	4,5 V
pins 5 and 6	$V_{5\text{-}6}$	max.	4,5 V
pins 7 and 10	$V_{7\text{-}10}$	max.	4,5 V
pins 9 and 11	$V_{9\text{-}11}$	max.	4,5 V
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 125 °C

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8-16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8-16}$	4,65	5,0	5,35	V
Supply current	$I_P = I_8$	1,2	2,1	3,0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2-15(p-p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2-15(p-p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2-15(p-p)}$	0,03	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0{,}5$ μA) (peak-to-peak value)	$V_{2-15(p-p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak value)	$V_{2-15(p-p)}$	28	–	–	mV
Q-killing range			see Fig. 2		
Inputs					
Input voltage (pin 2)	V_{2-16}	2,25	2,45	2,65	V
Input voltage (pin 15)	V_{15-16}	2,25	2,45	2,65	V
Input resistance (pin 2)	R_{2-15}	10	15	20	kΩ
Input capacitance (pin 2)	C_{2-15}	–	3	–	pF
Input limiting (pin 1) at I_1 = 3 mA	V_{1-16}	–	0,8	0,9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9 = 75$ μA	$-V_{9-8}$	–	0,1	0,5	V
Output voltage *low* (pin 9) at $I_9 = 75$ μA	V_{9-16}	–	0,1	0,5	V
Output current; output voltage *low*					
$-V_{9-8} = 4{,}5$ V	I_9	75	120	–	μA
$-V_{9-8} = 3{,}0$ V	I_9	75	130	–	μA
$-V_{9-8} = 1{,}0$ V	I_9	75	140	–	μA
Output current; output voltage *high*					
$-V_{9-8} = 0{,}5$ V	$-I_9$	75	120	–	μA
Output resistance between pins 7 and 10	R_{7-10}	3,1	4,7	6,2	kΩ

Notes

1. Voltage pin 9 is *low*; $I_9 = 75$ μA.
2. Voltage pin 9 remains *high*.
3. Undistorted output pulse with 100% AM input.

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*	V_{11-16}	3,75	3,9	4,05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*	V_{11-16}	3,4	3,55	3,7	V
Hysteresis of trigger levels	ΔV_{11-16}	0,25	0,35	0,45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3,4	5,0	6,6	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at $V_{12-16} = 2$ V	$-I_3$	2,5	7,5	20	μA
Output current (pin 14) at $V_{12-16} = 2$ V	$-I_{14}$	2,5	7,5	20	μA

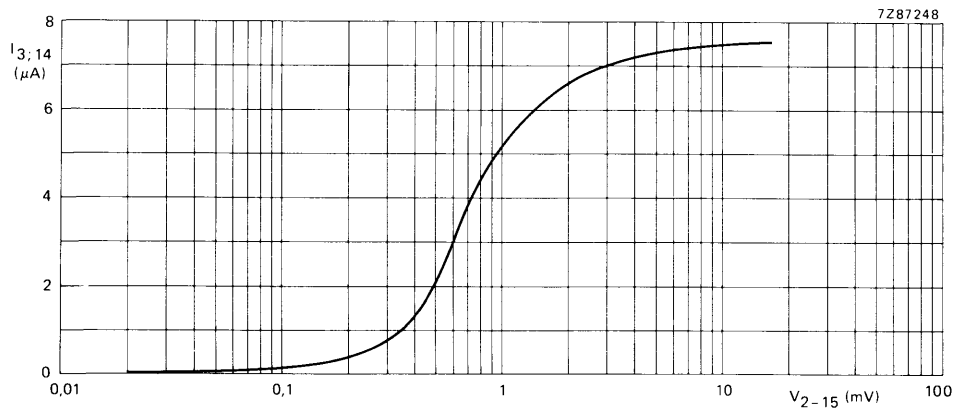
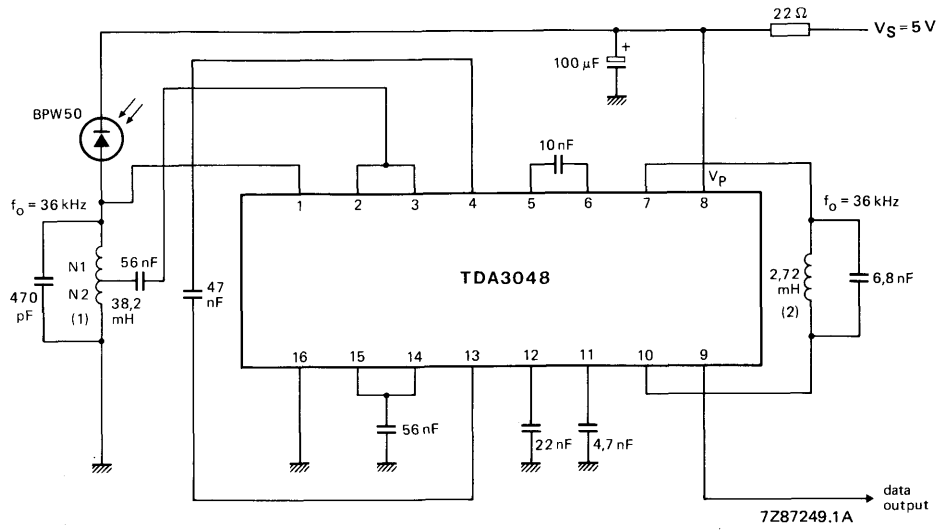


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage (V_{2-15}); $I_{3,14}$ is measured to ground, $V_{2-15(p-p)}$ is a symmetrical square wave. Measured in Fig. 4; $V_P = 5$ V.

APPLICATION INFORMATION



(1) N1 = 3,21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3048.

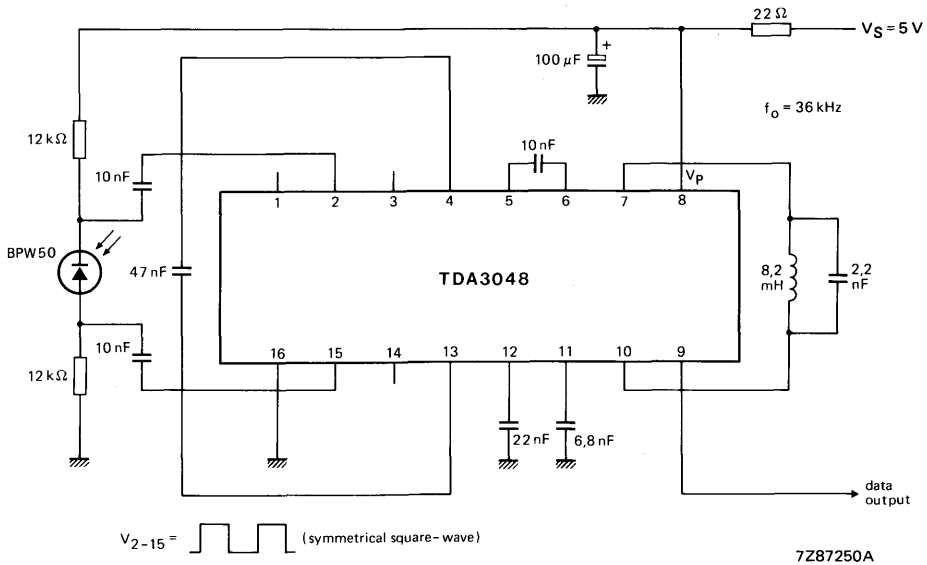


Fig. 4 Wide-band receiver with TDA3048.
For better sensitivity both 12 kΩ resistors may have a higher value.

SPATIAL, STEREO AND PSEUDO-STEREO SOUND CIRCUIT

The TDA3810 integrated circuit provides spatial, stereo and pseudo-stereo sound for radio and television equipment.

Features

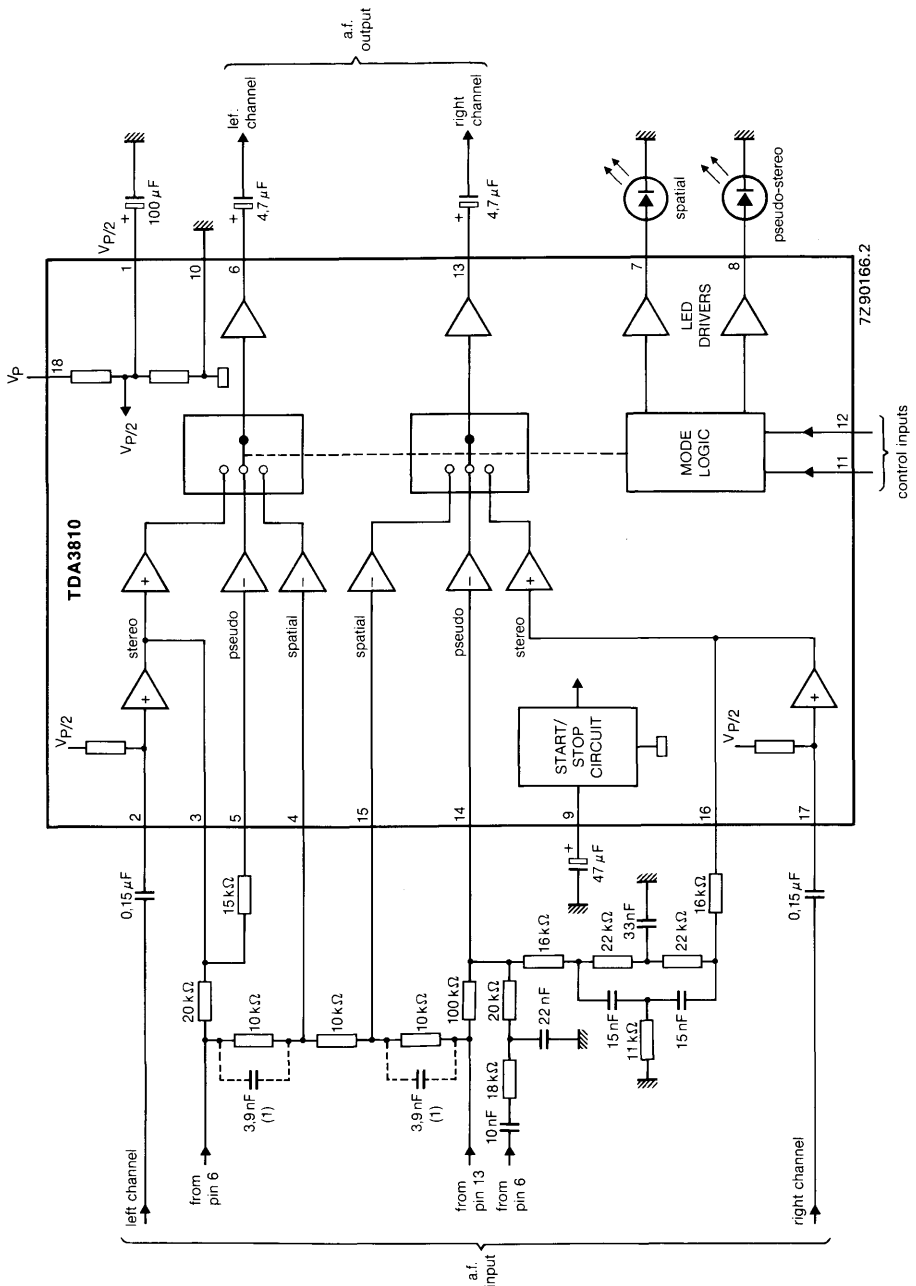
- Three switched functions: spatial (widened stereo image)
  stereo
  pseudo-stereo (artificial stereo from a mono source)
- Offset compensated operational amplifiers to reduce switch noise
- LED driver outputs to facilitate indication of selected operating mode
- Start/stop circuit to reduce switch noise and to prevent LED-flicker
- TTL-compatible control inputs

QUICK REFERENCE DATA

Supply voltage (pin 18)	V_P	typ.	12 V
Supply current (LEDs off)	I_P	typ.	6 mA
Operating ambient temperature range	T_{amb}	0 to	+ 70 °C
Input signal (r.m.s. value)	$V_{i(rms)}$	<	2 V
Total harmonic distortion (stereo)	THD	typ.	0,1 %
Channel separation (stereo)	α	typ.	70 dB
Gain (stereo)	G_V	typ.	0 dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Used in spatial mode for correction of high frequency only (optimal performance).

Fig. 1 Block diagram/test circuit showing external components; for control inputs to pins 11 and 12 see truth table.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)	V_P	max.	18 V
Storage temperature range	T_{stg}	−25 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; test circuit Fig. 1 stereo mode (pin 11 to ground) unless otherwise specified. Output load: $R_{6\text{-}10,13\text{-}10} \geqslant 4{,}7$ kΩ; $C_{6\text{-}10,13\text{-}10} \leqslant 150$ pF.

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 18)	V_P	4,5	–	16,5	V
Supply current	I_P	–	6	12	mA
Reference voltage	V_S	5,3	6	6,7	V
Input voltage (pin 2 or 17) THD = 0,2% (stereo mode)	$V_{i(rms)}$	–	–	2	V
Input resistance (pin 2 or 17)	R_i	50	75	–	kΩ
Voltage gain V_o/V_i	G_v	–	0	–	dB
Channel separation (R/L)	α	60	70	–	dB
Total harmonic distortion f = 40 to 16 000 Hz; $V_{o(rms)}$ = 1 V	THD	–	0,1	–	%
Power supply ripple rejection	RR	–	50	–	dB
Noise output voltage (unweighted) left and right output	$V_{n(rms)}$	–	10	–	μV
SPATIAL MODE (pins 11 and 12 HIGH) Antiphase crosstalk	α	–	50	–	%
Voltage gain	G_v	1,4	2,4	3,4	dB

PSEUDO-STEREO MODE

The quality and strength of the pseudo-stereo effect is determined by external filter components.

parameter	symbol	min.	typ.	max.	unit
CONTROL INPUTS (pins 11 and 12)					
Input resistance	R_i	70	120	–	kΩ
Switching current	$-I_i$	–	35	100	μA
LED DRIVERS (pins 7 and 8)					
Output current for LED	$-I_o$	10	12	15	mA
Forward voltage	V_F	–	–	6	V

Truth table

mode	control input state		LED spatial pin 7	LED pseudo pin 8
	pin 11	pin 12		
Mono pseudo-stereo	HIGH	LOW	off	on
Spatial stereo	HIGH	HIGH	on	off
Stereo	LOW	X	off	off

LOW = 0 to 0,8 V (the less positive voltage)
HIGH = 2 V to 5,5 V (the more positive voltage)
X = don't care

DC MOTOR DRIVE CIRCUIT
WITH MAGNETIC-FIELD DETECTOR

GENERAL DESCRIPTION

The TDA5040T is a bipolar integrated circuit for driving brushless DC motors. It has an on-chip magnetic-field detector (Hall-element), a trigger generator circuit with control signal output, a logic control circuit and a power output stage. Most applications require three interlinked TDA5040T ICs to give full control of motor speed and direction.

Features

- On-chip magnetic-field detector
- Trigger circuit with hysteresis to eliminate instability due to magnetic feedback
- Control signal available externally
- Three-state power output for direct connection to motor field winding
- Current limiting and zener diode protection in power output stage
- Thermal protection
- 8-lead mini-pack package for surface-mounting

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage:						
low power stage		$V_P = V_{6-3}$	5	–	16	V
high power stage		$V_{CC} = V_{5-3}$	0	–	15	V
Quiescent current:	I_O = 0 mA; V_P = 16 V; V_{CC} = 16 V					
	output LOW or floating	I_P	4	6	8	mA
	output HIGH	$I_P + I_{CC}$	6	9	12	mA
Maximum output current		$\pm I_O$	–	–	1,24	A
Storage temperature range		T_{stg}	–55	–	150	°C

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

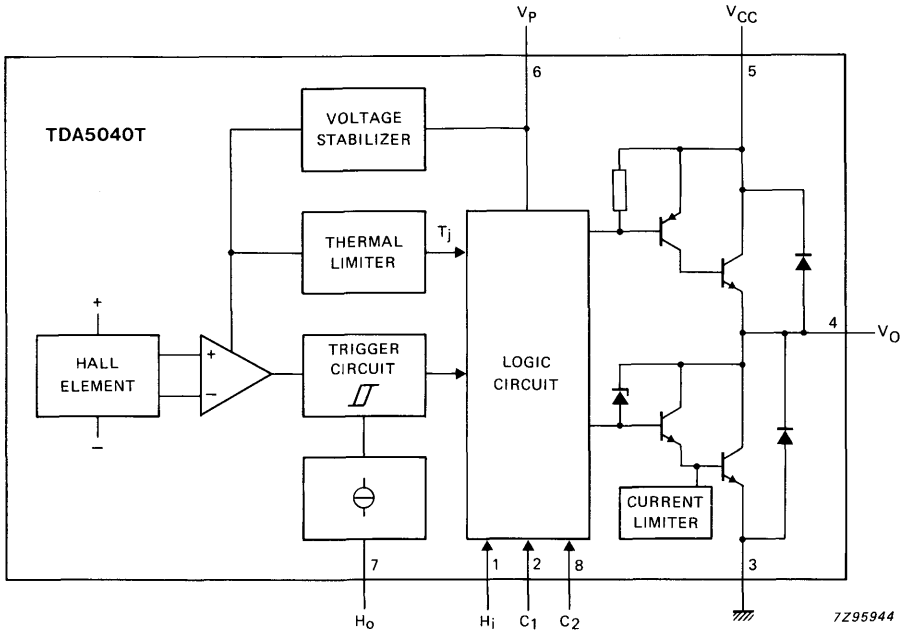


Fig. 1 Block diagram.

PINNING

pin	mnemonic	description
1	H_i	Hall-element input from H_o pin of other TDA5040T ICs
2	C_1	control input to define direction of motor rotation
3	GND	ground (0 V)
4	V_o	power output to motor field winding
5	V_{CC}	positive supply voltage to high power stage
6	V_P	positive supply voltage to low power stage
7	H_o	control output from Hall-element/trigger circuit
8	C_2	control input for power output active or floating

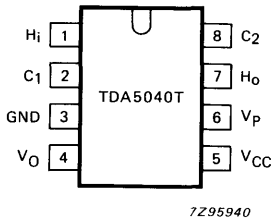


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The Hall-element resistivity changes in the presence of an external magnetic field. Signals obtained from this effect are amplified by a differential amplifier to drive a trigger circuit. The trigger circuit has hysteresis to eliminate instability due to magnetic feedback. The output from the trigger circuit (H_o) is available externally for use as a logic input (H_i) to other TDA5040T circuits in the motor-drive system. The direction of the current at the H_o output depends on the direction of the magnetic field relative to the IC. When the north pole is above the IC and the south pole is below, the current flow is from H_o; when the south pole is above and the north pole is below, then the current flow is into the IC.

The three-state output of the power amplifier stage is HIGH, LOW or floating, depending on the logic input signals H_i, C_1 and C_2, and the direction of the magnetic field (see Table 1). Input C_1 defines the direction of motor rotation and input C_2 is a float command to the output circuit (C_2 = LOW = output floating). Both C_1 and C_2 can be driven by a TTL, CMOS or LOCMOS circuit and both have characteristics that allow up to three inputs to be driven directly by one TTL, CMOS or LOCMOS circuit (e.g. allows a common float line for the three ICs in the system).

Thermal protection is incorporated in the IC. This switches the output to the floating state when the limiting temperature is exceeded. The thermal protection has hysteresis to avoid degradation of the IC during constant short-circuiting of the output.

The power output stage includes a current limiter, and a zener diode which protects the circuit in the event of V_{CC} being disconnected when the output is inductively loaded.

DEVELOPMENT DATA

Table 1 Truth table

T_j	M	C_1	C_2	H_i	H_o	V_o
L	N	HIGH	HIGH	HIGH	HIGH	floating
L	S	HIGH	HIGH	HIGH	LOW	HIGH
L	N	HIGH	HIGH	LOW	HIGH	LOW
L	S	HIGH	HIGH	LOW	LOW	floating
L	N	LOW	HIGH	HIGH	HIGH	floating
L	S	LOW	HIGH	HIGH	LOW	LOW
L	N	LOW	HIGH	LOW	HIGH	HIGH
L	S	LOW	HIGH	LOW	LOW	floating
all other conditions						floating

Where:

T_j = L — junction temperature is within the operating range

M = N — magnetic field north pole is above and south pole is below the IC; magnetic field strength > max. offset + ½ max. hysteresis

M = S — magnetic field south pole is above and north pole is below the IC; magnetic field strength > max. offset + ½ max. hysteresis

H_o,H_i — H_o is directly compatible with H_i, see Fig. 5 for linking arrangements

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltages					
low power stage		$V_P = V_{6-3}$	−0,5	+16,0	V
output stage	resistive load	$V_{CC} = V_{5-3}$	−0,5	+16,0	V
	inductive load	$V_{CC} = V_{5-3}$	0	+15,0	V
Voltage on pins 1,2,7,8		$V_{1,2,7,8-3}$	−0,5	16,0	V
Voltage on pin 4		V_{4-3}	−0,5	$V_{CC}+1$	V
Output current		$\pm I_4$	−	1,24	A
Storage temperature range		T_{stg}	−55	+150	°C
Junction temperature	peak value up to 160 °C during 5 s	T_j	−	150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 200 K/W

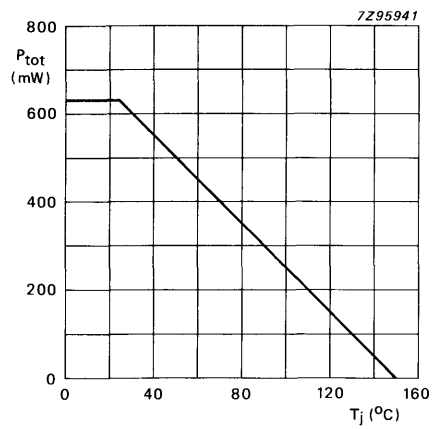


Fig. 3 Power derating curve.

DEVELOPMENT DATA

CHARACTERISTICS

Tested in the circuit of Fig. 4; 5 V $\leqslant V_P \leqslant$ 16 V (min. value is subject to change below 5 V); $-15\ ^{o}C \leqslant T_{amb} \leqslant +60\ ^{o}C$ (derate according to Fig. 3 for applications other than that shown in Fig. 5); all voltages are referred to GND (pin 3)

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Low power stage		$V_P = V_6$	5,0	–	16,0	V
Output stage		$V_{CC} = V_5$	0	–	15,0	V
Quiescent current	pin 4 LOW or floating; I_4 = 0 mA; $V_P = V_{CC}$ = 16 V	I_P	4,0	6,0	8,0	mA
	pin 4 HIGH; I_4 = 0 mA; $V_P = V_{CC}$ = 16 V	I_P+I_{CC}	6,0	9,0	12,0	mA
Hall-element and trigger stage						
Offset		M_{offset}	−15	–	+15	mT*
Hysteresis	using output H_o or V_o	M_{hys}	4,5	8,5	12,0	mT*
Hall output H_o (pin 7)						
Output current	V_P = 12 V; T_{amb} = 25 °C					
LOW	0,7 V $\leqslant V_7 \leqslant V_P$−0,25 V	I_{OL}	7	13	19	μA
HIGH	$V_7 \leqslant V_P$−0,25 V	$-I_{OH}$	7	13	19	μA
Temperature dependency		$\Delta I_7/\Delta T$	–	0,15	–	%/K
Supply voltage dependency		$\Delta I_7/\Delta V_P$	–	4	–	%/V
Hall input H_i (pin 1)						
Input voltage LOW	$-I_1 \geqslant 7\mu A$	V_{IL}	2,48	2,8	3,15	V
Input voltage HIGH	$I_1 \geqslant 7\mu A$	V_{IH}	3,7	4,2	4,75	V
Input switching level to drive output V_o in accordance with Table 1	referred to calculated switching level $(V_{IH}-V_{IL})/2$	V_{Isw}	0	100	200	mV

* 1T = 1 Tesla = 1 Weber/m² = 10000 Gauss

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Logic inputs C_1, C_2 (pins 2, 8)						
Input voltage LOW		V_{IL}	–	–	1	V
Input voltage HIGH		V_{IH}	2	–	–	V
Input current LOW	$V_{2,8}$ = 0,4 V	$-I_{IL}$	5	15	30	μA
Input current HIGH	$V_{2,8}$ = 16 V	I_{IH}	–	–	2	μA
Power output V_O (pin 4)	I_4 = 1 ms pulses					
Output voltage LOW	I_4 = 400 mA; duty factor = 10%	V_{OL}	–	1,1	1,25	V
Temperature dependency of V_{OL}		$\Delta V_{OL}/\Delta t$	–	−0,93	–	mV/K
Output voltage HIGH	$-I_4$ = 500 mA; duty factor = 10%	V_{OH}	$V_{CC}-1,35$	$V_{CC}-1,1$	–	V
Temperature dependency of V_{OH}		$\Delta V_{OH}/\Delta t$	–	+3,6	–	mV/K
Output current LOW	limited internally	I_{OL}	0,5	–	1,2	A
Output current floating	$V_4 = V_{CC}$ = 16 V	I_{float}	–	–	1,0	mA
	V_4 = 0 V; V_{CC} = 16 V	$-I_{float}$	–	–	1,0	mA
Load resistance	pin 4 to pin 5	R_L	6,0	–	–	Ω
Thermal protection						
Junction temperature for switch-off		$T_{j\ sw\text{-}off}$	130	–	160	°C
Junction temperature for switch-on		$T_{j\ sw\text{-}on}$	90	–	140	°C
Switching hysteresis		$T_{j\ hys}$	20	30	40	°C

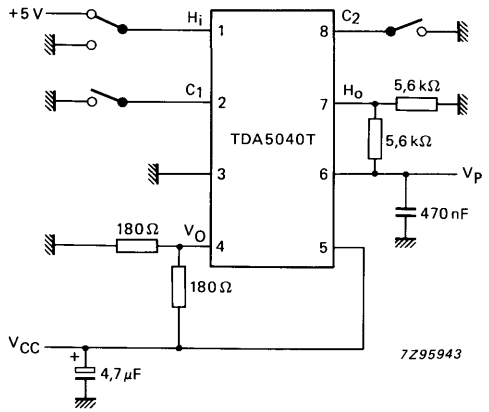
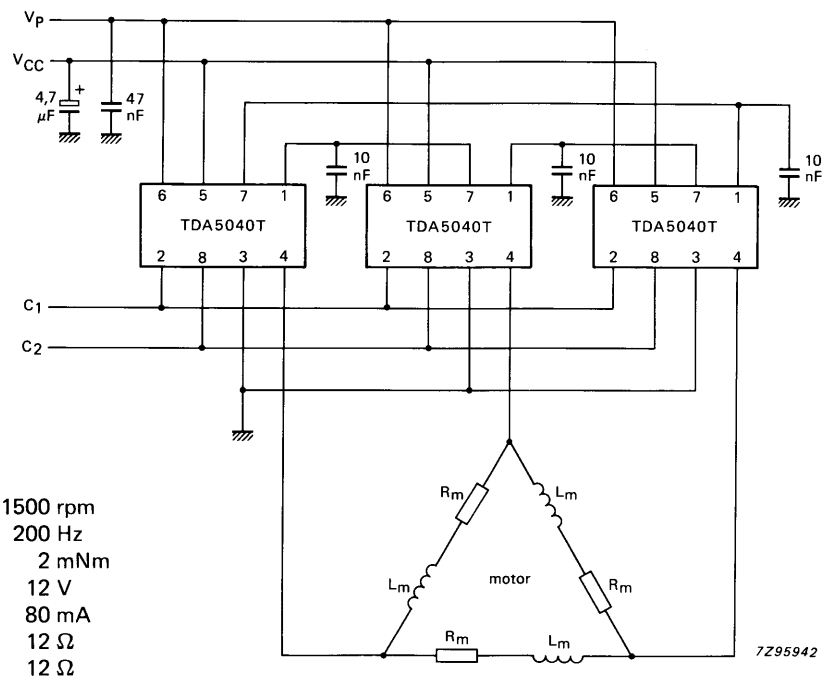


Fig. 4 Test circuit.

APPLICATION INFORMATION

DEVELOPMENT DATA



n_{nom} = 1500 rpm
f_{nom} = 200 Hz
T_{nom} = 2 mNm
V_P = 12 V
I_{CC} = 80 mA
R_m = 12 Ω
X_m = 12 Ω
EMF = 4 V

Fig. 5 Typical application circuit.

PHOTO DIODE SIGNAL PROCESSOR FOR COMPACT DISC PLAYERS

GENERAL DESCRIPTION

The TDA5708 is a bipolar integrated circuit designed for use in compact disc players with a single spot read-out system. It amplifies the photo-diode signals and processes the error signals for the focus- and radial control network.

Features

- Data amplifier with equalizer and A.G.C.
- Offset-free pre-amplifier with A.G.C. for the servo signals
- Trackloss and drop-out detection
- Normalizing focus error output signal to minimize radial error interference
- Laser supply amplifier and reference source
- Possibility for car application
- Single and dual supply application
- TTL compatible digital input/outputs

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	8 to 12	V
Quiescent supply current	I_Q	typ. 11	mA
HF input current (peak-to-peak value) for $V_{HFout(p-p)}$	$I_{HFin(p-p)}$	typ. 8	μA
LF input current (for each diode input)	I_D	typ. 2	μA
Laser supply output current	I_{L0}	typ. 2	mA
Operating ambient temperature range	T_{amb}	−30 to +85	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

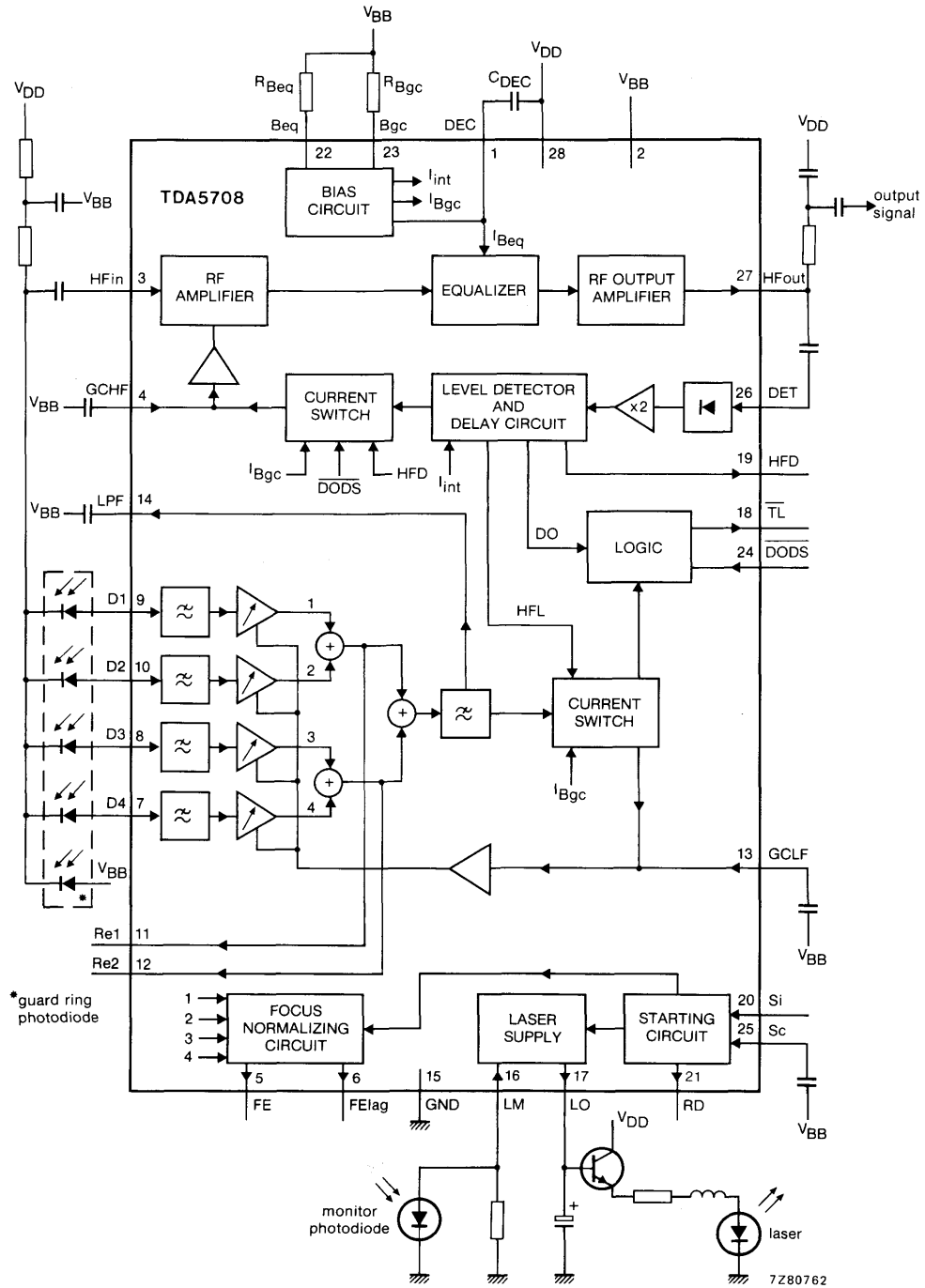


Fig. 1 Block diagram.

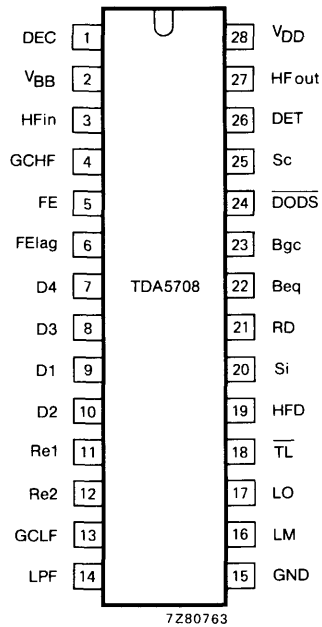


Fig. 2 Pinning diagram; for pin description see next page.

DEVELOPMENT DATA

PIN DESCRIPTION

Pin No.	Symbol	Description
1.	DEC	Decoupling bias-current HF part.
2	V_{BB}	Negative supply connection (also substrate connection).
3	HFin	HF current input.
4	GCHF	Gain control input of HF amplifier. Current output from HF amplitude detector.
5	FE	Current output of normalized, switched focus error signal.
6	FElag	Current output of switched focus error signal, intended for lag network.
7, 8	D4, D3	LF photo diode current input.
9, 10	D1, D2	LF photo diode current input.
11	Re1	Summation of amplified currents D1 and D2.
12	Re2	Summation of amplified currents D3 and D4.
13	GCLF	Gain control input of LF amplifiers. Current output from LF amplitude detector.
14	LPF	Low pass filter for I_{ret}, used in track loss (TL) detector and LF control part ($I_{ret} = I_{Re1} + I_{Re2}$).
15	GND	Laser supply ground. Logic ground.
16	LM	Laser monitor diode input.
17	LO	Laser amplifier current output.
18	$\overline{TL}$	Track loss.
19	HFD	High frequency detector output.
20	Si	On/off control, laser supply and focus circuitry.
21	RD	Ready signal output; starting up procedure finished.
22	Beq	Bias current input for equalizer and HF input parts.
23	Bgc	Bias current input for HF output part and LF gain control, TL and FE circuitry.
24	$\overline{DODS}$	Drop out detector suppression.
25	Sc	Starting up input.
26	DET	HF detector voltage input.
27	HFout	HF amplifier and equalizer voltage output.
28	V_{DD}	Positive supply voltage.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges		
pin 28 – pin 2	V_{DD}	−0,3 to + 13 V
pin 15 – pin 2	V_{GND}	−0,3 to + 13 V
pin 16 (open loop)	V_{LM}	V_{BB} to V_{DD} V
Total power dissipation	P_{tot}	see Fig. 3
Storage temperature range	T_{stg}	−55 to + 150 °C
Operating ambient temperature range	T_{amb}	−30 to + 85 °C
Operating junction temperature	T_j	max. 150 °C

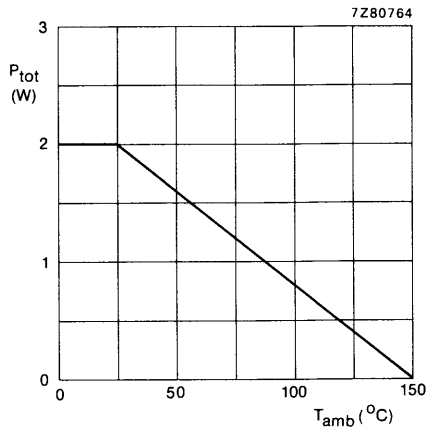


Fig. 3 Power derating curve.

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 10 V; V_{BB} = 0 V; V_{GND} = 0 V; T_{amb} = 25 °C; R_{Beq} = 12 kΩ; R_{Bgc} = 24 kΩ; all voltages with respect to V_{BB}; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage (pin 28)	V_{DD}	8	–	12	V
Laser ground	V_{GND}	V_{BB}	–	V_{DD} −3	V
Quiescent supply current	I_Q	–	11	–	mA
H.F. input (pin 3)					
D.C. voltage level	V_{HFin}	–	1,4	–	V
Input current range (peak-to-peak value) at f = 100 kHz	$I_{HFin(p-p)}$	3	–	10	μA
Input impedance	$\lvert Z_{HFin}\rvert$	0,5	1	2	kΩ
H.F. output (pin 27)					
Output voltage at I_{HFin} = 0 μA; V_{GCHF} = 2,8 V	V_{HFout}	V_{DD}−5	–	V_{DD}−3	V
at I_{HFin} = 0 μA; V_{GCHF} = 6,3 V	V_{HFout}	–	V_{DD} −4,4	–	V
Output voltage (note 1; Fig. 6) (peak-to-peak value) at $I_{HFin(p-p)}$ = 6 μA	$V_{O1(p-p)}$	–	1	–	V
at $I_{HFin(p-p)}$ = 3 to 10 μA	$V_{O(p-p)}$	–	M_1	–	V
Output impedance (note 1; Fig. 6)	$\lvert Z_{HFout}\rvert$	–	50	–	Ω
Bias input (pin 22)					
D.C. voltage level at R_{Beq} = 12 kΩ	V_{Beq}	–	590	–	mV
Input current	I_{Beq}	–	−50	–	μA
Bias input (pin 23)					
D.C. voltage level at R_{Bgc} = 24 kΩ	V_{Bgc}	–	1,28	–	V
Input current	I_{Bgc}	–	−50	–	μA
Decoupling output (pin 1)					
Output voltage	V_{DEC}	–	V_{DD} −1,5	–	V
Output impedance	$\lvert Z_{DEC}\rvert$	–	2	–	kΩ
Level detector input (pin 26)					
D.C. voltage level	V_{DET}	–	0,82	–	V
Input current range	I_{DET}	−100	–	+ 100	μA
Input impedance	$\lvert Z_{DET}\rvert$	–	10	–	kΩ

parameter	symbol	min.	typ.	max.	unit
Reference current (HF part)					
Positive reference current (Fig. 7)	I_{refp}	–	55	–	μA
Negative reference current (Fig. 8; note 13)	I_{refn}	–	M_5	–	μA
Gain control (pin 4)					
Input voltage for:					
minimum h.f. gain	V_{GCHF}	–	2,8	–	V
maximum h.f. gain	V_{GCHF}	–	6,3	–	V
Input impedance at V_{GCHF} = 2,8 to 6,3 V	$\lvert Z_{GCHF}\rvert$	–	10	–	MΩ
Output current					
at I_{DET} = 0; $\overline{DODS}$ = HIGH or LOW	I_{GCHF}	–	−0,4	–	μA
at $I_{DET} < 0{,}5\ I_{refp}$; $\overline{DODS}$ = HIGH or LOW	I_{GCHF}	–	−0,4	–	μA
at $I_{DET} > 0{,}5\ I_{refp}$; $\overline{DODS}$ = HIGH	I_{GCHF}	–	−4,6	–	μA
at $I_{DET} > 0{,}5\ I_{refp}$; $\overline{DODS}$ = LOW	I_{GCHF}	–	−0,4	–	μA
at $I_{DET} < I_{refp}$; $\overline{DODS}$ = HIGH	I_{GCHF}	–	−4,6	–	μA
at $I_{DET} < I_{refp}$; $\overline{DODS}$ = LOW	I_{GCHF}	–	−0,4	–	μA
at $I_{DET} > I_{refp}$; $\overline{DODS}$ = LOW	I_{GCHF}	–	94	–	μA
at $I_{DET} > I_{refp}$; $\overline{DODS}$ = HIGH	I_{GCHF}	–	94	–	μA
at $I_{DET} > 0{,}5\ I_{refn}$; $\overline{DODS}$ = HIGH or LOW	I_{GCHF}	–	−0,4	–	μA
at $I_{DET} < 0{,}5\ I_{refn}$; $\overline{DODS}$ = HIGH	I_{GCHF}	–	−4,6	–	μA
at $I_{DET} > I_{refn}$; $\overline{DODS}$ = HIGH	I_{GCHF}	–	−4,6	–	μA
at $I_{DET} < I_{refn}$; $\overline{DODS}$ = HIGH	I_{GCHF}	–	94	–	μA
HFD output (pin 19)					
Output voltage LOW at I_{HFD} = 400 μA (sink current); $I_{DET} < 0{,}5\ I_{refp}$	V_{HFD}	–	V_{GND}+0,1	V_{GND}+0,4	V
Output voltage HIGH at I_{HFD} = 50 μA (source current); $I_{DET} > 0{,}5\ I_{refp}$	V_{HFD}	V_{GND}+2,4	V_{GND}+9,9	–	V
Output sink current at I_{DET} = 0	I_{HFD}	–	1,5	–	mA
Output source current at $I_{DET} > 0{,}5\ I_{refp}$	I_{HFD}	–	−108	–	μA
Delay time (note 2)	τ_1, τ_2	–	15	–	μs

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
L.F. photo diode inputs (pins 7 to 10) (values given for each input)					
D.C. voltage level	V_D	–	1,5	–	V
Input current range	I_D	0	–	6	μA
Input impedance at 1 MHz; I_D = 1 μA	$\lvert Z_D \rvert$	–	2	–	kΩ
Gain control (pin 13)					
Input voltage for:					
minimum l.f. gain	V_{GCLF}	–	3	–	V
maximum l.f. gain	V_{GCLF}	–	V_{DD} −1,5	–	V
Input impedance	$\lvert Z_{GCLF} \rvert$	–	4	–	MΩ
Output current (note 3)					
at $I_{DET} < 0{,}625\ I_{refp}$	I_{GCLF}	–	$-0{,}1 I_{Bgc}$	–	μA
at $I_{DET} > 0{,}625\ I_{refp}$ $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$	I_{GCLF}	–	$-1{,}1 I_{Bgc}$	–	μA
at $I_{DET} > 0{,}625\ I_{refp}$ $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1\ \mu A$	I_{GCLF}	–	$M_4 - 2{,}1 I_{Bgc}$	–	μA
Re1, Re2 outputs (pin 11, pin 12)					
Output current (see Fig. 9)					
at $I_{D1} = I_{D2} = 0$; $I_{D3} = I_{D4} = 1\ \mu A$; $V_{GCLF} = V_{DD}$	I_{Re2}	–	136	170	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$; $V_{GCLF} = V_{DD}$	I_{Re2}	–	0	–	μA
at $I_{D1} = I_{D2} = 1\ \mu A$; $I_{D3} = I_{D4} = 0$; $V_{GCLF} = V_{DD}$	I_{Re1}	–	136	170	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$; $V_{GCLF} = V_{DD}$	I_{Re1}	–	0	–	μA
Output voltage					
at $V_{GCLF} = V_{DD}$; I_{Re1} = 150 μA	V_{Re1}	–	V_{BB} + 1,4	–	V
at $V_{GCLF} = V_{DD}$; I_{Re2} = 150 μA	V_{Re2}	–	V_{BB} + 1,4	–	V
Output impedance (pin 11)	$\lvert Z_{Re1} \rvert$	–	5	–	MΩ
Output impedance (pin 12)	$\lvert Z_{Re2} \rvert$	–	5	–	MΩ
LPF output (pin 14)					
D.C. voltage level	V_{LPF}	–	3	–	V
Input impedance	$\lvert Z_{LPF} \rvert$	–	2	–	kΩ

parameter	symbol	min.	typ.	max.	unit
FElag output (pin 6)					
Output voltage					
at $V_{Sc} = V_{GCLF} = V_{DD}$; $I_{FElag} = +100\ \mu A$	V_{FElag}	–	–	$V_{BB} + 1$	V
at $V_{Sc} = V_{GCLF} = V_{DD}$; $I_{FElag} = -100\ \mu A$	V_{FElag}	$V_{DD} - 1,5$	–	–	V
Output impedance	$\lvert Z_{FElag} \rvert$	–	4	–	MΩ
Output current (Fig. 10)					
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1\ \mu A$; $V_{Sc} = V_{DD}$	I_{FElag}	–	0	–	μA
at $I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$; $V_{Sc} = V_{DD}$	I_{FElag}	–	−130	–	μA
at $I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$; $V_{Sc} = V_{BB} + 0,7$ V	I_{FElag}	–	0	–	μA
at $I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$; $V_{Sc} = V_{DD}$	I_{FElag}	–	130	–	μA
at $I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$; $V_{Sc} = V_{BB} + 0,7$ V	I_{FElag}	–	0	–	μA
FE output (pin 5)					
Output voltage					
at $V_{Sc} = V_{GCLF} = V_{DD}$; $I_{FE} = +100\ \mu A$	V_{FE}	–	–	$V_{BB} + 1$	V
at $V_{Sc} = V_{GCLF} = V_{DD}$; $I_{FE} = -100\ \mu A$	V_{FE}	$V_{DD} - 1,5$	–	–	V
Output impedance	$\lvert Z_{FE} \rvert$	–	4	–	MΩ
Output current (see Fig. 10)					
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1\ \mu A$; $V_{Sc} = V_{DD}$	I_{FE}	–	0	–	μA
at $I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$; $V_{Sc} = V_{DD}$	I_{FE}	–	−66	–	μA
at $I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$; $V_{Sc} = V_{DD}$	I_{FE}	–	66	–	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1\ \mu A$; $V_{Sc} = V_{BB} + 0,7$ V; V_{Si} = LOW	I_{FE}	–	−300	–	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1\ \mu A$; $V_{Sc} = V_{BB} + 1,4$ V; V_{Si} = LOW	I_{FE}	–	−100	–	μA
$\overline{\text{DODS}}$ logic input (pin 24)					
Switching levels					
input voltage LOW	$V_{\overline{DODS}}$	–	–	$V_{GND} + 0,8$	V
input voltage HIGH	$V_{\overline{DODS}}$	$V_{GND} + 2$	–	–	V
Input source current	$I_{\overline{DODS}}$	–	−29	–	μA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Starting input (pin 25)					
Output voltage					
at V_{Si} = LOW	V_{Sc}	–	–	V_{BB} + 0,7	V
at V_{Si} = HIGH	V_{Sc}	V_{DD} −0,5	–	–	V
Output source current					
at V_{Si} = LOW	I_{Sc}	–	−1	–	μA
Output sink current					
at V_{Si} = HIGH	I_{Sc}	–	1,2	–	mA
Si logic input (pin 20)					
Switching levels					
input voltage LOW	V_{Si}	–	–	V_{GND} + 0,8	V
input voltage HIGH	V_{Si}	V_{GND} + 2	–	–	V
Input source current	I_{Si}	–	−29	–	μA
TL logic output (pin 18)					
Output voltage level LOW (see Table 1)					
at $I_{\overline{TL}}$ = 400 μA (sink current)	$V_{\overline{TL}}$	–	–	V_{GND} + 0,4	V
Output voltage level HIGH (see Table 1)					
at $I_{\overline{TL}}$ = 50 μA (source current)	$V_{\overline{TL}}$	V_{GND} + 2,4	–	–	V
Output sink current					
at $V_{\overline{TL}}$ = LOW	$I_{\overline{TL}}$	–	2	–	mA
Output source current					
at $V_{\overline{TL}}$ = HIGH	$I_{\overline{TL}}$	–	−100	–	μA
Delay times (note 4)	τ_3, τ_4	–	15	–	μs
Delay times (note 4)	τ_5, τ_6	–	15	–	μs
RD logic output (pin 21)					
Output voltage level LOW (see Table 2)					
at I_{RD} = 400 μA (sink current	V_{RD}	–	–	V_{GND} + 0,4	V
Output voltage level HIGH (see Table 2)					
at I_{RD} = 50 μA (source current; V_{Sc} = 3 V; V_{Si} = LOW	V_{RD}	V_{GND} + 2,4	–	–	V
Output sink current					
at V_{Sc} = V_{DD}; V_{Si} = HIGH	I_{RD}	–	2,9	–	mA
Output source current					
at V_{Sc} = V_{DD}; V_{Si} = LOW	I_{RD}	–	−105	–	μA

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
LO output (pin 17) (see Figs 11 and 12)					
Output voltage ($V_{DD} - V_{LO}$)	V_{LO}	0,5	–	25	V
Output impedance	$\lvert Z_{LO} \rvert$	–	95	–	kΩ
Output leakage current at V_{Si} = HIGH	I_{LO}	–	–	−10	μA
Maximum output current at V_{Si} = LOW	I_{LO}	–	−4,5	–	mA
LM input (pin 16) (see Figs 11 and 12)					
Input voltage ($V_{LM} - V_{GND}$) (closed loop conditions)	V_{LM}	170	188	220	mV
Input bias current	I_{LM}	–	–	−2	μA
H.F. part					
D.C. characteristics					
$G1 = \frac{\Delta V_{HFout}}{\Delta I_{HFin}}$; $\lvert I_{HFin} \rvert \leqslant 1\ \mu A$					
at ΔI_{HFin} = 1 μA; V_{GCHF} = 6,3 V	G1(max)	–	$45 \cdot 10^4$	–	V/A
at ΔI_{HFin} = 1 μA; V_{GCHF} = 2,8 V	G1(min)	–	0	–	V/A
A.C. characteristics (see Fig. 13)					
$G2 = 20 \log \frac{V_{01}}{V_{02}}$; (note 5)	G2	–	6	–	dB
Phase of input/output signal at 1 MHz (note 6)	ϕ	–	$\pi/2$	–	rad.
Group delay (note 6) at f_{HFin} = 300 kHz + Δf	$\tau 300$	–	270	–	ns
Flatness (note 6) between 0,1 and 1 MHz	$\Delta\tau$	–	0	–	ns
LF part					
Maximum d.c. gain (note 7; Fig. 9)					
for: $A_1 = \lvert \frac{I_{Re2}}{I_{D3} + I_{D4}} \rvert$; $I_{D1} = I_{D2} = 0$; V_{GCLF} = 6,3 V					
at I_{D3} = 0 μA; I_{D4} = 1 μA	A_1	–	68	–	
at I_{D3} = 1 μA; I_{D4} = 0 μA	A_1	M_2 −10%	M_2	M_2 + 10%	
for: $A_2 = \lvert \frac{I_{Re1}}{I_{D1} + I_{D2}} \rvert$; $I_{D3} = I_{D4} = 0$; V_{GCLF} = 6,3 V					
at I_{D1} = 0 μA; I_{D2} = 1 μA	A_2	M_2 −10%	M_2	M_2 + 10%	
at I_{D1} = 1 μA; I_{D2} = 0 μA	A_2	M_2 −10%	M_2	M_2 + 10%	

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
LF part (continued)					
Minimum d.c. gain (note 8; Fig. 9)					
for: $A_3 = \lvert\frac{I_{Re2}}{I_{D3} + I_{D4}}\rvert$;					
$I_{D1} = I_{D2} = 0$; $V_{GCLF} = 3{,}0$ V					
at $I_{D3} = 0\ \mu A$; $I_{D4} = 1\ \mu A$	A_3	–	0,5	–	
at $I_{D3} = 1\ \mu A$; $I_{D4} = 0\ \mu A$	A_3	$M_3 - 10\%$	M_3	$M_3 + 10\%$	
for: $A_4 = \lvert\frac{I_{Re1}}{I_{D1} + I_{D2}}\rvert$;					
$I_{D4} = I_{D3} = 0$; $V_{GCLF} = 3{,}0$ V					
at $I_{D1} = 0\ \mu A$; $I_{D2} = 1\ \mu A$	A_4	$M_3 - 10\%$	M_3	$M_3 + 10\%$	
at $I_{D1} = 1\ \mu A$; $I_{D2} = 0\ \mu A$	A_4	$M_3 - 10\%$	M_3	$M_3 + 10\%$	
A.C. gain (note 9; Fig. 14)					
for G4 = 20 log P1; $I_{D3} = I_{D4} = 0$					
at $I_{D1} = 0$; $I_{D2(p\text{-}p)} = 1\ \mu A$	G4	–	−3,3	–	dB
at $I_{D1(p\text{-}p)} = 1\ \mu A$; $I_{D2} = 0$	G4	–	−3,3	–	dB
A.C. gain (note 10; Fig. 14)					
for G5 = 20 log P2; $I_{D1} = I_{D2} = 0$					
at $I_{D3} = 0$; $I_{D4(p\text{-}p)} = 1\ \mu A$	G5	–	−3,3	–	dB
at $I_{D3(p\text{-}p)} = 1\ \mu A$; $I_{D4} = 0$	G5	–	−3,3	–	dB
Reference current (closed loop conditions; see Fig. 15)					
$I_{ret} = I_{Re1} + I_{Re2}$ at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 2\ \mu A$	I_{ret}	–	200	–	μA
Laser supply					
Transconductance					
For d.c. (note 11)					
at V_{S1} = LOW	G_{LDC}	–	0,5	–	A/V
at V_{Si} = HIGH	G_{LDC}	–	0	–	A/V
For a.c. (note 12)					
delay time	$\tau 11$	–	tbf	–	ns

Notes to the characteristics

1. H.F. part output voltage and output impedance for closed loop conditions: f_{HFin} = 0,1 to 1 MHz. M_1 is the measured value of V_{O1}.
2. HFD delay times τ_1 and τ_2 measured as shown in Fig. 4.

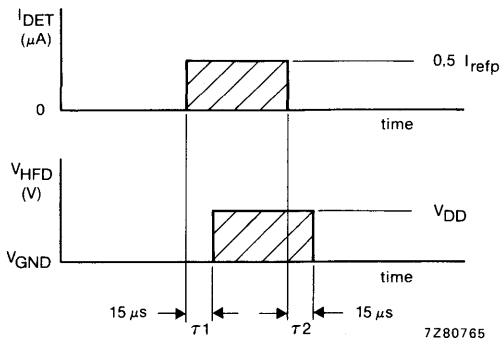


Fig. 4 Delay time τ between I_{DET} and V_{HFD}.

3. $M_4 = \frac{(I_{D1} + I_{D2} + I_{D3} + I_{D4})}{2}$. M_2; (M_2 see note 7) with $I_{D1} = I_{D2} = I_{D3} = I_{D4}$ = 1 μA and Re1, Re2 connected to 1,5 V.
4. $\overline{TL}$ delay times τ_3, τ_4, τ_5 and τ_6 measured as shown in Fig. 5.

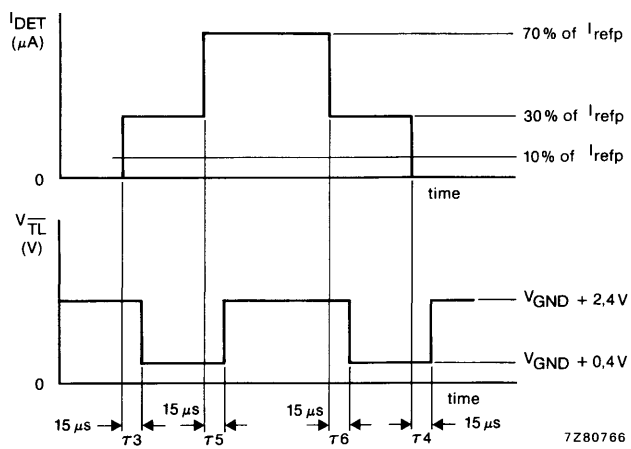


Fig. 5 Delay times between I_{DET} and $V_{\overline{TL}}$.

5. Voltage output signal V_{O1} measured at f_{HFin} = 100 kHz; $I_{HFin(p-p)}$ = 3 μA; V_{GCHF} = 6,3 V. Voltage output signal V_{O2} measured at f_{HFin} = 1 MHz; $I_{HFin(p-p)}$ = 3 μA; V_{GCHF} = 6,3 V.

DEVELOPMENT DATA

Notes to the characteristics (continued)

6. Phase of input/output signal, group delay and flatness measured at $I_{HFin(p\text{-}p)} = 1\ \mu A$; $V_{GCHF} = 6{,}3\ V$.

   Group delay: $\tau = \frac{d\phi}{dw}$; $\Delta f \approx 50\ kHz$.

   Flatness: $\Delta\tau = \tau_{max} - \tau_{min}$.

7. M_2 is the measured value of $A_1 = \left| \frac{I_{Re2}}{I_{D3} + I_{D4}} \right|$

   for $I_{D1} = I_{D2} = I_{D3} = 0$; $I_{D4} = 1\ \mu A$ and $V_{GCLF} = 6{,}3\ V$.

8. M_3 is the measured value of $A_3 = \left| \frac{I_{Re2}}{I_{D3} + I_{D4}} \right|$

   for $I_{D1} = I_{D2} = I_{D3} = 0$; $I_{D4} = 1\ \mu A$ and $V_{GCLF} = 3{,}0\ V$.

9. P1 is the measured value of $\frac{I_{Re1}(1)}{I_{D1}(1) + I_{D2}(1)} \cdot \frac{I_{D1}(2) + I_{D2}(2)}{I_{Re1}(2)}$

   Where:

   (1) are the current levels at $f_i = 25\ kHz$.
   (2) are the current levels at $f_i = 1\ kHz$.

   Measured taken at $V_{GCLF} = 6{,}3\ V$.

10. P2 is the measured value of $\frac{I_{Re2}(1)}{I_{D3}(1) + I_{D4}(1)} \cdot \frac{I_{D3}(2) + I_{D4}(2)}{I_{Re2}(2)}$

    Where:

    (1) are the current levels at $f_i = 25\ kHz$.
    (2) are the current levels at $f_i = 1\ kHz$.

    Measured taken at $V_{GCLF} = 6{,}3\ V$.

11. Laser supply transconductance for d.c.

    $G_{LDC} = \frac{\Delta I_{LO}}{\Delta V_{LM}}$ $(0 < -I_{LO} < 2\ mA)$.

12. Laser supply transconductance for a.c.

    $G_{LAC} = G_{LDC} \cdot \frac{1}{1 + S \cdot \tau 11}$

    Where: S is the laplace operator in the frequency domain.

13. M_5 is the measured value of I_{refp}.

Table 1 Test conditions for track loss output ($\overline{TL}$)

conditions	$\overline{DODS}$	inputs		output level
		$I_{D(tot)}$	I_{DET}	$\overline{TL}$
1	HIGH	$< 4{,}9\ I_{Bgc}$	independent	HIGH
2	HIGH	$> 5{,}1\ I_{Bgc}$	10% of I_{refp}	HIGH
3	HIGH	$> 5{,}1\ I_{Bgc}$	30% of I_{refp}	LOW
4	HIGH	$> 5{,}1\ I_{Bgc}$	70% of I_{refp}	HIGH
5	LOW	$< 4{,}9\ I_{Bgc}$	independent	HIGH
6	LOW	$> 5{,}1\ I_{Bgc}$	10% of I_{refp}	LOW
7	LOW	$> 5{,}1\ I_{Bgc}$	30% of I_{refp}	LOW
8	LOW	$> 5{,}1\ I_{Bgc}$	70% of I_{refp}	HIGH

Where:

$\overline{DODS}$ = HIGH $\quad \overline{DODS} \geqslant V_{GND} + 2{,}4$ V.

$\overline{DODS}$ = LOW $\quad \overline{DODS} \leqslant V_{GND} + 0{,}8$ V.

$I_{D(tot)} = (I_{D1} + I_{D2} + I_{D3} + I_{D4}) \cdot G3 \circ G4 \cdot G5$.

For G3, G4, G5 see transfer functions description of TDA5708.

Table 2 Test condition for ready output (RD)

conditions	inputs		output level
	V_{Sc}	V_{Si}	RD
1	$\geqslant 4V_j + V_{OFF}$	HIGH	LOW
2	$\leqslant 4V_j - V_{OFF}$	HIGH	LOW
3	$\geqslant 4V_j + V_{OFF}$	LOW	HIGH
4	$\leqslant 4V_j - V_{OFF}$	LOW	LOW

Where:

$V_{OFF} \approx 120$ mV.

V_j is the junction voltage (0,7 V typ.).

DEVELOPMENT DATA

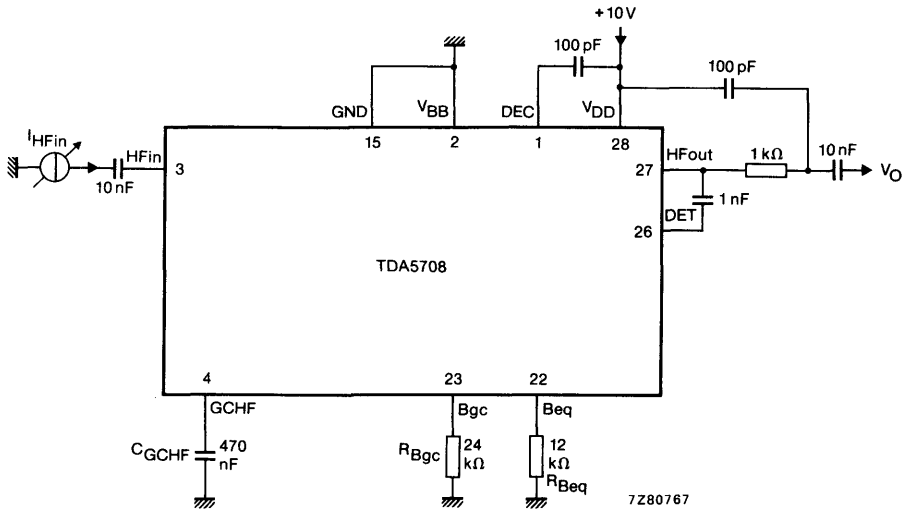
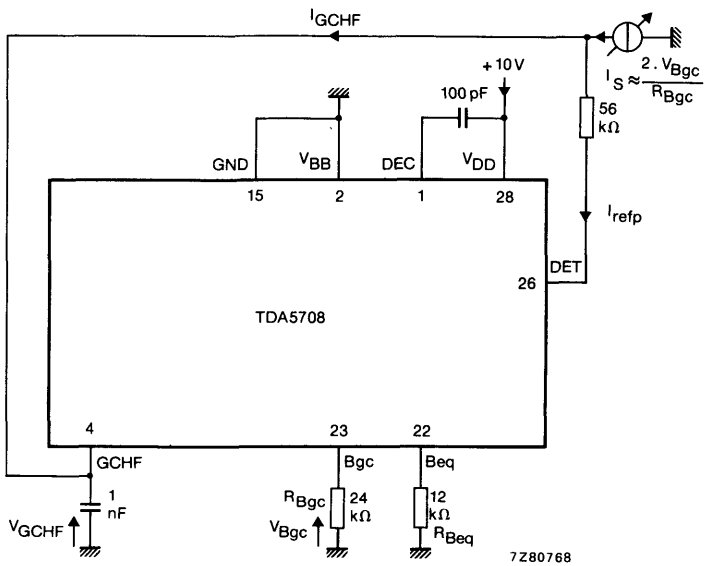
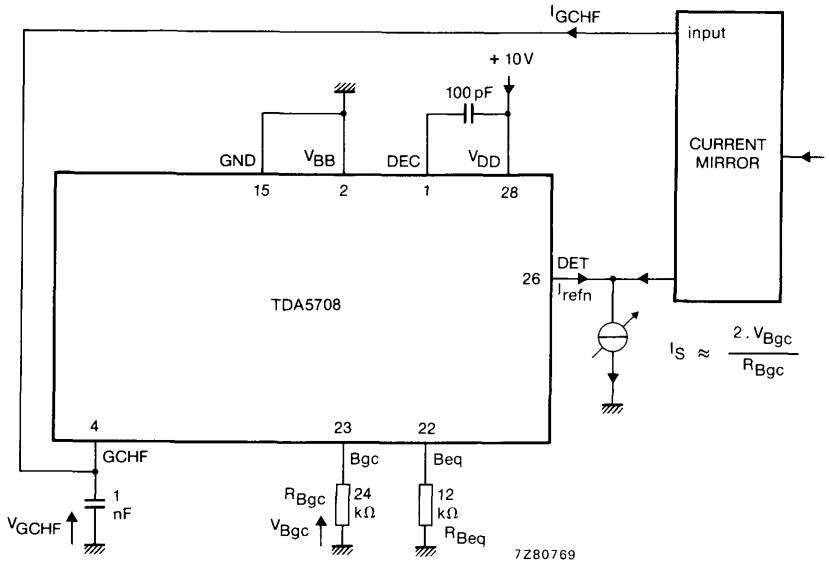


Fig. 6 Test circuit for HF-part; closed-loop condition.



Condition: $\overline{DODS}$ = LOW; V_{GCHF} = 2,8 to 6,3 V.

Fig. 7 Test circuit for positive reference current (I_{refp}).



Condition: $\overline{DODS}$ = LOW; V_{GCHF} = 2,8 to 6,3 V.

Fig. 8 Test circuit for negative reference current (I_{refn}).

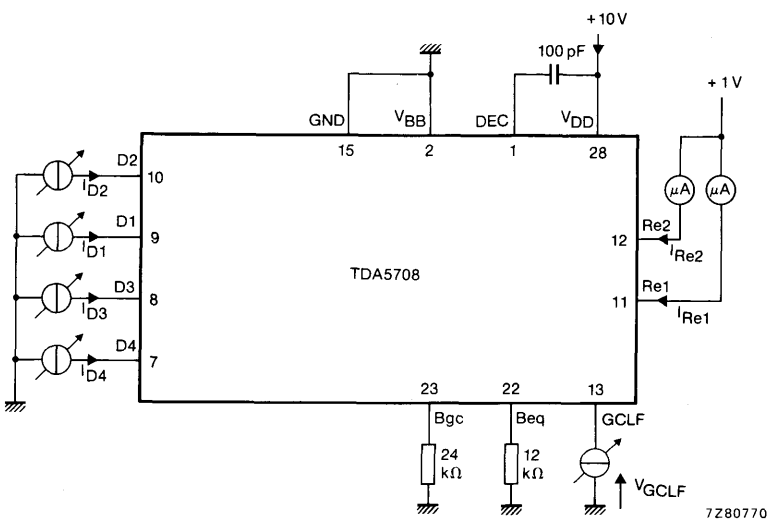


Fig. 9 Test circuit for output current I_{Re1} and I_{Re2}.

DEVELOPMENT DATA

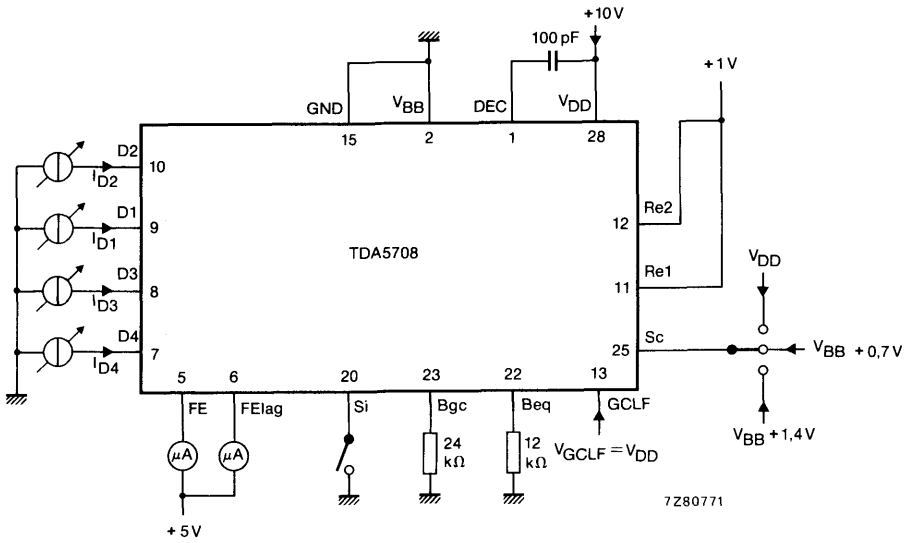


Fig. 10 Test circuit for output current I_{FE} and I_{FElag}.

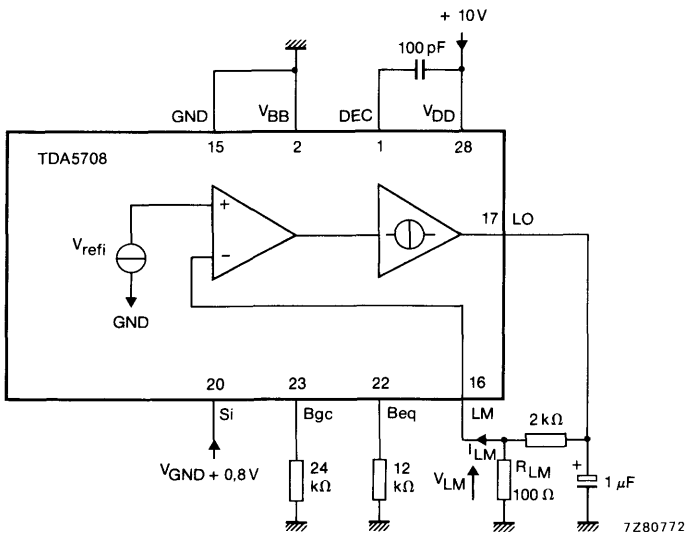


Fig. 11 Test circuit for V_{LM} ($V_{refi} \approx V_{LM}$) and I_{LM}.

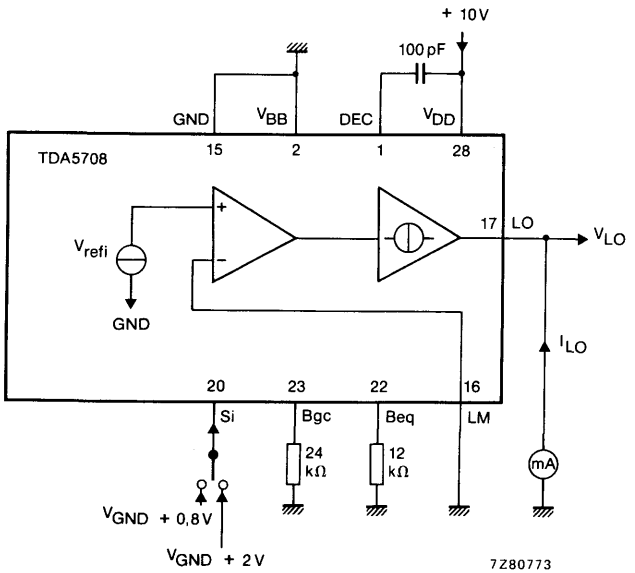


Fig. 12 Test circuit for V_{LO} and I_{LO}.

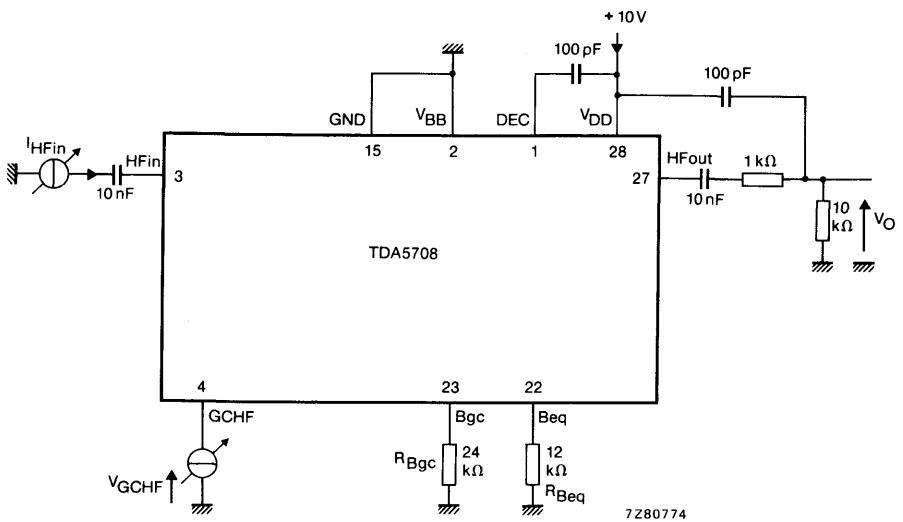


Fig. 13 Test circuit for HF part; a.c. characteristics.

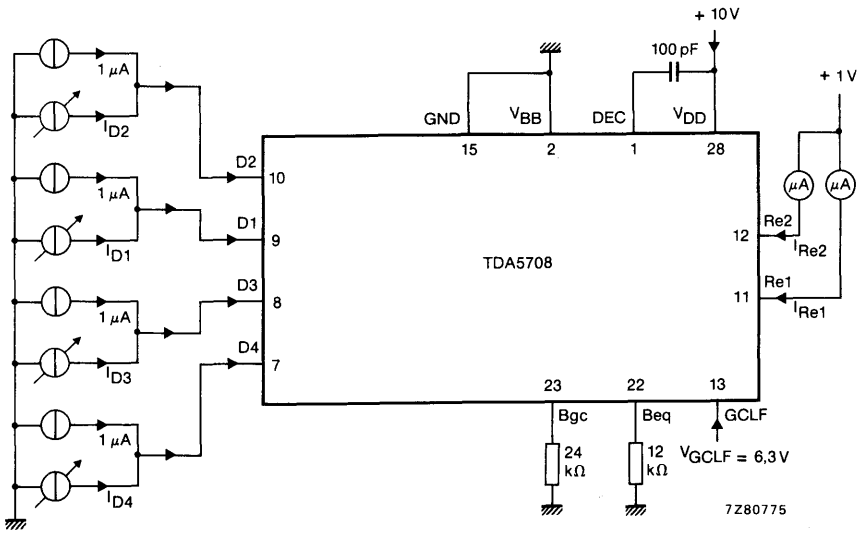


Fig. 14 Test circuit for LF part; a.c. gain.

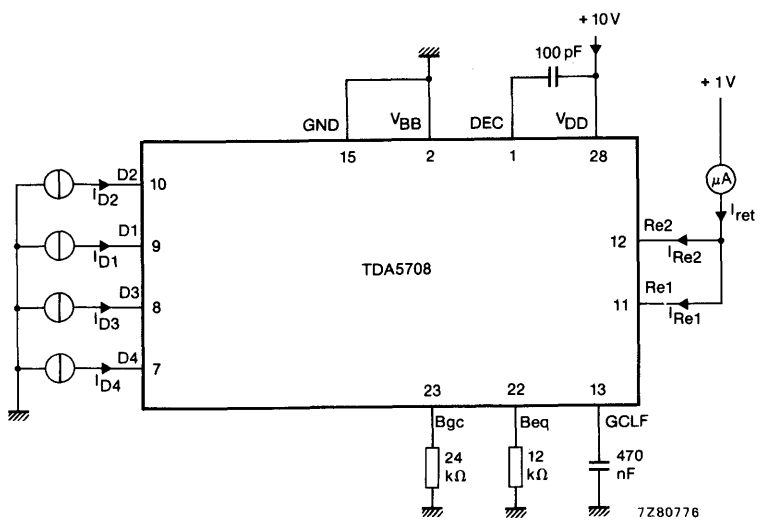


Fig. 15 Test circuit for total reference current I_{ret}.

RADIAL ERROR SIGNAL PROCESSOR FOR COMPACT DISC PLAYERS

GENERAL DESCRIPTION

The TDA5709 is a bipolar integrated circuit which provides control signals for the radial motor. These control signals are generated from radial error signals received from a photo-diode signal processor (TDA5708), and velocity control signals from the control processor.

Features

- Tracking error processor with automatic asymmetry control
- A.G.C. circuitry with automatic start-up and wobble generator
- Tracking control for fast forward/reverse scan, search, repeat and pause functions
- TTL compatible digital input/output
- Digitalized tracking error signal
- Possibility for car application

QUICK REFERENCE DATA

Supply voltage range	$V_{DD}-V_{BB}$	8 to 13	V
Quiescent supply current	I_Q	typ. 6	mA
Operating ambient temperature range	T_{amb}	−30 to + 85	°C

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

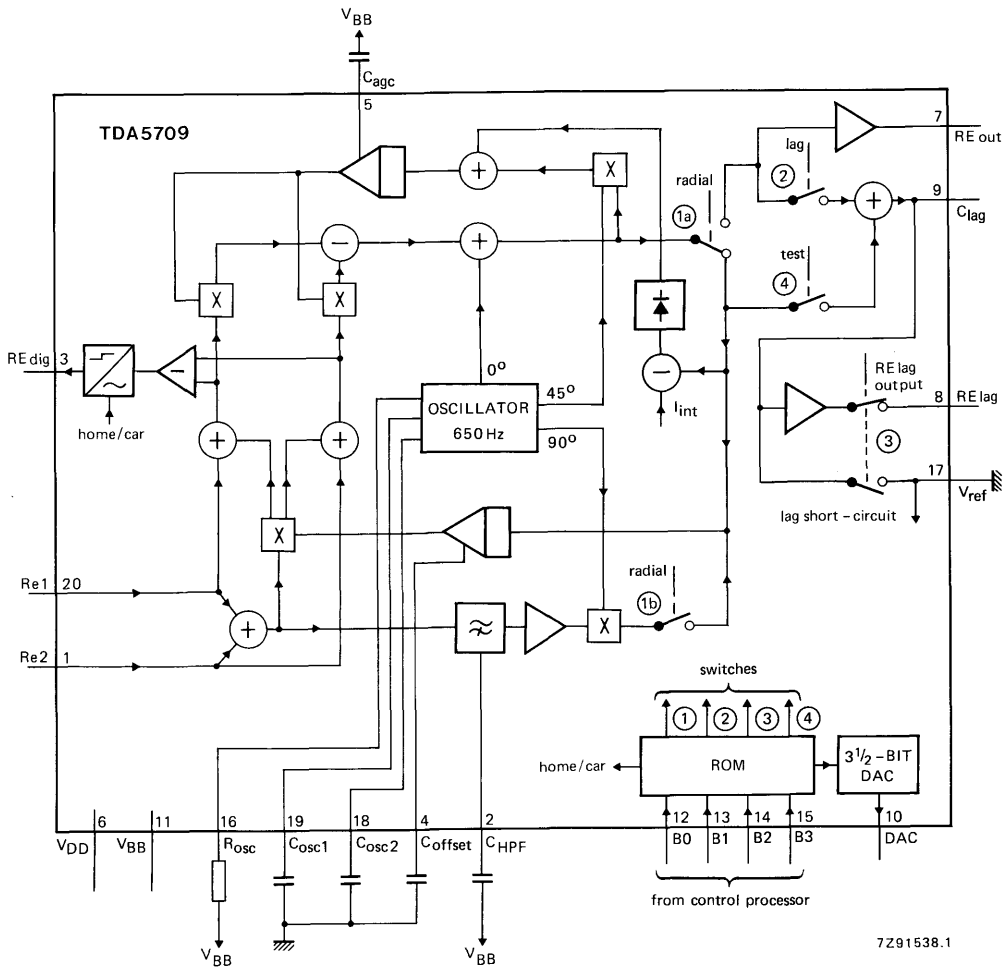


Fig. 1 Block diagram.

DEVELOPMENT DATA

PIN DESCRIPTION

Pin No.	Symbol	Description
1	Re2	Input for amplified currents from photo diodes D1 and D2
2	C_{HPF}	High-pass filter for Re1 and Re2, used for radial offset control
3	REdig	Digital output of sign (Re2 − Re1)
4	C_{offset}	Offset control input for radial offset
5	C_{agc}	Gain control input for radial error signal
6	V_{DD}	Positive supply voltage
7	REout	Current output of amplified (Re2 − Re1) input currents
8	RElag	Voltage output of integrated (Re2 − Re1) input currents
9	C_{lag}	Integrator capacitor for (Re1 − Re2) input currents
10	DAC	Current output for track jumping (3½ bits)
11	V_{BB}	Negative supply connection (also substrate connection)
12	B0	Input control bits for off-, catch-, play-status and DAC output current
13	B1	
14	B2	
15	B3	
16	R_{osc}	Biassing resistor for oscillator frequency and internal amplitude
17	V_{ref}	Intermediate supply voltage
18	C_{osc2}	Frequency setting capacitors for oscillator
19	C_{osc1}	
20	Re1	Input for amplified currents from photo-diodes D3 and D4

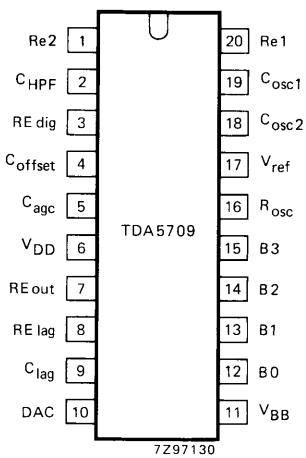


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range ($V_{DD} - V_{BB}$) pin 6 – pin 11	$V_{DD}-V_{BB}$	−0,3 to + 13	V
Total power dissipation	P_{tot}	see Fig. 3	
Storage temperature range	T_{stg}	−55 to + 150	°C
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Operating junction temperature	T_j	max. 150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	= 72	K/W

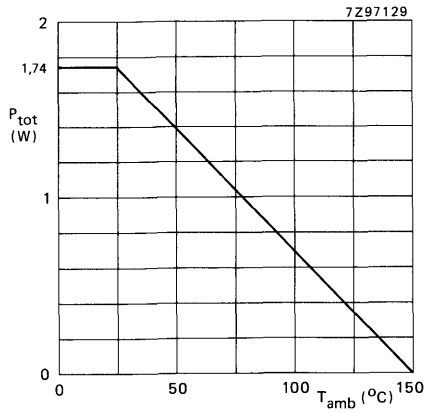


Fig. 3 Power derating curve.

CHARACTERISTICS

V_{DD} = + 5 V; V_{BB} = −5 V; T_{amb} = 25 °C; V_{ref} = 0 V; R_{osc} = 24 kΩ; all voltages with respect to V_{ref}; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage					
pin 6 − pin 11 ($V_{DD} - V_{BB}$)		8	−	13	V
pin 17 − pin 11 ($V_{ref} - V_{BB}$)		4,5	5,0	5,5	V
Quiescent supply current	I_Q	−	6	−	mA
REdig output (pin 3)					
Output voltage level					
HIGH (note 1; C)	V_{REdig}	V_{ref} + 2,4	−	−	V
LOW (note 1; A)	V_{REdig}	V_{ref} −0,3	−	V_{ref} + 0,4	V
LOW (note 1; B)	V_{REdig}	V_{BB}	−	V_{BB} + 0,4	V
Output current					
sink current (note 1; A or B)	I_{REdig}	400	−	−	μA
source current (note 1; C)	I_{REdig}	−	−150	−50	μA
Digital inputs (pins 12 to 15)					
B0, B1, B2 and B3					
Input voltage HIGH (note 2)	V_B	V_{ref} + 2	−	V_{DD}	V
Input voltage LOW (note 2)	V_B	V_{BB} + 2	−	V_{ref} + 0,8	V
Input voltage HIGH (note 3)	V_B	V_{BB} + 2	−	V_{DD}	V
Input voltage LOW (note 3)	V_B	V_{BB} −0,3	−	V_{BB} + 0,8	V
Input current					
at V_B = HIGH	I_B	−	0	−	μA
at V_B = LOW	I_B	−	−	−10	μA
DAC output (pin 10)					
Output voltage range					
at I_{DAC} = + 150 μA (sink current)	V_{DAC}	V_{BB} + 1,5	−	V_{DD}	V
at I_{DAC} = −150 μA (source current)	V_{DAC}	V_{BB}	−	V_{DD} −1	V
Output impedance					
at I_{DAC} = 200 μA	$\lvert Z_{DAC} \rvert$	−	50	−	MΩ

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
DAC output (continued)					
Ratio of output current pin 10 to pin 16 (see Table 1)	I_{10}/I_{16}	3,6	4	4,4	
		−4,6	−4	−3,4	
		0,9	1	1,1	
		−1,2	−1	−0,8	
		0,68	0,75	0,82	
		−0,86	−0,75	−0,64	
		0,45	0,5	0,55	
		−0,58	−0,5	−0,42	
		0,23	0,25	0,27	
		−0,29	−0,25	−0,2	
Analogue input (pin 16)					
Input voltage level	V_{Rosc}	–	V_{BB} + 1,2	–	V
Input current level	I_{Rosc}	–	−50	–	μA
Radial error inputs (Re1 pin 20, Re2 pin 1)					
Input voltage level at I_{Re1}, I_{Re2} = −105 μA	V_{Re1}, V_{Re2}	–	V_{BB} + 1,4	–	V
Input current	I_{Re1}, I_{Re2}	–	105	–	μA
Input impedance	$\lvert Z_{Re1}\rvert$, $\lvert Z_{Re2}\rvert$	–	1	–	kΩ
Gain control input (pin 5)					
Input voltage for minimum radial gain	V_{Cagc}	–	V_{BB} + 3,5	–	V
maximum radial gain	V_{Cagc}	–	V_{BB} + 5,5	–	V
Input impedance	$\lvert Z_{Cagc}\rvert$	–	20	–	MΩ
Offset control (pin 4)					
Output current at $I_{Re1} = I_{Re2} = -105$ μA; $V_{Cosc1} = V_{Cosc2} = V_{ref}$	$-I_{Coffset}$	–	0,25	–	μA
Input voltage for maximum amplification Re1	$V_{Coffset}$	–	V_{ref} −1	–	V
minimum amplification Re2	$V_{Coffset}$	–	V_{ref} −1	–	V
minimum amplification Re1	$V_{Coffset}$	–	V_{ref} + 1	–	V
maximum amplification Re2	$V_{Coffset}$	–	V_{ref} + 1	–	V
Input impedance	$\lvert Z_{Coffset}\rvert$	–	30	–	MΩ

parameter	symbol	min.	typ.	max.	unit
High-pass filter (pin 2)					
Voltage level at $I_{Re1} = I_{Re2} = 0$	V_{HPF}	–	$V_{BB} + 2,8$	–	V
Impedance	$\|Z_{HPF}\|$	–	5	–	kΩ
Oscillator					
(C_{osc1} pin 19, C_{osc2} pin 18)					
Linear input voltage range V_{Cosc1}, V_{Cosc2}	V_{Cosc}	$V_{ref} - 2$	–	$V_{ref} + 2$	V
RElag voltage output (pin 8)					
Output voltage range					
at $I_{RElag} = +200\ \mu A$ (sink current)	V_{RElag}	$V_{BB} + 1,5$	–	V_{DD}	V
at $I_{RElag} = -200\ \mu A$ (source current)	V_{RElag}	V_{BB}	–	$V_{DD} - 1$	V
Maximum source current output	I_{RElag}	–	−2,5	–	mA
Maximum sink current output	I_{RElag}	–	4	–	mA
Output impedance (f < 10 kHz)					
with RElag switched on	$\|Z_{RElag}\|$	–	–	50	Ω
with RElag switched off	$\|Z_{RElag}\|$	1	–	–	MΩ
REout push-pull current output (pin 7)					
Output voltage range					
at $I_{REout} = +40\ \mu A$ (sink current)	V_{REout}	$V_{BB} + 1,5$	–	V_{DD}	V
at $I_{REout} = -40\ \mu A$ (source current)	V_{REout}	V_{BB}	–	$V_{DD} - 1$	V
Output impedance	$\|Z_{REout}\|$	–	2	–	MΩ
C_{lag} push-pull current output/voltage input (pin 9)					
Output voltage range					
at $I_{Clag} = +4\ \mu A$ (sink current)	V_{Clag}	$V_{BB} + 1,5$	–	V_{DD}	V
at $I_{Clag} = -4\ \mu A$ (source current)	V_{Clag}	V_{BB}	–	$V_{DD} - 1,5$	V
Output impedance	$\|Z_{Clag}\|$	–	15	–	MΩ

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TRANSFER SPECIFICATIONS					
Oscillator (pins 19, 18)					
(V_{osc1}, V_{osc2}: −2 V to + 2 V)					
Transconductance factor					
$\frac{I_{Cosc2}}{V_{Cosc1}} \cdot R_{osc}$		–	0,48	–	
$\frac{I_{Cosc1}}{V_{Cosc2}} \cdot R_{osc}$		–	−0,48	–	
Amplitude stabilization					
$I_{osc1} = f(V_{osc1})$ at $V_{Cosc2} = 0$					
V_{osc1} = 0 V	I_{osc1}	–	0,1	–	μA
V_{osc1} = + 0,87 V	I_{osc1}	–	M_2 + 1,4	–	μA
V_{osc1} = −0,87 V	I_{osc1}	–	M_2 − 1,4	–	μA
V_{osc1} = + 1,2 V (note 4)	I_{osc1}	–	M_2	–	μA
V_{osc1} = − 1,2 V	I_{osc1}	–	M_2	–	μA
V_{osc1} = + 1,8 V	I_{osc1}	–	M_2 − 3,5	–	μA
V_{osc1} = − 1,8 V	I_{osc1}	–	M_2 + 3,5	–	μA
Amplitude stabilization					
$I_{osc2} = f(V_{osc2})$ at $V_{Cosc1} = 0$					
V_{osc2} = 0 V	I_{osc2}	–	0,1	–	μA
V_{osc2} = + 0,87 V	I_{osc2}	–	M_3 + 1,4	–	μA
V_{osc2} = −0,87 V	I_{osc2}	–	M_3 − 1,4	–	μA
V_{osc2} = + 1,2 V (note 5)	I_{osc2}	–	M_3	–	μA
V_{osc2} = − 1,2 V	I_{osc2}	–	M_3	–	μA
V_{osc2} = + 1,8 V	I_{osc2}	–	M_3 − 3,5	–	μA
V_{osc2} = − 1,8 V	I_{osc2}	–	M_3 + 3,5	–	μA
Transconductance factor					
$\frac{I_{Clag}}{V_{osc1}} \cdot R_{osc}$					
with test on; radial off;					
$I_{Re1} = I_{Re2} = 0$		–	−0,08	–	

parameter	symbol	min.	typ.	max.	unit
Transconductance factor $\frac{I_{Clag}}{V_{osc1}} \cdot R_{osc}$					
with lag on; radial on; $I_{Re1} = I_{Re2} = 0$		–	−0,08	–	
Transconductance factor $\frac{I_{REout}}{V_{osc2}} \cdot R_{osc}$					
with radial on; $I_{Re1} = I_{Re2} = 0$		–	0	–	
$\frac{I_{REout}}{V_{osc1}} \cdot R_{osc}$					
with radial on; $I_{Re1} = I_{Re2} = 0$		–	0,8	–	
Transconductance factor $\frac{I_{Coffset}}{V_{Cosc2}} \cdot R_{osc}$					
with radial on; $I_{Re1} = I_{Re2} = 0$					
at $I_{HPF} = 30\ \mu A$		–	0,48	–	
at $I_{HPF} = 0\ \mu A$		–	0	–	
at $I_{HPF} = -30\ \mu A$		–	−0,48	–	
with radial off; $I_{Re1} = I_{Re2} = 0$					
at $I_{HPF} = 30\ \mu A$		–	0	–	
Transconductance factor $\frac{I_{Coffset}}{V_{Cosc1}} \cdot R_{osc}$					
with radial on; $I_{Re1} = I_{Re2} = 0$					
at $I_{HPF} = 30\ \mu A$		–	0	–	
with radial off; $I_{Re1} = I_{Re2} = 0$					
at $I_{HPF} = 30\ \mu A$		–	0,08	–	
Transconductance factor $\frac{I_{agc}}{V_{Cosc1}} \cdot R_{osc}$					
with radial on; $V_{agc} = 0,5$ V; $V_{Coffset} = V_{Cosc2} = 0$ V					
at $I_{Re1} = -150\ \mu A$; $I_{Re2} = 0$		–	−0,48	–	
at $I_{Re1} = I_{Re2} = -100\ \mu A$		–	note 6	–	
at $I_{Re1} = 0$; $I_{Re2} = -150\ \mu A$		–	+ 0,48	–	

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Transconductance factor					
$\frac{I_{agc}}{V_{Cosc2}} \cdot R_{osc}$					
with radial on; V_{agc} = 0,5 V;					
$V_{offset} = V_{Cosc1}$ = 0 V					
at $I_{Re1} = -150\ \mu A$; $I_{Re2} = 0$		–	−0,48	–	
at $I_{Re1} = I_{Re2} = -100\ \mu A$		–	0	–	
at $I_{Re1} = 0$; $I_{Re2} = -150\ \mu A$		–	+0,48	–	
Transfer $C_{lag} \rightarrow$ RElag					
$\frac{V_{RElag}}{V_{Clag}}$; at frequencies < 10 kHz					
with lag short-circuit off;					
RElag output on		–	1	–	
Slew rate					
RElag amplifier					
with lag short-circuit off;					
RElag output on	SR	–	0,4	–	V/μs
Switch lag short-circuit					
Impedance $\frac{\Delta V_{Clag}}{\Delta I_{Clag}}$					
with lag short-circuit on;					
$\lvert I_{Clag} \rvert < 10\ \mu A$	$\lvert Z_{lag\ sc} \rvert$	–	–	1	kΩ
Offset $\lvert V_{Clag} - V_{ref} \rvert$					
with lag short-circuit on;					
$I_{Clag} = 0\ \mu A$	$\lvert V_{RElag} \rvert$	–	–	10	mV
Transfer resistance (Re1, Re2 to C_{HPF})					
$\frac{\Delta V_{CHPF}}{\Delta(I_{Re1} + I_{Re2})}$		–	2,5	–	kΩ
Gain (Re1, Re2 to REout)					
$\frac{\Delta I_{REout}}{\Delta(I_{Re1} - I_{Re2})}$					
with lag short-circuit on; radial on;					
$V_{Coffset} = V_{osc1} = V_{osc2}$ = 0 V					
V_{agc} = 0,5 V		–	5	–	times

parameter	symbol	min.	typ.	max.	unit
Offset current RE					
Offset current with lag short-circuit on; radial on; $V_{Coffset} = V_{osc1} = V_{osc2} = 0$ V $V_{agc} = 0{,}5$ V at $I_{Re1} = I_{Re2} = 100\ \mu A$	I_{RE}	–	0	–	μA
Gain (Re1, Re2 to C_{agc})					
$\frac{\Delta I_{Cagc}}{\Delta(I_{Re1} - I_{Re2})}$ at $I_{Re1} = -104\ \mu A$ with lag short-circuit on; radial on; $V_{Coffset}$ = (see note 7); $V_{agc} = 0{,}5$ V; $V_{Cosc1} = 0$ V; $V_{Cosc2} = 1{,}2$ V; $\Delta(I_{Re1} - I_{Re2}) = 8\ \mu A$		–	0,8	–	times
$\frac{\Delta I_{Cagc}}{\Delta(I_{Re1} - I_{Re2})}$ at $I_{Re2} = -104\ \mu A$ with lag short-circuit on; radial on; $V_{Coffset}$ = (note 7); $V_{agc} = 0{,}5$ V; $V_{Cosc1} = 0$ V; $V_{Cosc2} = 1{,}2$ V; $\Delta(I_{Re2} - I_{Re1}) = 8\ \mu A$		–	−0,8	–	times
Offset current I_{Cagc}					
Offset current with lag short-circuit on; radial on; $V_{Cosc1} = 0$ V; $V_{Cosc2} = 0$ V $V_{agc} = 0{,}5$ V at $I_{Re1} = I_{Re2} = -100\ \mu A$	I_{Cagc}	–	0	–	μA
Transconductance factor					

$\frac{\Delta I_{RE} \cdot V_{RANGE}}{I_{tot} \cdot V_{Coffset}}$
with $V_{Cosc1} = V_{Cosc2} = 0$ V;
radial on; $V_{agc} = -3$ V;
$V_{RANGE} = 1$ V (internal);
$I_{tot} = I_{Re1} + I_{Re2}$
at $I_{Re1} = I_{Re2} = -100\ \mu A$
		–	2,5	–	

$\frac{\Delta I_{RE} \cdot V_{RANGE}}{I_{tot} \cdot V_{Coffset}}$ with $V_{Cosc1} = V_{Cosc2} = 0$ V; radial on; $V_{agc} = V_{BB}$; $V_{RANGE} = 1$ V (internal); $I_{tot} = I_{Re1} + I_{Re2}$ at $I_{Re1} = I_{Re2} = -100\ \mu A$		–	0	–	

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Gain control current I_{agc}					
I_{agc} with $V_{Cosc1} = V_{Cosc2} = 0$ V; $V_{agc} = 0{,}5$ V; radial off; $V_{Coffset} = 0$ V					
at $I_{REtot} = 200\ \mu A$; $I_{Re1} - I_{Re2} = 35\ \mu A$	I_{agc}	–	0	–	μA
at $I_{REtot} = 200\ \mu A$; $I_{Re1} - I_{Re2} = 65\ \mu A$	I_{agc}	–	50	–	μA

Notes to the characteristics

1. REdig output conditions:
   A: $I_{Re1} > I_{Re2} + 5\ \mu A$; $V_{Coffset} = V_{ref}$; B0 and B1 and B2 and B3 $> V_{BB} + 2{,}0$ V.
   B: $I_{Re1} > I_{Re2} + 5\ \mu A$; $V_{Coffset} = V_{ref}$; B0 or B1 or B2 or B3 $< V_{BB} + 0{,}8$ V.
   C: $I_{Re2} > I_{Re1} + 5\ \mu A$; $V_{Coffset} = V_{ref}$; don't cares for B0, B1, B2 and B3.
2. In the 'home' application all logical inputs B0, B1, B2 and B3 must be $> V_{BB} + 2$ V.

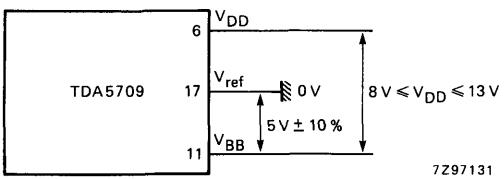


Fig. 4 TDA5709 'home' application.

3. In the 'car' application one or more of the logical inputs B0, B1, B2, B3 must be $< V_{BB} + 0{,}8$ V.

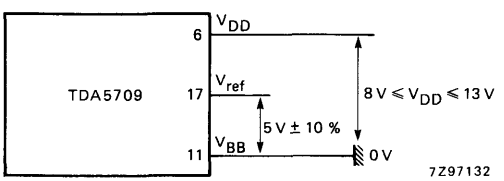


Fig. 5 TDA5709 'car' application.

4. M_2 is the measured value of I_{osc1} at $V_{osc1} = 0$ V.
5. M_3 is the measured value of I_{osc2} at $V_{osc2} = 0$ V.
6. Parabolic curve.
7. $V_{Coffset}$ must be adjusted so that $I_{Clag} = 4\ \mu A$.

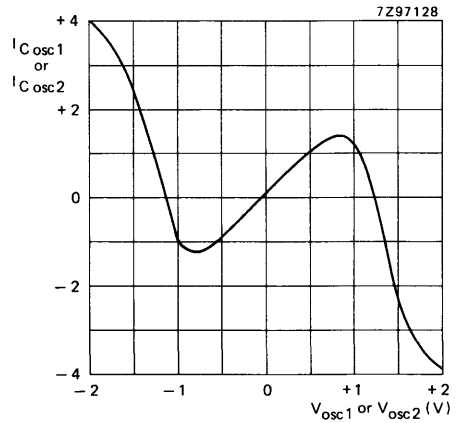


Fig. 6 Amplitude stabilization (typical curve).

Table 1 Truth table for DAC output current

DEVELOPMENT DATA

type names	DAC output (μA)*	logical inputs				internal switches				
		B0	B1	B2	B3	lag	lag s/c	rad	test	output REIag
OFF	0	0	0	0	0	off	on	off	off	off
CATCH	0	0	0	0	1	off	on	on	off	off
PUSH	−200	0	0	1	0	off	on	off	off	off
(kick)	−200	0	0	1	1	off	off	off	off	on
PULL	50	0	1	0	0	off	on	off	off	off
PULL	37,5	0	1	0	1	off	on	off	off	off
PULL	25	0	1	1	0	off	on	off	off	off
PULL	12,5	0	1	1	1	off	on	off	off	off
PUSH	−50	1	0	0	0	off	on	off	off	off
PUSH	−37,5	1	0	0	1	off	on	off	off	off
PUSH	−25	1	0	1	0	off	on	off	off	off
PUSH	−12,5	1	0	1	1	off	on	off	off	off
PULL	200	1	1	0	0	off	on	off	off	off
(kick)	200	1	1	0	1	off	off	off	off	on
play	0	1	1	1	0	on	off	on	off	on
test**	0	1	1	1	1	off	off	off	on	on

Where:
0 = input voltage LOW; 1 = input voltage HIGH.
* With R_{osc} = 24 kΩ.
** Non-proper operating of output REdig if the logical zero is close to V_{BB}.

FM RADIO CIRCUIT

GENERAL DESCRIPTION

The TDA7000 is a monolithic integrated circuit for mono FM portable radios, where a minimum on peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The i.f. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

The TDA7000 includes the following functions:

- R.F. input stage
- Mixer
- Local oscillator
- I.F. amplifier/limiter
- Phase demodulator
- Mute detector
- Mute switch

QUICK REFERENCE DATA

Supply voltage range (pin 5)	V_P	2,7 to 10	V
Supply current at V_P = 4,5 V	I_P	typ. 8	mA
R.F. input frequency range	f_{rf}	1,5 to 110	MHz
Sensitivity for −3 dB limiting (e.m.f. voltage) (source impedance: 75 Ω; mute disabled)	EMF	typ. 1,5	μV
Signal handling (e.m.f. voltage) (source impedance: 75 Ω)	EMF	typ. 200	mV
A.F. output voltage at R_L = 22 kΩ	V_o	typ. 75	mV

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

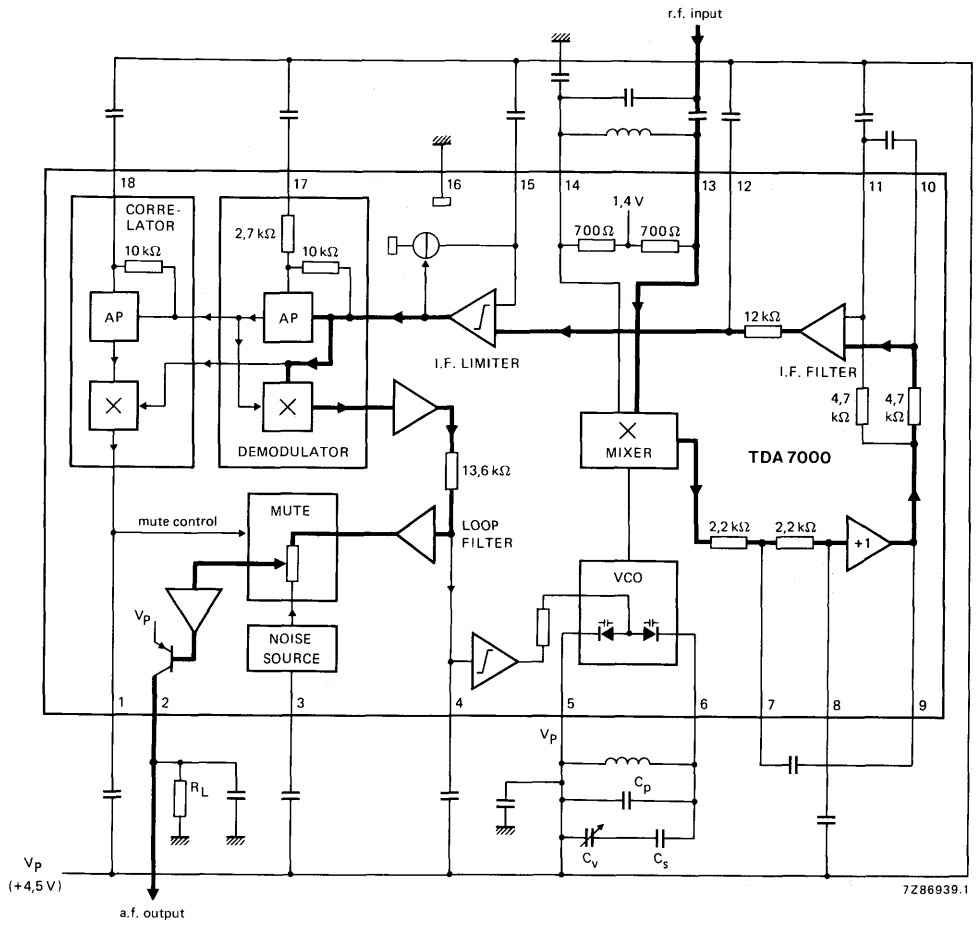


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 5)	V_P	max.	12 V
Oscillator voltage (pin 6)	V_{6-5}	V_P–0,5 to V_P +0,5	V
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}		–55 to + 150 °C
Operating ambient temperature range	T_{amb}		0 to + 60 °C

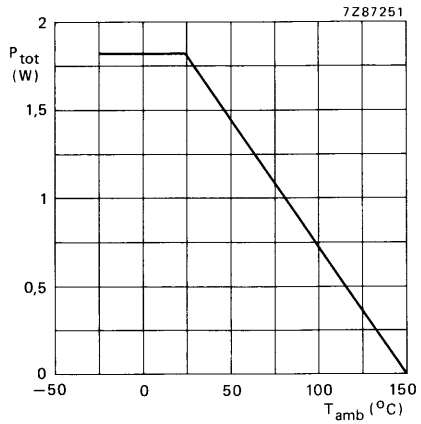


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 5)	V_P	2,7	4,5	10	V
Supply current at V_P = 4,5 V	I_P	–	8	–	mA
Oscillator current (pin 6)	I_6	–	280	–	μA
Voltage at pin 14	V_{14-16}	–	1,35	–	V
Output current at pin 2	I_2	–	60	–	μA
Voltage at pin 2; R_L = 22 kΩ	V_{2-16}	–	1,3	–	V

A.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4 (mute switch open, enabled); f_{rf} = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 0,2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity (see Fig. 3) (e.m.f. voltage)					
for −3 dB limiting; muting disabled	EMF	–	1,5	–	μV
for −3 dB muting	EMF	–	6	–	μV
for S/N = 26 dB	EMF	–	5,5	–	μV
Signal handling (e.m.f. voltage) for THD < 10%; Δf = ± 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio	S/N	–	60	–	dB
Total harmonic distortion					
at Δf = ± 22,5 kHz	THD	–	0,7	–	%
at Δf = ± 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage (ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1 kHz; Δf = ± 75 kHz AM signal: f_m = 1 kHz; m = 80%	AMS	–	50	–	dB
Ripple rejection (ΔV_P = 100 mV; f = 1 kHz)	RR	–	10	–	dB
Oscillator voltage (r.m.s. value) at pin 6	$V_{6\text{-}5(rms)}$	–	250	–	mV
Variation of oscillator frequency with supply voltage (ΔV_P = 1 V)	Δf_{osc}	–	60	–	kHz/V
Selectivity	S_{+300}	–	45	–	dB
	S_{-300}	–	35	–	dB
A.F.C. range	Δf_{rf}	–	± 300	–	kHz
Audio bandwidth at ΔV_o = 3 dB measured with pre-emphasis (t = 50 μs)	B	–	10	–	kHz
A.F. output voltage (r.m.s. value) at R_L = 22 kΩ	$V_{o(rms)}$	–	75	–	mV
Load resistance					
at V_P = 4,5 V	R_L	–	–	22	kΩ
at V_P = 9,0 V	R_L	–	–	47	kΩ

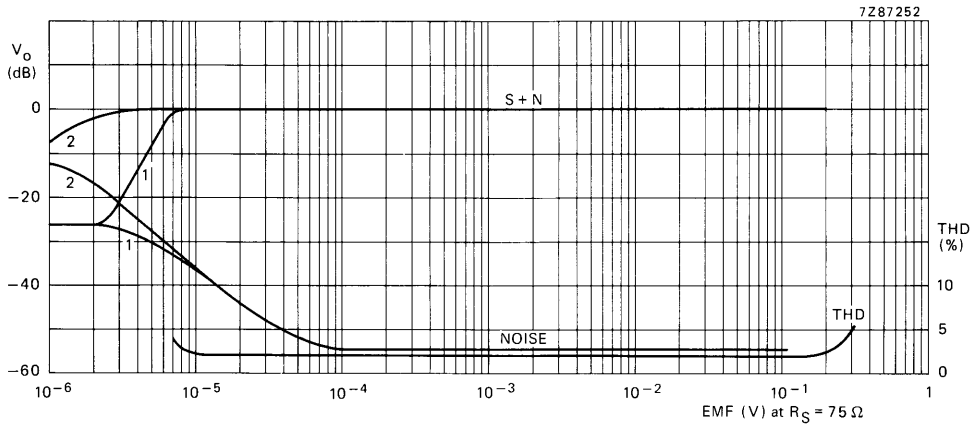


Fig. 3 A.F. output voltage (V_o) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance (R_S) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 75 mV; f_{rf} = 96 MHz.
for S + N curve: $\Delta f = \pm 22{,}5$ kHz; f_m = 1 kHz.
for THD curve: $\Delta f = \pm 75$ kHz; f_m = 1 kHz.

Notes

1. The muting system can be disabled by feeding a current of about 20 μA into pin 1.
2. The interstation noise level can be decreased by choosing a low-value capacitor at pin 3. Silent tuning can be achieved by omitting this capacitor.

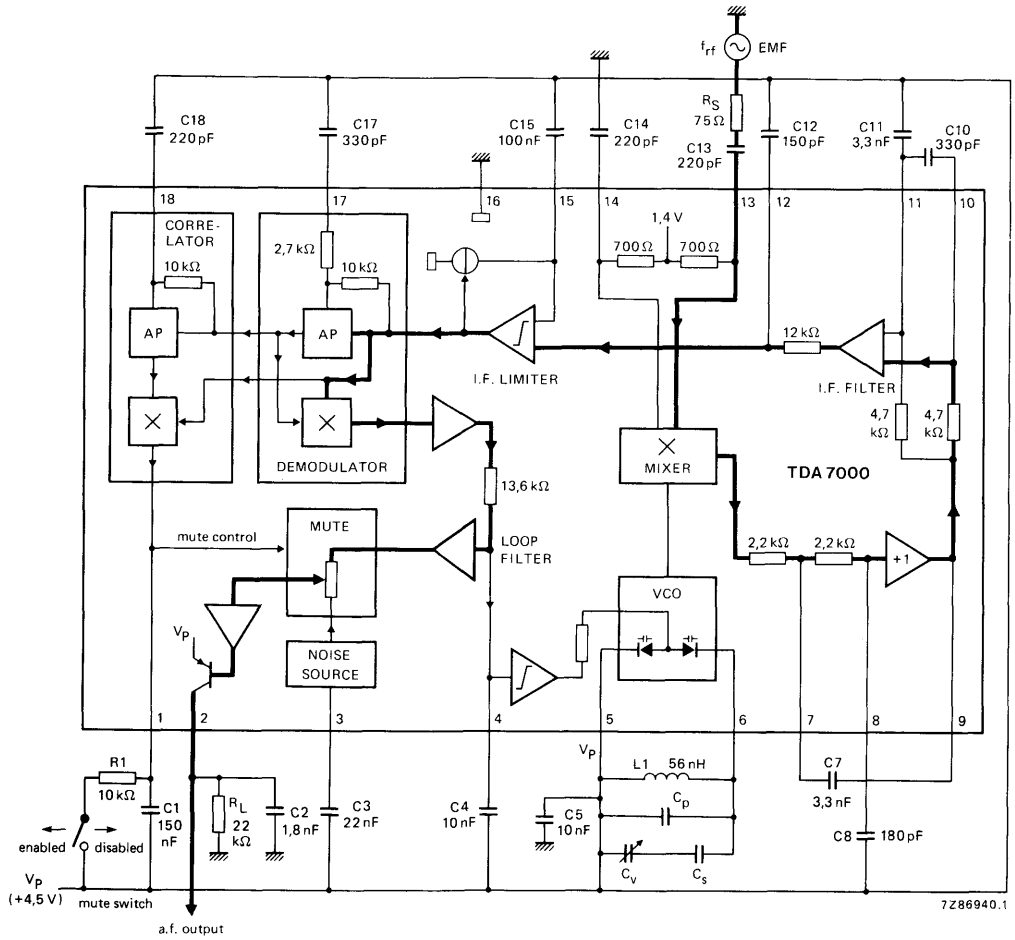


Fig. 4 Test circuit; for printed-circuit boards see Figs 5 and 6.

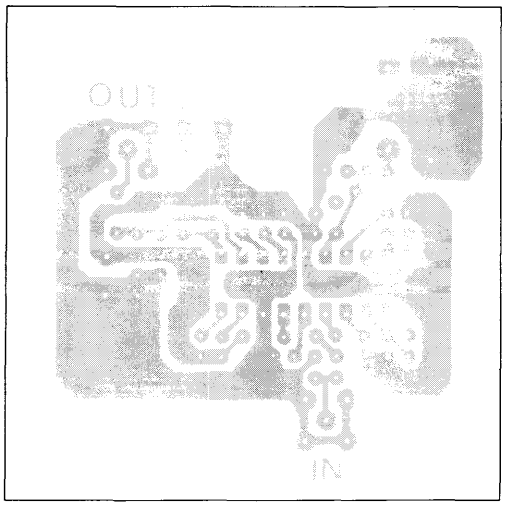


Fig. 5 Track side of printed-circuit board used for the circuit of Fig. 4.

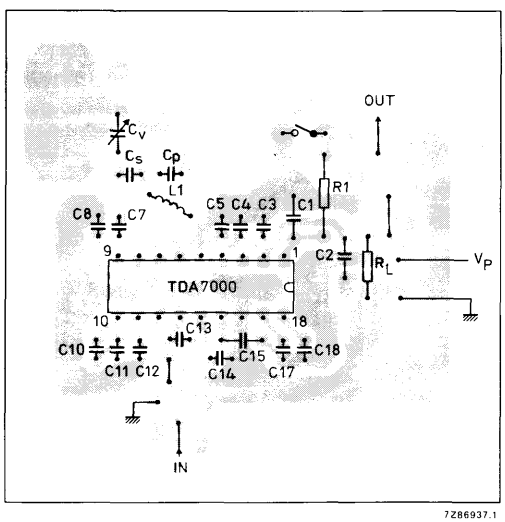


Fig. 6 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

FM RADIO CIRCUIT

GENERAL DESCRIPTION

The TDA7010T is a monolithic integrated circuit for mono FM portable radios, where a minimum on peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The i.f. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

The TDA7010T includes the following functions:

- R.F. input stage
- Mixer
- Local oscillator
- I.F. amplifier/limiter
- Phase demodulator
- Mute detector
- Mute switch

QUICK REFERENCE DATA

Supply voltage range (pin 4)	V_P	2,7 to 10	V
Supply current at V_P = 4,5 V	I_P	typ. 8	mA
R.F. input frequency range	f_{rf}	1,5 to 110	MHz
Sensitivity for −3 dB limiting (e.m.f. voltage) (source impedance: 75 Ω; mute disabled)	EMF	typ. 1,5	μV
Signal handling (e.m.f. voltage) (source impedance: 75 Ω)	EMF	typ. 200	mV
A.F. output voltage at R_L = 22 kΩ	V_o	typ. 75	mV

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).

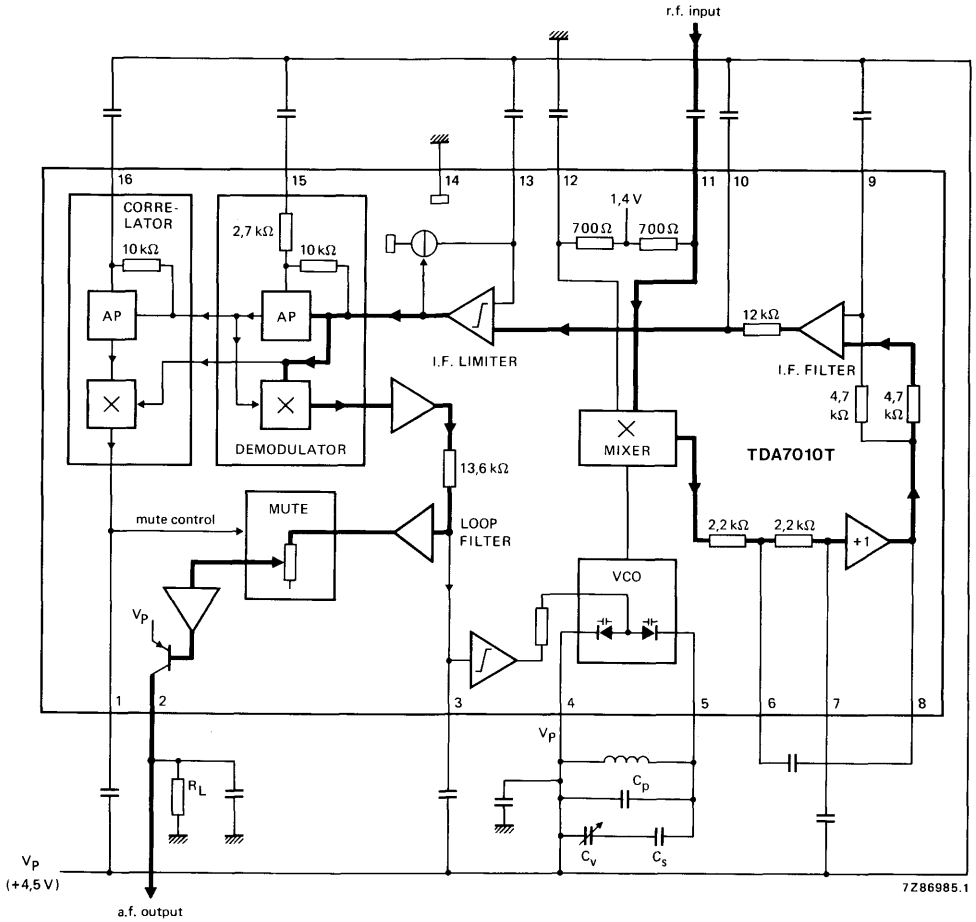


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 4)	V_P	max.	12 V
Oscillator voltage (pin 5)	V_{6-5}	V_P–0,5 to V_P + 0,5	V
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}	–55 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 60	°C

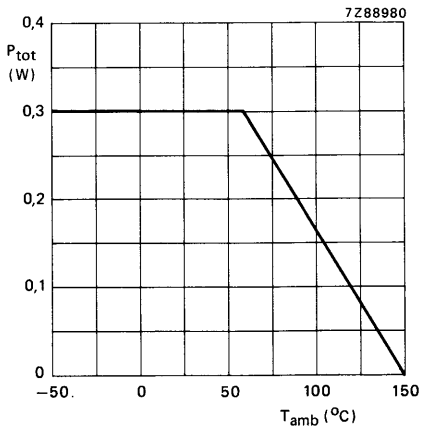


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_P	2,7	4,5	10	V
Supply current at V_P = 4,5 V	I_P	–	8	–	mA
Oscillator current (pin 5)	I_5	–	280	–	μA
Voltage at pin 12	V_{12-14}	–	1,35	–	V
Output current at pin 2	I_2	–	60	–	μA
Voltage at pin 2; R_L = 22 kΩ	V_{2-14}	–	1,3	–	V

A.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4 (mute switch open, enabled); f_{rf} = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 0,2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity (see Fig. 3) (e.m.f. voltage)					
for −3 dB limiting; muting disabled	EMF	–	1,5	–	μV
for −3 dB muting	EMF	–	6	–	μV
for S/N = 26 dB	EMF	–	5,5	–	μV
Signal handling (e.m.f. voltage) for THD < 10%; Δf = ± 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio	S/N	–	60	–	dB
Total harmonic distortion at Δf = ± 22,5 kHz	THD	–	0,7	–	%
at Δf = ± 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage (ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1 kHz; Δf = ± 75 kHz AM signal: f_m = 1 kHz; m = 80%	AMS	–	50	–	dB
Ripple rejection (ΔV_P = 100 mV; f = 1 kHz)	RR	–	10	–	dB
Oscillator voltage (r.m.s. value) at pin 5	$V_{5\text{-}4(rms)}$	–	250	–	mV
Variation of oscillator frequency with supply voltage (ΔV_P = 1 V)	Δf_{osc}	–	60	–	kHz/V
Selectivity	S_{+300}	–	43	–	dB
	S_{-300}	–	28	–	dB
A.F.C. range	Δf_{rf}	–	± 300	–	kHz
Audio bandwidth at ΔV_o = 3 dB measured with pre-emphasis (t = 50 μs)	B	–	10	–	kHz
A.F. output voltage (r.m.s. value) at R_L = 22 kΩ	$V_{o(rms)}$	–	75	–	mV
Load resistance at V_P = 4,5 V	R_L	–	–	22	kΩ
at V_P = 9,0 V	R_L	–	–	47	kΩ

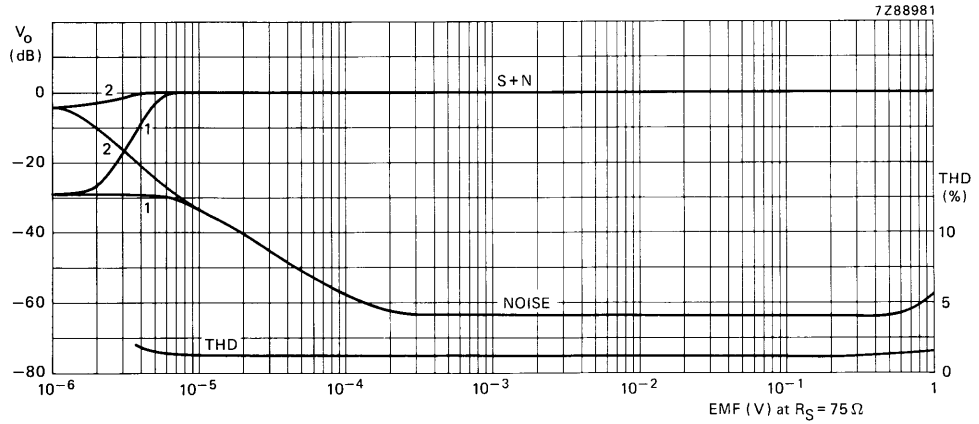


Fig. 3 A.F. output voltage (V_o) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance (R_S) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 75 mV; f_{rf} = 96 MHz.
for S + N curve: $\Delta f = \pm$ 22,5 kHz; f_m = 1 kHz.
for THD curve: $\Delta f = \pm$ 75 kHz; f_m = 1 kHz.

Notes

1. The muting system can be disabled by feeding a current of about 20 μA into pin 1.

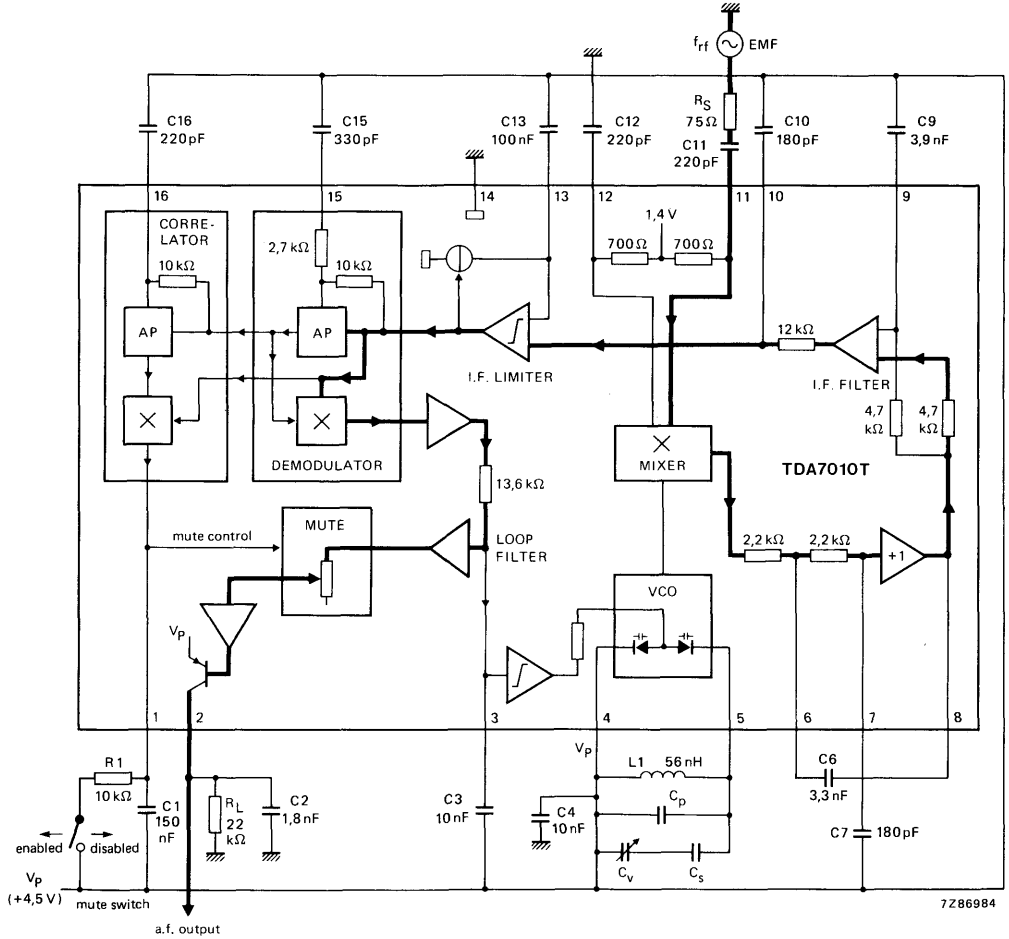


Fig. 4 Test circuit; for printed-circuit boards see Figs 5 and 6.

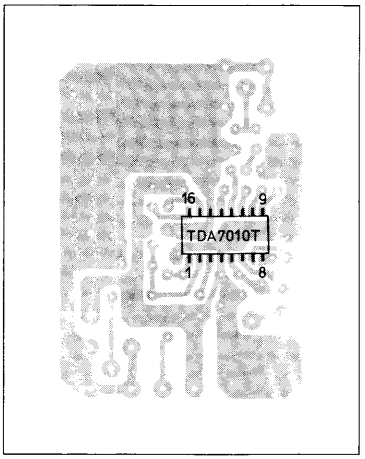


Fig. 5 Track side of printed-circuit board used for the circuit of Fig. 4.

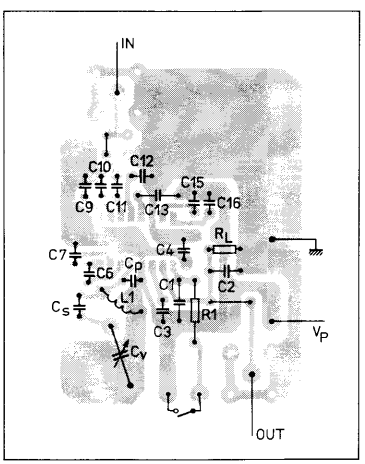


Fig. 6 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

FM RADIO CIRCUIT FOR MTS

GENERAL DESCRIPTION

The TDA7021T integrated radio receiver circuit is for portable radios, stereo as well as mono, where a minimum of periphery is important in terms of small dimensions and low cost. It is fully compatible for applications using the low-voltage micro tuning system (MTS). The IC has a frequency locked loop (FLL) system with an intermediate frequency of 76 kHz. The selectivity is obtained by active RC filters. The only function to be tuned is the resonant frequency of the oscillator. Interstation noise as well as noise from receiving weak signals is reduced by a correlation mute system.

Special precautions have been taken to meet local oscillator radiation requirements. Because of the low intermediate frequency, low pass filtering of the MUX signal is required to avoid noise when receiving stereo. 50 kHz roll-off compensation, needed because of the low pass characteristic of the FLL, is performed by the integrated LF amplifier. For mono application this amplifier can be used to directly drive an earphone. The field-strength detector enables field-strength dependent channel separation control.

Features

- RF input stage
- Mixer
- Local oscillator
- IF amplifier/limiter
- Frequency detector
- Mute circuit
- MTS compatible
- Loop amplifier
- Internal reference circuit
- LF amplifier for
  - mono earphone amplifier or
  - MUX filter
- Field-strength dependent channel separation control facility

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4-3}$	1,8	–	6,0	V
Supply current	V_P = 3 V	I_4	–	6,3	–	mA
RF input frequency		f_{rf}	1,5	–	110	MHz
Sensitivity (e.m.f.) for –3 dB limiting	source impedance = 75 Ω; mute disabled	EMF	–	4	–	μV
Signal handling (e.m.f.)	source impedance = 75 Ω	EMF	–	200	–	mV
AF output voltage		V_o	–	90	–	mV

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).

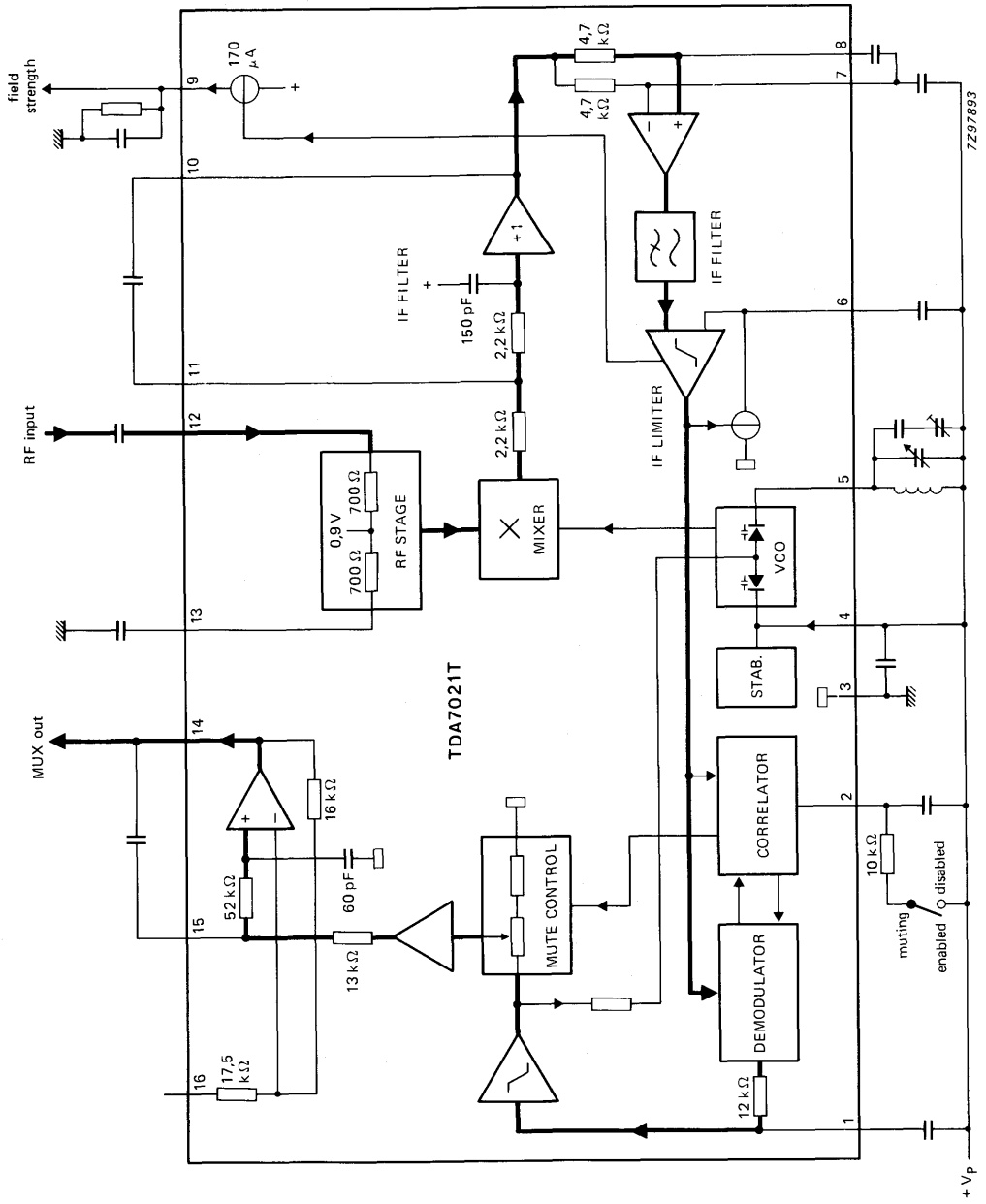


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4-3}$	–	7,0	V
Oscillator voltage		V_{5-4}	V_P–0,5	V_P + 0,5	V
Storage temperature range		T_{stg}	–55	+150	°C
Operating ambient temperature range		T_{amb}	–10	+70	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 300 K/W

DC CHARACTERISTICS

V_P = 3 V, T_{amb} = 25 °C, measured in circuit of Fig. 4, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4-3}$	1,8	3,0	6,0	V
Supply current	V_P = 3 V	I_4	–	6,3	–	mA
Oscillator current		I_5	–	250	–	μA
Voltage at pin 13		V_{13-3}	–	0,9	–	V
Output voltage (pin 14)		V_{14-3}	–	1,3	–	V

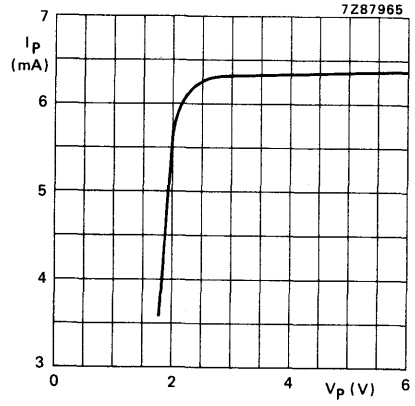


Fig. 2 Supply current as a function of the supply voltage.

DEVELOPMENT DATA

AC CHARACTERISTICS (MONO OPERATION)

V_P = 3 V; T_{amb} = 25 °C; measured in Fig. 5; f_{rf} = 96 MHz modulated with $\Delta f = \pm 22{,}5$ kHz; f_m = 1 kHz; EMF = 0,3 mV (e.m.f. at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity (e.m.f.)	see Fig. 3					
for −3 dB limiting	muting disabled	EMF	–	4,0	–	μV
for −3 dB muting		EMF	–	5,0	–	μV
for (S+N)/N = 26 dB		EMF	–	7,0	–	μV
Signal handling (e.m.f.)	THD < 10%; $\Delta f = \pm 75$ kHz	EMF	–	200	–	mV
Signal-to-noise ratio		(S+N)/N	–	60	–	dB
Total harmonic distortion	$\Delta f = \pm 22{,}5$ kHz	THD	–	0,7	–	%
	$\Delta f = \pm 75$ kHz	THD	–	2,3	–	%
AM suppression of output voltage	ratio of AM signal (f_m = 1 kHz; m = 80%) to FM signal (f_m = 1 kHz; Δf = 75 kHz)	AMS	–	50	–	dB
Ripple rejection	ΔV_P = 100 mV; f = 1 kHz	RR	–	30	–	dB
Oscillator voltage (r.m.s. value)		$V_{5\text{-}4(rms)}$	–	250	–	mV
Variation of oscillator frequency with supply voltage	ΔV_P = 1 V	$\frac{\Delta f_{osc}}{\Delta V_P}$	–	5	–	kHz/V
Variation of oscillator frequency with temperature		$\frac{\Delta f_{osc}}{\Delta T}$	–	0,2	–	kHz/K
Selectivity	see Fig. 9; no modulation					
		S_{+300}	–	46	–	dB
		S_{-300}	=	30	–	dB
AFC range		$\pm\Delta f_{rf}$	–	160	–	kHz
Mute range		$\pm\Delta f_{rf}$	–	120	–	kHz
Audio bandwidth	ΔV_o = 3 dB; measured with 50 μs pre-emphasis	B	–	10	–	kHz
AF output voltage (r.m.s. value)	R_L (pin 14) = 100 Ω	$V_{o(rms)}$	–	90	–	mV
AF output current						
max. d.c. load		$I_{o(dc)}$	−100	–	+100	μA
max. a.c. load (peak value)	THD = 10%	$I_{o(ac)}$	–	3	–	mA

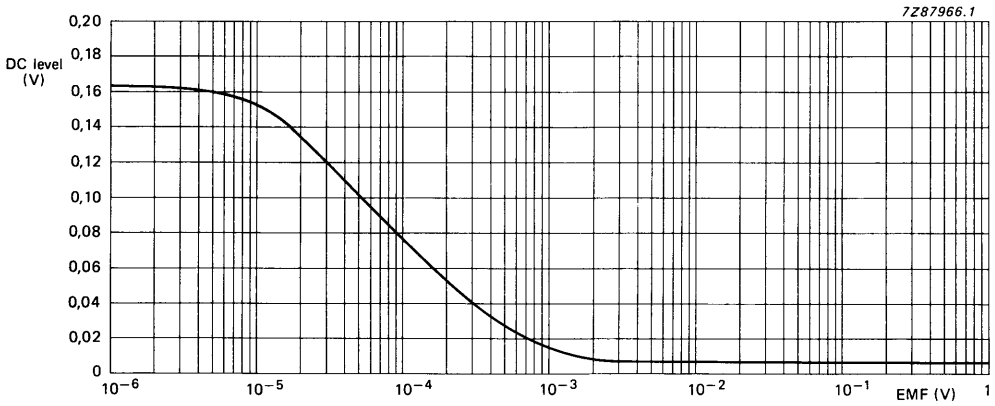


Fig. 3 Field strength voltage (V_{g-3}) at R_{source} = 1 kΩ; f = 96,75 MHz; Vp = 3 V.

DEVELOPMENT DATA

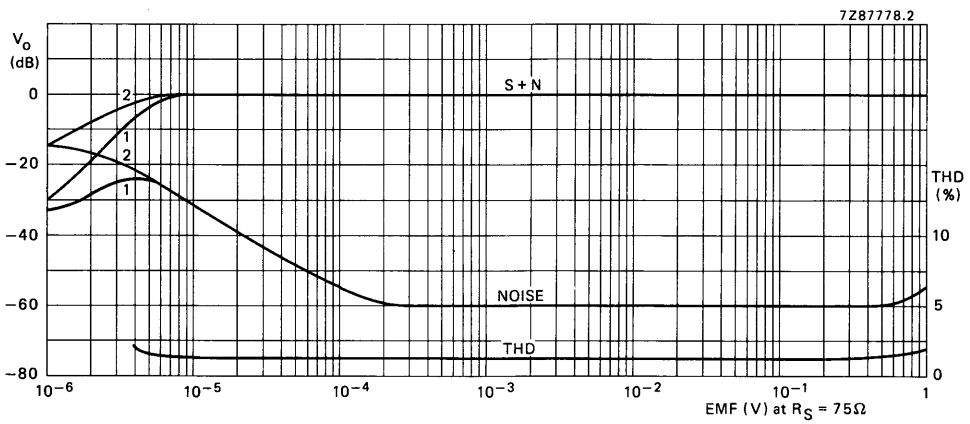
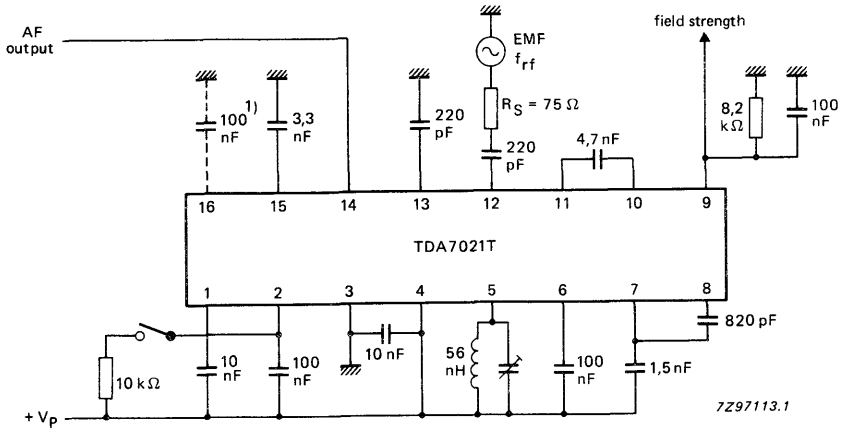


Fig. 4 Mono operation: AF output voltage (V_o) and total harmonic distortion (THD) as functions of input e.m.f. (EMF); R_{source} = 75 Ω; f_{rf} = 96 MHz; 0 dB = 90 mV. For S+N and noise curves (1) is with muting enabled and (2) is with muting disabled; signal Δf = ± 22,5 kHz and f_m = 1 kHz. For THD curve, Δf = ± 75 kHz and f_m = 1 kHz.



1) The AF output can be decreased by disconnecting the 100 nF capacitor from pin 16.

Fig. 5 Test circuit for mono operation.

AC CHARACTERISTICS (STEREO OPERATION)

V_P = 3 V; T_{amb} = 25 °C; measured in Fig. 8; f_{rf} = 96 MHz modulated with pilot Δf = ± 6,75 kHz and AF signal Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 1 mV (e.m.f. at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity (e.m.f.) for (S+N)/N = 26 dB	see Fig. 8; pilot off	EMF	–	11	–	μV
Selectivity	see Fig. 9; no modulation	S+300	–	40	–	dB
		S–300	–	22	–	dB
Signal-to-noise ratio		(S+N)/N	–	50	–	dB
Channel separation	V_i = L-signal; f_m = 1 kHz; pilot on:					
	at f_{rf} = 97 MHz	α	–	26	–	dB
	at f_{rf} = 87,5 MHz and 108 MHz	α	–	14	–	dB

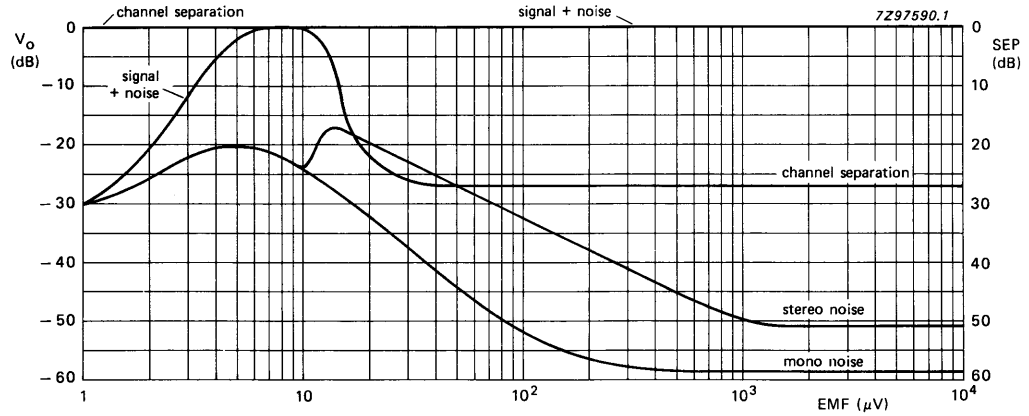


Fig. 6 Stereo operation: signal/noise and channel separation of TDA7021T when used in the circuit of Fig. 8.

DEVELOPMENT DATA

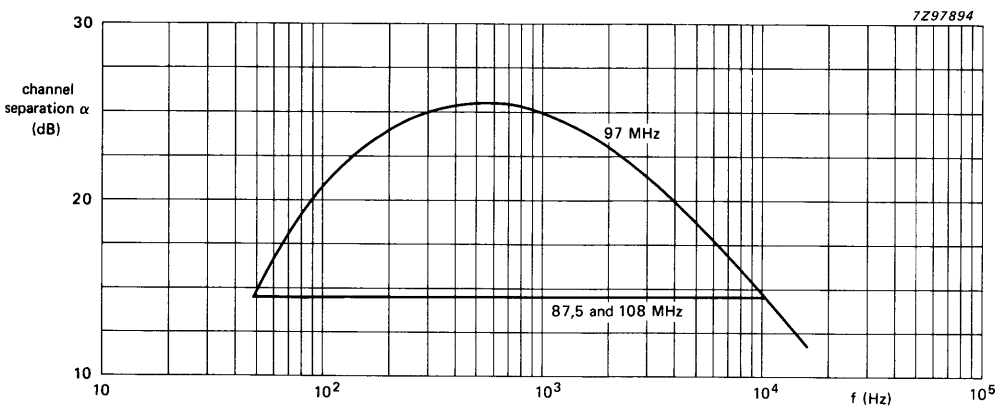


Fig. 7 Stereo operation: channel separation as a function of audio frequency in the circuit of Fig. 8.

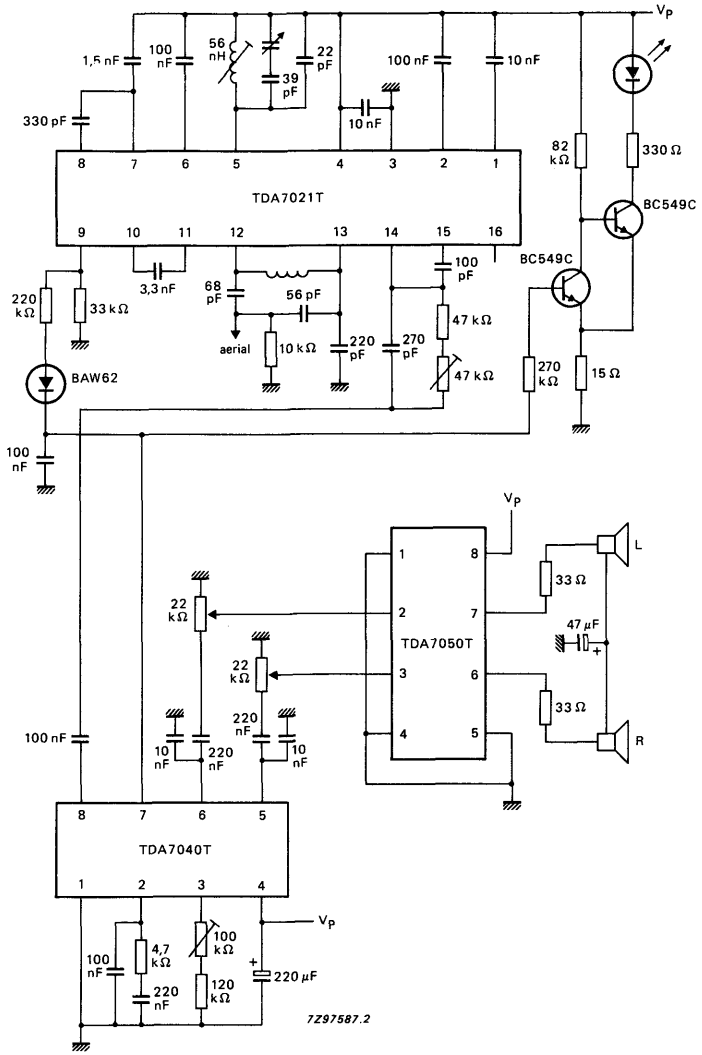


Fig. 8 Stereo application in combination with a low voltage PLL stereo decoder (TDA7040T) and a low voltage mono/stereo power amplifier (TDA7050T).

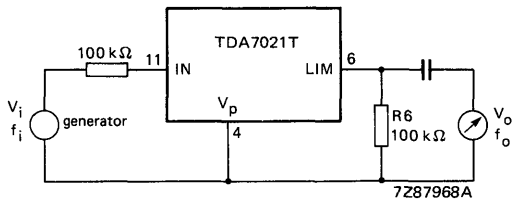


Fig. 9 Test set-up, V_i = 30 mV; f_i = 76 kHz; selective voltmeter at output has $R_i \geqslant 1$ MΩ and $C_i \leqslant 8$ pF; $f_o = f_i$.

Note to Fig. 9

This test set-up is to incorporate the circuit of Fig. 5 for mono operation or the circuit of Fig. 8 for stereo operation. For either circuit, replace the 100 nF capacitor at pin 6 with R6 (100 kΩ) as shown above.

Selectivity

$$S_{+300} = 20 \log \frac{V_o \mid (300\ \text{kHz} - f_i)}{V_o \mid f_i}$$

$$S_{-300} = 20 \log \frac{V_o \mid (300\ \text{kHz} + f_i)}{V_o \mid f_i}$$

DEVELOPMENT DATA

LOW VOLTAGE MICRO TUNING SYSTEM (MTS)

GENERAL DESCRIPTION

The TDA7030T low voltage tuning system incorporates all analogue and digital functions necessary for complete control of a TDA7021T FM radio receiver. The tuning system coverage is precisely defined by an integrated 100 kHz crystal oscillator.

The complete low voltage radio receiver system comprises:

TDA7021T	Single-chip FM radio receiver;
TDA7030T	Low voltage micro tuning system;
TDA7040T	Low voltage stereo decoder;
TDA7050T	Low voltage stereo power amplifier.

Features

- Memory function with four presets and last-input recall
- Search tuning
- Integrating AFC
- 16-step stereo volume control
- On/off power switch driver
- On-chip interface for 16-point frequency scale LCD

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

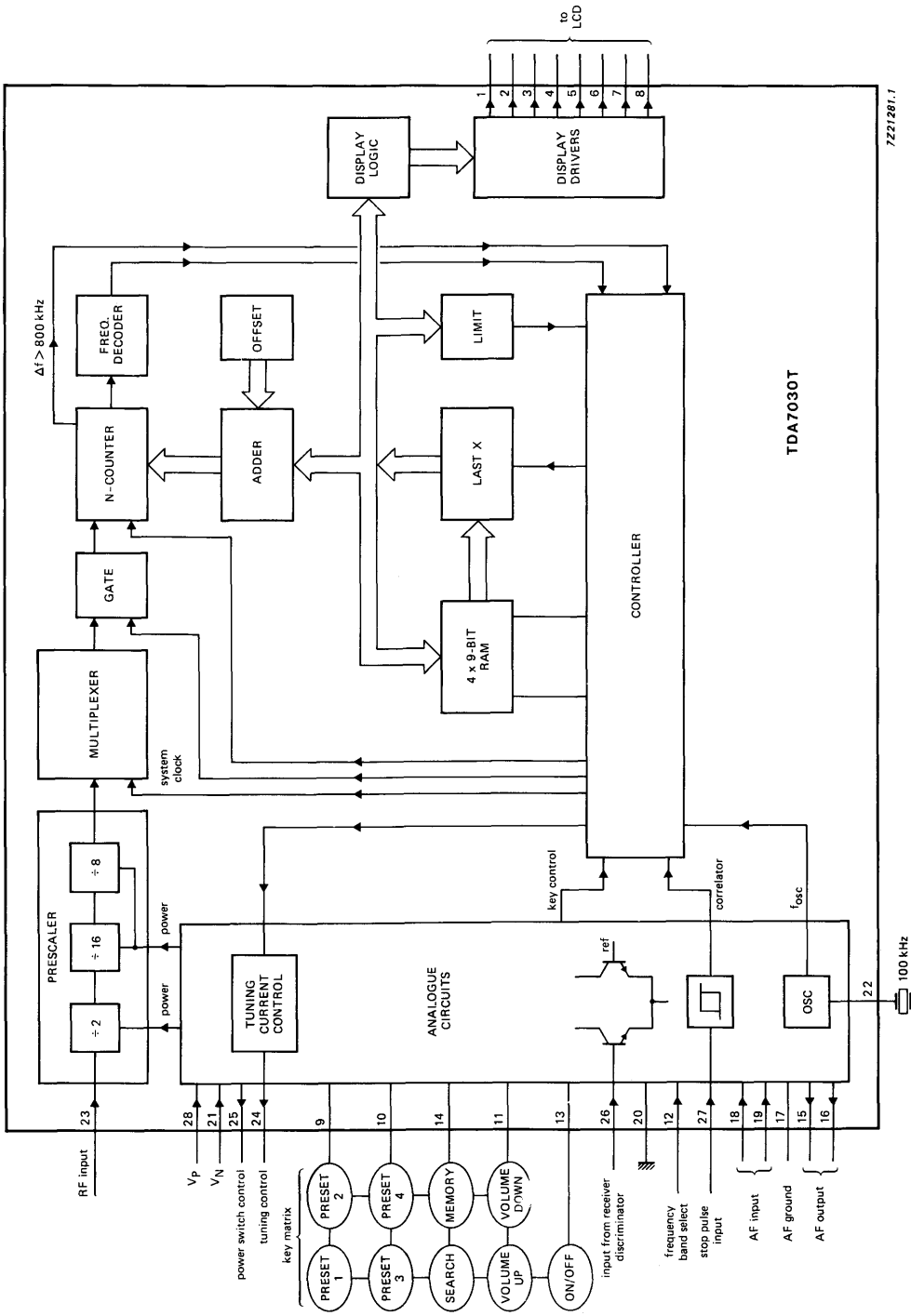


Fig. 1 Block diagram.

Notes to Fig. 1

Prescaler first stage (divide-by-2):

input frequency 75,925 to 89,925 MHz (Japan)
87,425 to 107,925 MHz (Europe and USA)
sensitivity 50 mV (typical)
input impedance (typical) 350 Ω/12 pF
first stage turns on when radio is switched on

Prescaler second stage (divide-by-16):

switches on only for dividing

Prescaler third stage (divide-by-8):

switches on only for dividing

Multiplexer:	switches the clock for the N-counter (proportional tuning)
Gate:	gate time 10,24 ms (one digit = 25 kHz)
N-counter:	13-bit down-counter for tuned frequency
Freq. decoder:	supplies N-counter information to the controller
Tuning current control:	1) integrating AFC (+ 1 to −1 μA max.) 2) search tuning (50 nA) 3) tuning current (5 μA) 4) down-set current (> 100 μA)
Adder and offset:	allows the system to store information in 9 bits
RAM:	4 x 9-bit
Last X:	last memory and search tuning counter
Limit:	band limit controller
Display drivers:	outputs to drive a 4 x 4 LCD matrix
Controller:	controls the system

DEVELOPMENT DATA

PINNING

pin	description
1	LCD matrix: segments 3, 4, 11, 12
2	LCD matrix: segments 2, 5, 10, 13
3	LCD matrix: segments 1, 6, 9, 14
4	LCD matrix: segments 0, 7, 8, 15
5	LCD matrix: backplane 4
6	LCD matrix: backplane 3
7	LCD matrix: backplane 2
8	LCD matrix: backplane 1
9	key matrix: preset 1/preset 2
10	key matrix: preset 3/preset 4
11	key matrix: volume up/down
12	frequency band select
13	key matrix: on/off control
14	key matrix: search memory

pin	description
15	volume control: AF output right
16	volume control: AF output left
17	volume control: AF ground
18	volume control: AF input right
19	volume control: AF input left
20	ground
21	negative supply voltage (V_N)
22	oscillator crystal connection
23	RF input from receiver oscillator
24	VCO tuning circuit
25	current source for power switch transistor
26	input from receiver discriminator
27	stop pulse input
28	positive supply voltage (V_P)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 28)	$V_P = V_{28-21}$	−0,5	+ 7,0	V
Supply current (pin 21)	I_{21}	−10	+ 10	mA
AF ground current (pin 17)	I_{17}	−10	+ 10	mA
Input voltage (pins 9, 10, 11, 12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 24, 25, 27)	V_I	–	7,0	V
Output current (pins 9, 10, 11, 12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 24, 25, 27)	I_O	–	−1,0	mA
Input voltage LCD matrix (pins 1, 2 3, 4, 5, 6, 7, 8)	V_I	−0,5	+ 5,0	V
Total power dissipation	P_{tot}	–	35	mW
Operating ambient temperature range	T_{amb}	−10	+ 70	°C
Storage temperature range	T_{stg}	−25	+ 150	°C

CHARACTERISTICS

$V_P = V_{28-21}$ = 1,8 to 5,0 V; T_{amb} = 25 °C; all voltages are referred to V_N (pin 21); typical values specified at V_P = 3 V; unless otherwise specified

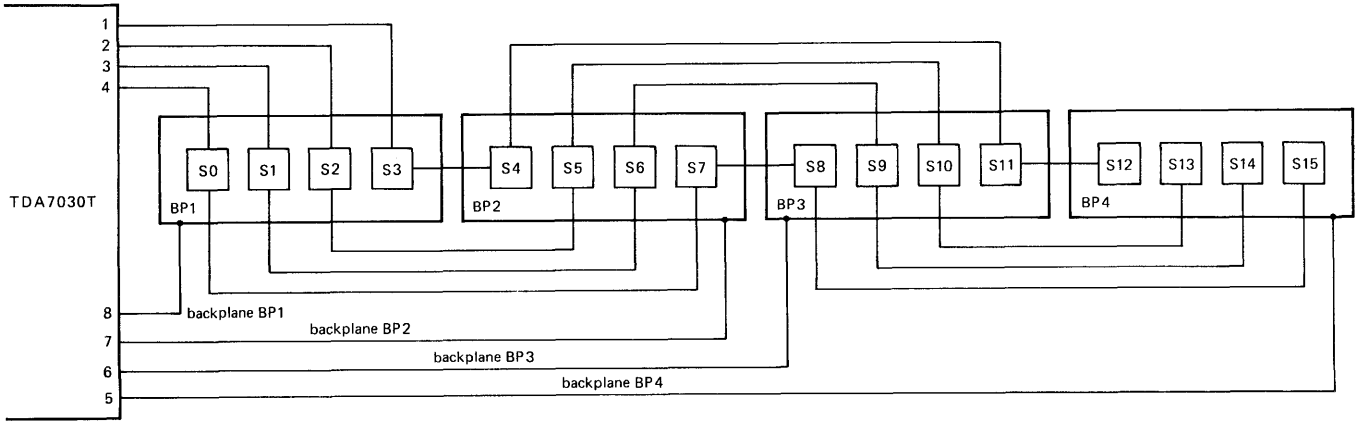
parameter	conditions	symbol	min.	typ.	max.	unit
Supply current	standby	I_P	–	20	–	μA
	radio on	I_P	–	2,0	–	mA
	tuning	I_P	–	5,5	–	mA
Frequency band select (pin 12)						
Band selection input voltage	frequency band with respect to TDA7021 IF:					
	76,0 to 90,0 MHz	V_{12}	V_P−0,5	–	V_P	V
	87,5 to 108,0 MHz	V_{12}	0	–	0,5	V
Oscillator (pin 22)						
Crystal frequency		f_{osc}	–	100	–	kHz
Series resonance resistance		R_L	–	–	15	kΩ
Shunt capacitance		C_O	–	*	–	pF
DC output current		I_{22}	–	−0,5	–	μA

* Value to be fixed.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Key matrix (pins 9, 10, 11, 13, 14)						
On, search, preset 1, preset 3, volume up		V_I	V_P–0,5	–	V_P	V
Memory, preset 2, preset 4, volume down		V_I	0	–	0,5	V
Input current		I_I	–	2	–	μA
Output current		I_O	–	–2	–	μA
Volume control AF inputs (pins 18, 19)						
AF input voltage (r.m.s. value)	total harmonic distortion < 1%	$V_{i(rms)}$	–	–	100	mV
AF input impedance		Z_i	–	10	–	kΩ
Volume control AF outputs (pins 15, 16)						
Attenuation in 16 steps of	R_L = 20 kΩ	A ΔA	0 3	– –	48 –	dB dB
Output impedance		Z_O	–	20	–	kΩ
Total harmonic distortion		THD	–	0,5	3,0	%
Signal-to-noise ratio	0 dB attenuation 20 dB attenuation	(S+N)/N (S+N)/N	– –	66 55	– –	dB dB
Power switch current source (pin 25)						
Current source capability		I_{25}	–500	–	–	μA
LCD matrix (pins 1, 2, 3, 4, 5, 6, 7, 8)			see Fig. 2			
VCO tuning current (pin 24)						
AFC off		I_{24}	–	0	–	μA
RF down set		I_{24}	–100	–	–	μA
RF tuning		I_{24}	–	5	–	μA
RF search		I_{24}	–	50	–	nA
AFC operating	depends on $V_{28\text{-}26}$	I_{24}	–1	–	+ 1	μA
RF input (pin 23)						
Input frequency		f	50	–	150	MHz
Sensitivity		α	70	–	500	mV
Receiver discriminator (pin 26)						
Output voltage	referred to V_P; I_{24} = 0 μA	V_{26}	–	300	–	mV
Stop pulse input (pin 27)						
On (field strength detected)		V_{27}	V_P–400	–	V_P	mV
Off (no field strength detected)		V_{27}	0	–	V_P–600	mV

APPLICATION INFORMATION



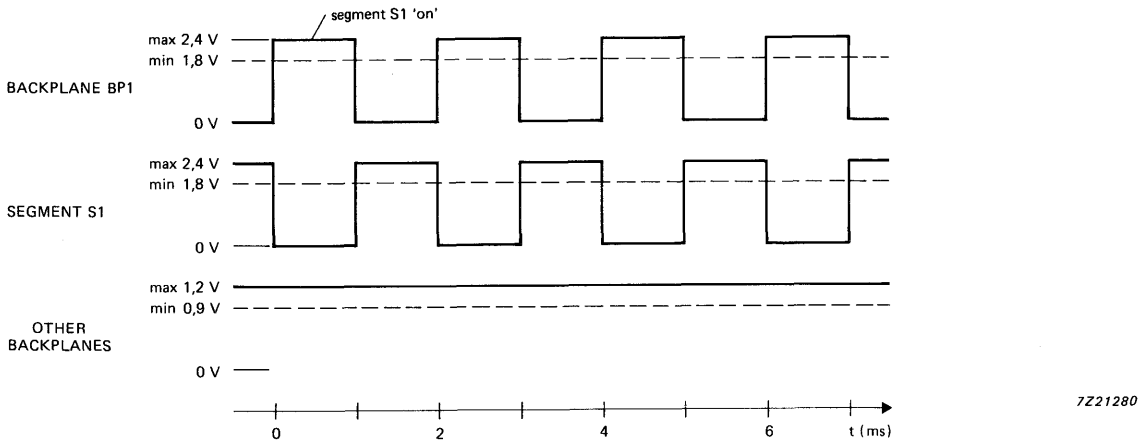


Fig. 2 LCD matrix with waveforms showing drive for segment S1.

DEVELOPMENT DATA

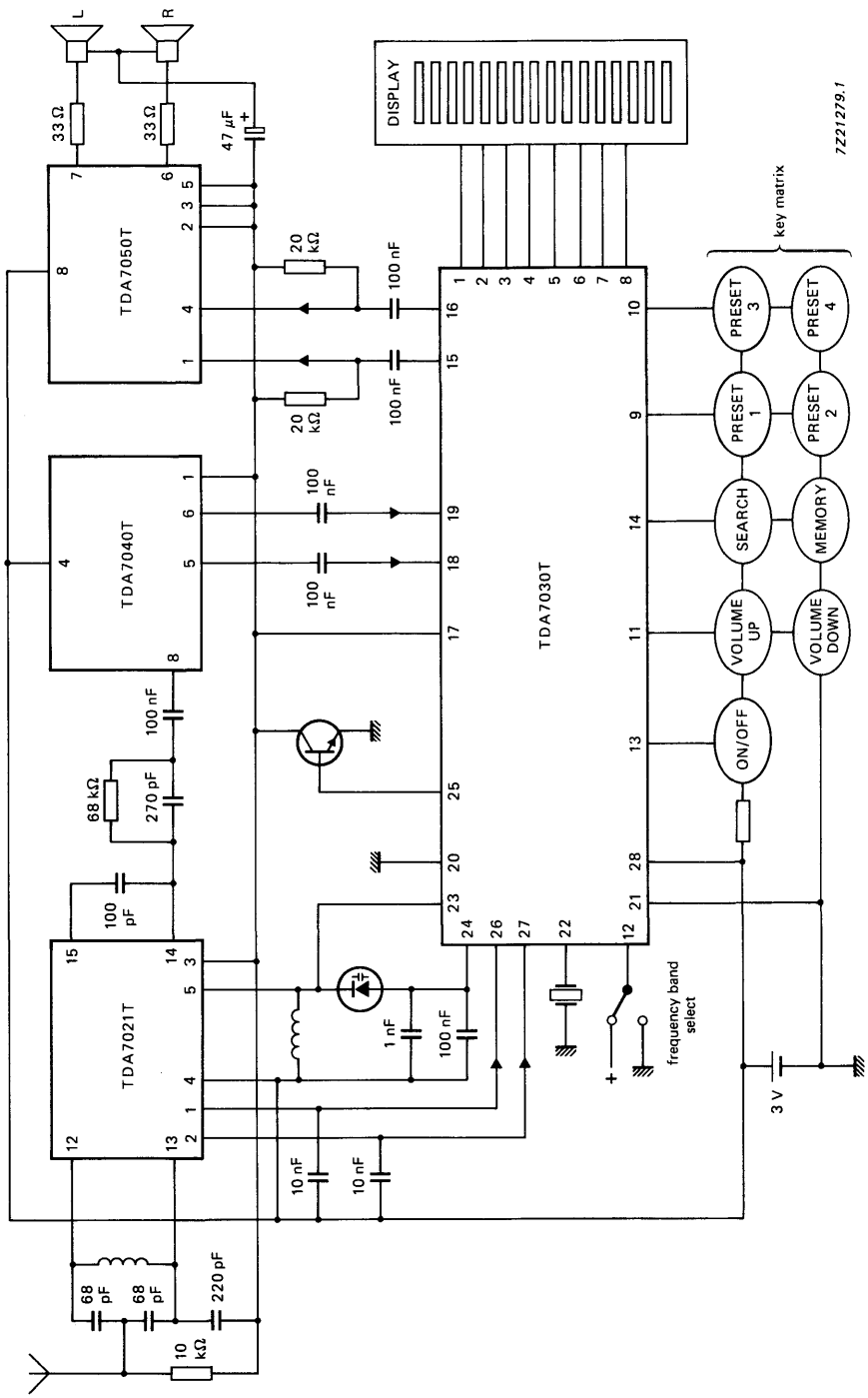


Fig. 3 System application using the TDA7030T in conjunction with the single-chip FM radio receiver (TDA7021T), low voltage stereo decoder (TDA7040T) and low voltage stereo power amplifier (TDA7050T).

LOW VOLTAGE PLL STEREO DECODER

GENERAL DESCRIPTION

The TDA7040T is a monolithic integrated circuit for low cost FM stereo radios with an absolute minimum of peripheral components and a simple lay-out.

Features

- Built-in four pole low pass filter with a 70 kHz corner frequency suppressing unwanted out-of-band input signals
- Fully integrated 228 kHz oscillator
- Pilot presence detector and soft mono/stereo blend
- Built-in interference suppression
- External stereo lamp driver applicable
- Adjustable gain

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_P	1,8	–	6	V
Supply current V_P = 3 V	I_P	–	3	–	mA
Total harmonic distortion	THD	–	0,3	–	%
Signal to noise ratio	S/(S + N)	–	70	–	dB
Channel separation	α	–	40	–	dB

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

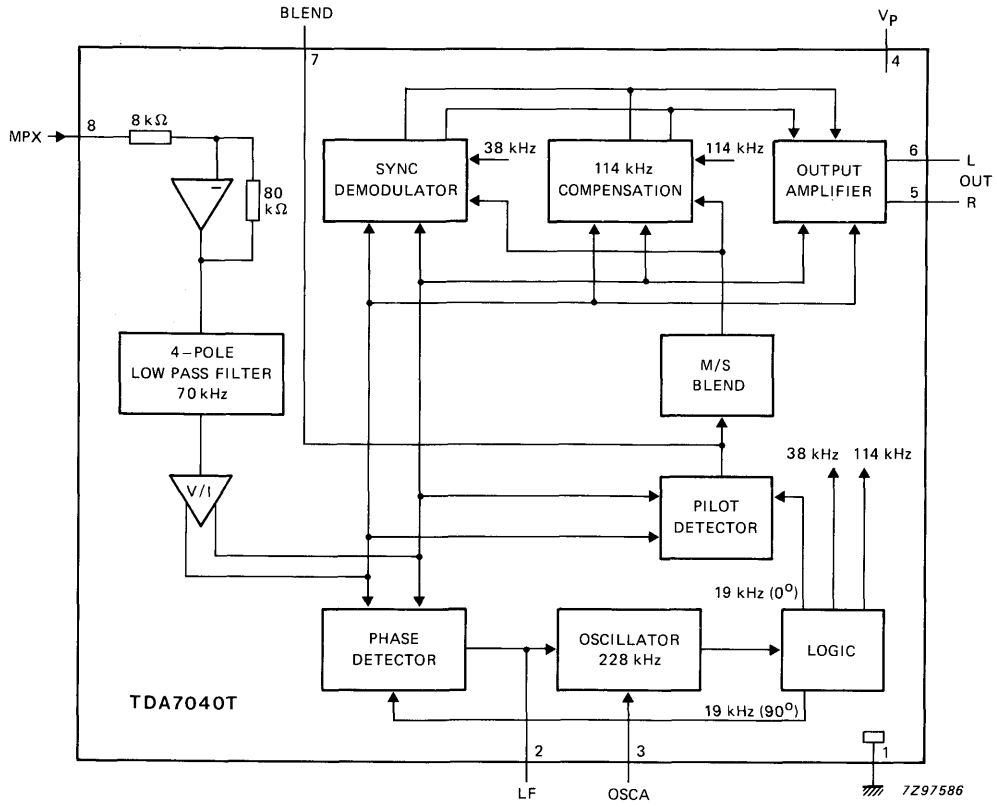


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	–	–	7	V
Operating ambient temperature	T_{amb}	−10	–	+ 70	°C
Storage temperature range	T_{stg}	−55	–	+ 150	°C

CHARACTERISTICS

V_P = 3 V; T_{amb} = 25 °C; test circuit Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_P	1,8	3,0	6,0	V
Supply current	I_P	–	3	4	mA
Output voltage (r.m.s. value) $V_{i(rms)}$ L and R 120 mV; f = 1 kHz	$V_{5,\,6\text{-}1}$	–	240	–	mV
Channel balance $V_{i(rms)}$ L and R 40 mV; f = 1 kHz	ΔG_v	–	0	1	dB
Output resistance	R_O	–	5	–	kΩ
Total harmonic distortion $V_{i(rms)}$ L and R 40 mV; f = 1 kHz	THD	–	0,1	–	%
Total harmonic distortion $V_{i(rms)}$ L and R 40 mV; f = 1 kHz; $V_{p(rms)}$ = 12 mV	THD	–	0,3	–	%
Signal-to-noise ratio $V_{i(rms)}$ = 120 mV; f = 1 kHz	S/(S + N)	–	70	–	dB
Signal-to-noise ratio $V_{i(rms)}$ = 120 mV; f = 1 kHz $V_{p(rms)}$ = 12 mV	S/(S + N)	–	70	–	dB
Channel separation $V_{i(rms)}$ L and R 40 mV; f = 1 kHz; $V_{p(rms)}$ = 12 mV	α	–	40	–	dB
Capture range $V_{p(rms)}$ = 12 mV; deviation from centre frequency	Δf	–	± 3	–	%
Carrier leak $V_{i(rms)}$ L and R 120 mV; $V_{p(rms)}$ = 12 mV; f = 1 kHz; f = 19 kHz		–	30	–	dB
f = 38 kHz		–	50	–	dB
SCA (Subsidiary Communications Authorization) rejection $V_{i(rms)}$ L and R 120 mV; $V_{p(rms)}$ = 12 mV; f = 1 kHz; $V_{SCA(RMS)}$ = 12 mV; f = 67 kHz	α_{67}	–	70	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
ACI (Adjacent channel interference) $V_{i(rms)}$ L and R 120 mV; $V_{p(rms)}$ = 12 mV; f = 1 kHz; $V_{ACI(RMS)}$ = 1,3 mV; f = 114 kHz $V_{ACI(RMS)}$ = 1,3 mV; f = 190 kHz	α_{114} α_{119}	– –	90 85	– –	dB dB
Traffic radio (V.W.F.) suppression $\alpha_{57(VWF)} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz} \pm 23\text{ Hz})}$ measured with: 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 kHz, f_m = 23 Hz AM, m = 60%)	$\alpha_{57(VWF)}$	–	75	–	dB

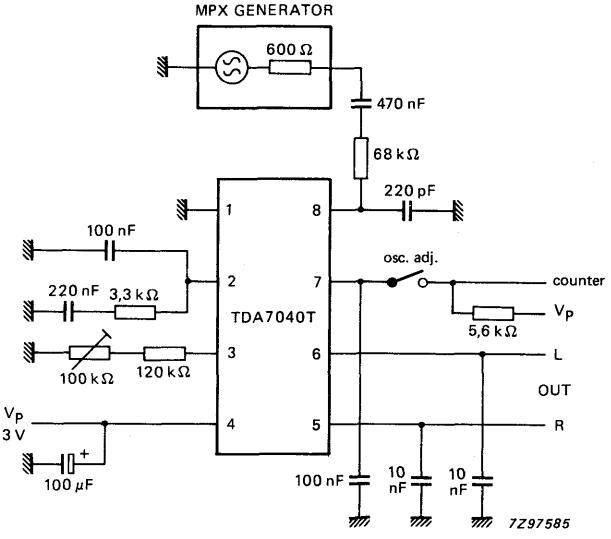


Fig. 2 Test circuit.

DEVELOPMENT DATA

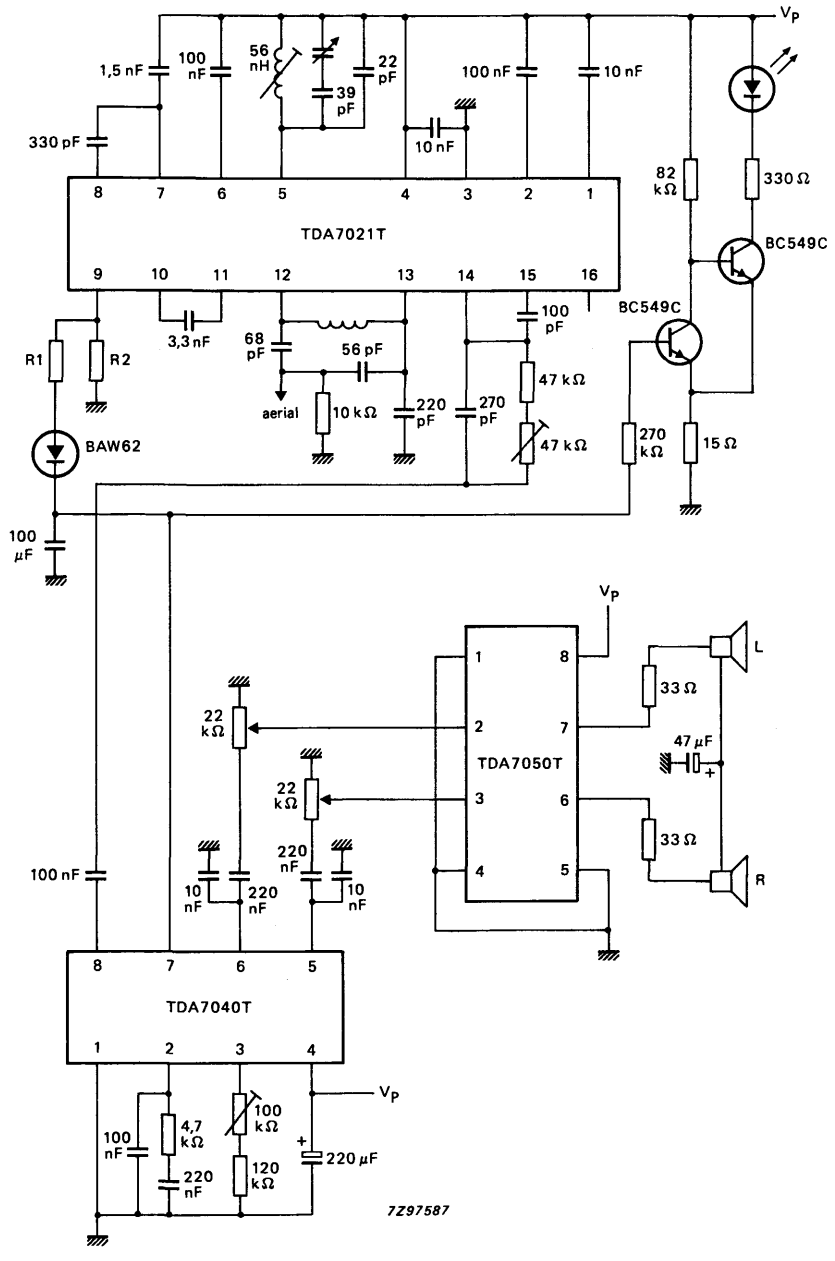


Fig. 3 Application diagram in combination with TDA7021T and TDA7050T.

CHARACTERISTICS

Of the combination TDA7021T, TDA7040T and TDA7050T (Fig. 3).
Conditions unless otherwise specified: $V_{vhf(rms)}$ = 1 mV; f_{hf} = 97 MHz; f_{dev} = 22,5 kHz; $f_{dev\ pilot}$ = 6,75 kHz; noise measured unweighted in a range from 400 Hz to 15 kHz.

parameter	symbol	min.	typ.	max.	unit
Total harmonic distortion (pilot on)					
V_i = (L + R) signal; f_{mod} = 1 kHz	THD	–	0,5	–	%
V_i = L signal; f_{mod} = 1 kHz	THD	–	1,0	–	%
Signal to noise ratio					
V_i = (L + R) signal; f_{mod} = 1 kHz					
pilot off	S/(S + N)	–	56	–	dB
pilot on	S/(S + N)	–	50	–	dB
Channel separation					
V_i = L-signal, f_{mod} = 1 kHz; pilot on; f_{RF} = 97 MHz	α	–	26	–	dB
V_i = L-signal, f_{mod} = 1 kHz; pilot on; f_{RF} = 87,5 MHz and 108 MHz	α	–	14	–	dB
Output voltage (pilot off)					
V_i = (L + R) signal, f_{mod} = 1 kHz	$V_{o(rms)}$	–	80	–	mV

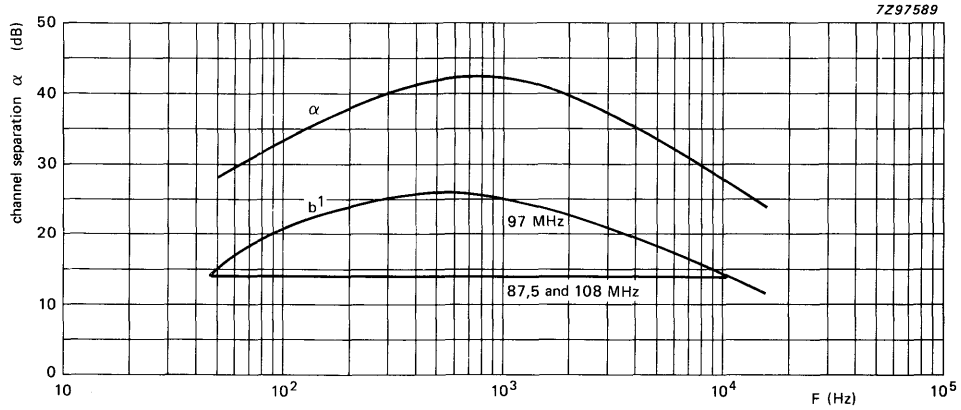


Fig. 4 Channel separation as a function of audio frequency.
a = measured in test circuit (Fig. 2)
b = measured in application diagram (Fig. 3)

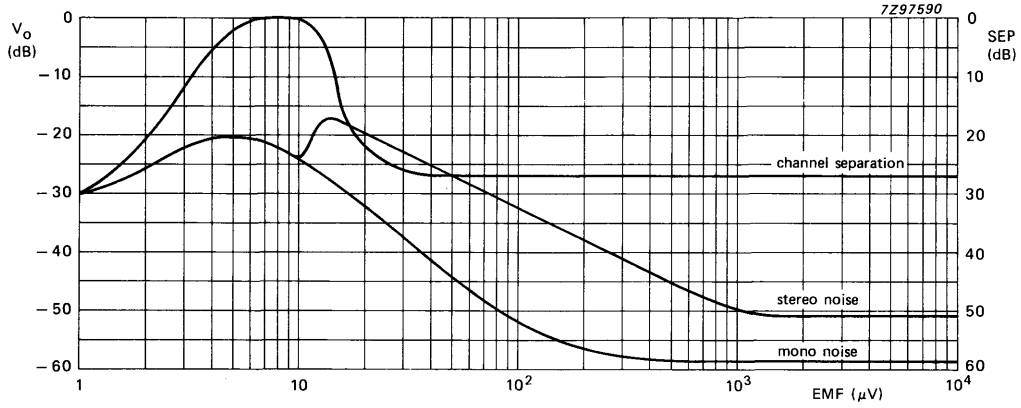


Fig. 5 Signal/noise and channel separation behaviour in Fig. 3. at R1 = 270 kΩ and R2 = 13 kΩ; without diode BAW62.

DEVELOPMENT DATA

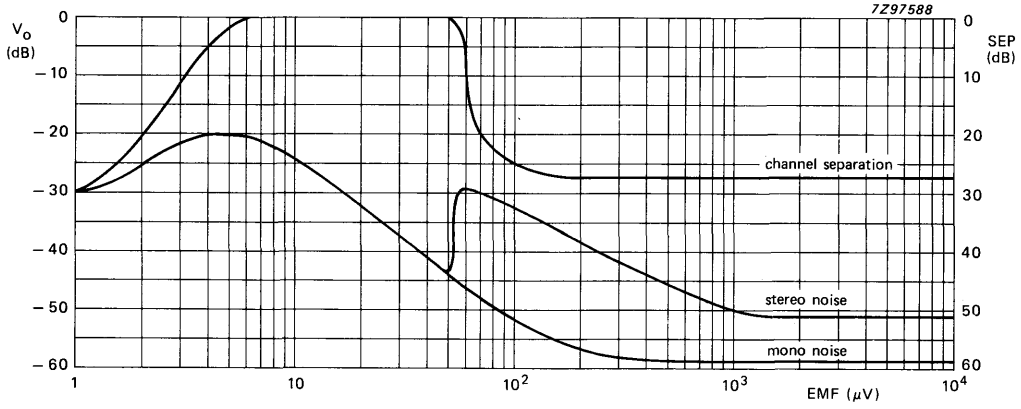


Fig. 6 Signal/noise and channel separation behaviour in Fig. 3. at R1 = 200 kΩ, R2 = 30 kΩ; with diode BAW62.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

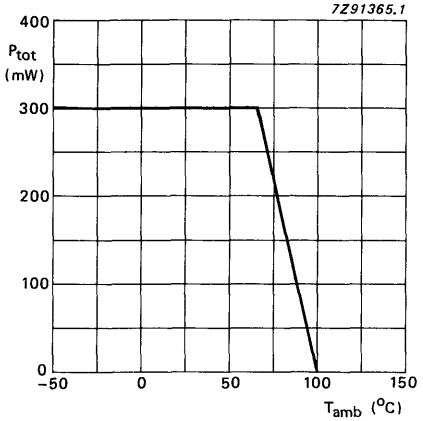


Fig. 1 Power derating curve.

THERMAL RESISTANCE

From junction to ambient $R_{thj\text{-}a}$ = 110 K/W

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\|\Delta V\|$	–	–	70	mV
Input impedance (at R_S = ∞)	$\|Z_i\|$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\|Z_i\|$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

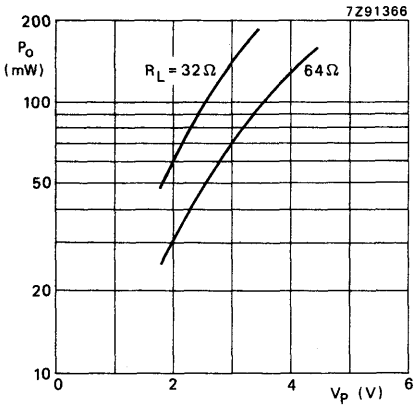


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

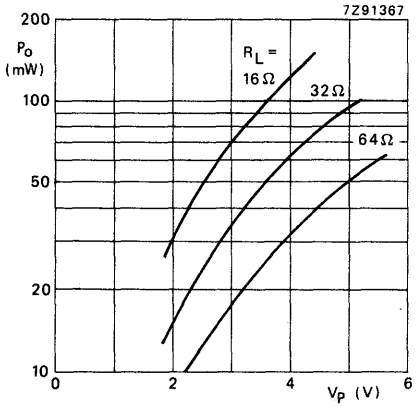


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

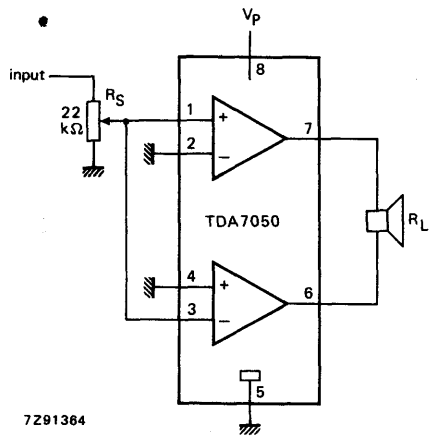


Fig. 4 Application diagram (BTL); also used as test circuit.

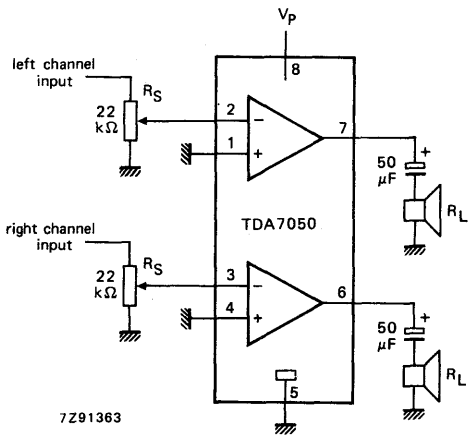


Fig. 5 Application diagram (stereo); also used as test circuit.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

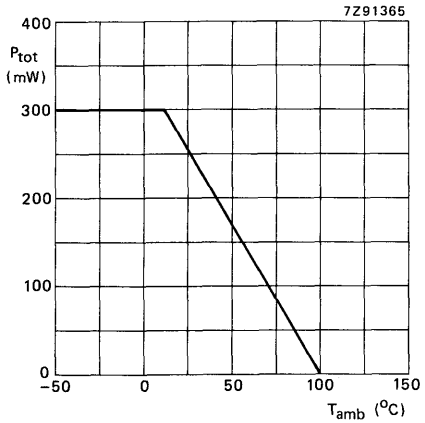


Fig. 1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\ max} - T_{amb}}{R_{th\ j\text{-}a}} = \frac{100-60}{300} = 0{,}1\ W.$$

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

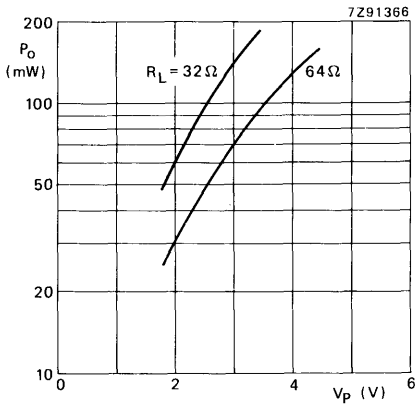


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

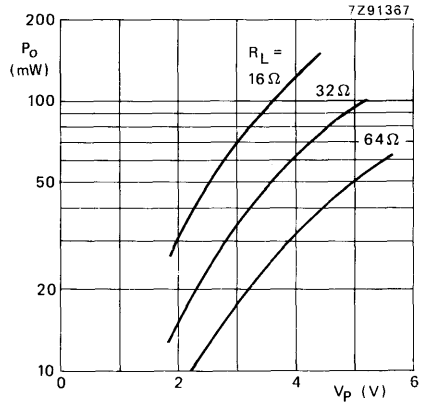


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

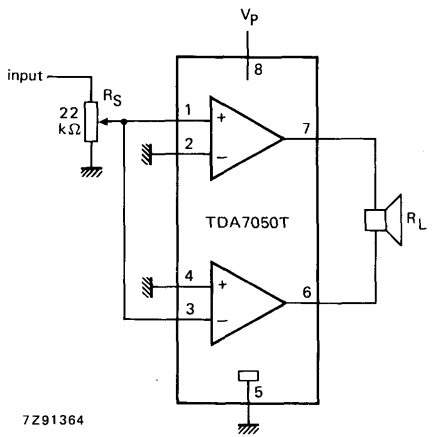


Fig. 4 Application diagram (BTL); also used as test circuit.

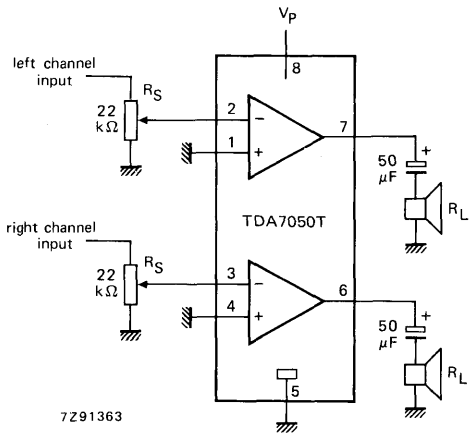


Fig. 5 Application diagram (stereo); also used as test circuit.

1 W BTL MONO AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDA7052 is a mono output amplifier in a 8-lead dual-in-line (DIL) plastic package. The device is designed for battery-fed portable audio applications.

Features:

- No external components
- No switch-on or switch-off clicks
- Good overall stability
- Low power consumption
- No external heatsink required
- Short-circuit proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_V	39	40	41	dB
Output power	THD = 10%; 8 Ω	P_o	–	1,2	–	W
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

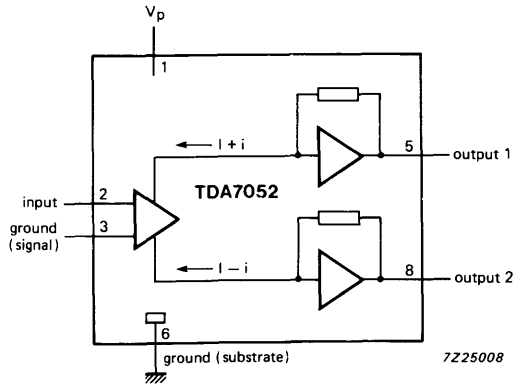


Fig. 1 Block diagram.

PINNING

1	V_P	supply voltage	5	OUT1	output 1
2	IN	input	6	GND2	ground (substrate)
3	GND1	ground (signal)	7	n.c.	not connected
4	n.c.	not connected	8	OUT2	output 2

FUNCTIONAL DESCRIPTION

The TDA7052 is a mono output amplifier designed for battery-fed portable audio applications, such as tape recorders and radios.
The gain is fixed internally at 40 dB. A large number of tape recorders and radios are still designed for mono sound, plus a space-saving trend by reduction of the number of battery cells. This means a decrease in supply voltage which results in an reduction of output power. To compensate for this reduction, the TDA7052 uses the Bridge-Tied-Load principle (BTL) which can deliver an output power of 1,2 W (THD = 10%) into an 8 Ω load with a power supply of 6 V. The load can be short-circuited at each signal excursion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	18	V
Non-repetitive peak output current	I_{OSM}	–	1,5	A
Total power dissipation	P_{tot}	see Fig. 2		
Crystal temperature	T_c	–	150	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

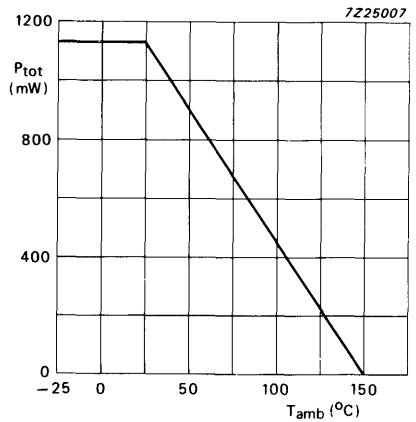


Fig. 2 Power derating curve.

POWER DISSIPATION

Assume V_P = 6 V; R_L = 8 Ω; T_{amb} = 50 °C maximum.
The maximum sinewave dissipation is 0,9 W.

$$R_{th\,j\text{-}a} = \frac{150 - 50}{0{,}9} \approx 110 \text{ K/W}.$$

Where $R_{th\,j\text{-}a}$ of the package is 110 K/W, so no external heatsink is required.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	39	40	41	dB
Output power	THD = 10%	P_o	*	1,2	–	W
Noise output voltage (RMS value)						
	note 1	$V_{no(rms)}$	–	150	300	μV
	note 2	$V_{no(rms)}$	–	60	–	μV
Frequency response		f_r	–	20 Hz to 20 kHz	–	Hz
Supply voltage ripple rejection	note 3	SVRR	40	50	–	dB
DC output offset voltage pin 5 to 8	R_S = 5 kΩ	ΔV_{5-8}	–	–	100	mV
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%
Input impedance		$\|Z_i\|$	–	100	–	kΩ
Input bias current		I_{bias}	–	100	300	nA

Notes to the characteristics

1. The unweighted RMS noise output voltage is measured at a bandwidth of 60 Hz to 15 kHz with a source impedance (R_S) of 5 kΩ.
2. The RMS noise output voltage is measured at a bandwidth of 5 kHz with a source impedance of 0 Ω and a frequency of 500 kHz. With a practical load (R = 8 Ω; L = 200 μH) the noise output current is only 100 nA.
3. Ripple rejection is measured at the output with a source impedance of 0 Ω and a frequency between 100 Hz and 10 kHz. The ripple voltage = 200 mV (RMS value) is applied to the positive supply rail.

* Value to be fixed.

APPLICATION INFORMATION

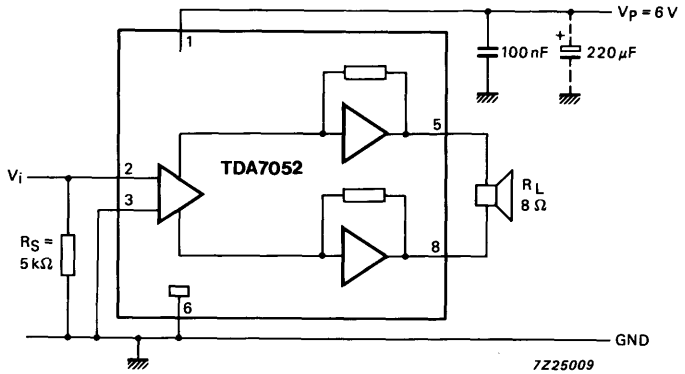


Fig. 3 Application diagram.

DEVELOPMENT DATA

2 × 1 W PORTABLE/MAINS-FED STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7053 is an integrated class-B stereo power amplifier in a 16-lead dual-in-line (DIL) plastic package. The device, consisting of two BTL amplifiers, is primarily developed for portable audio applications but may also be used in mains-fed applications.

Features

- No external components
- No switch-ON/OFF clicks
- Good overall stability
- Low power consumption
- Short-circuit-proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	9	16	mA
Output power	$R_L = 8\ \Omega$; $V_P = 6$ V	P_O	–	1.2	–	W
Internal voltage gain		G_V	38	39	40	dB
Total harmonic distortion	$P_O = 0.1$ W	THD	–	0.2	1.0	%

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

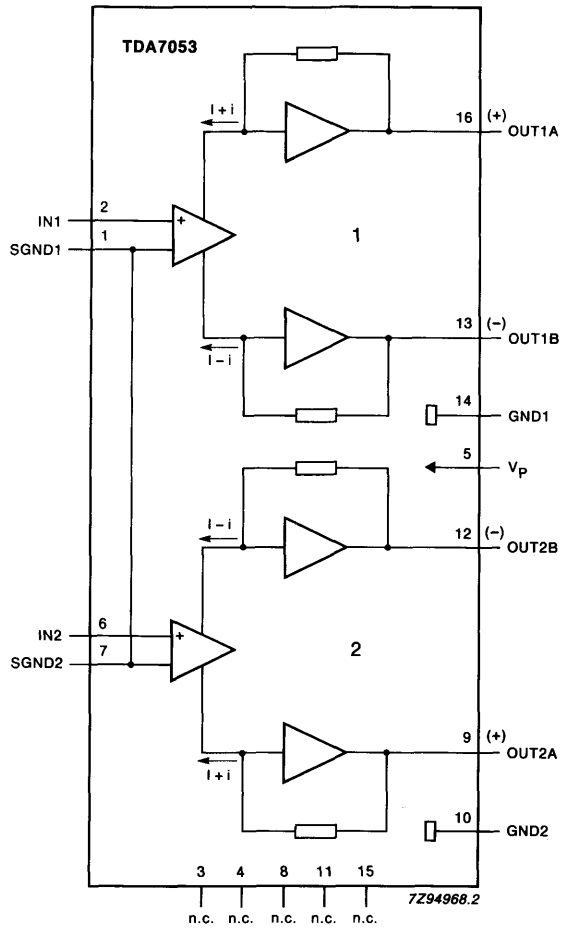


Fig. 1 Block diagram.

PINNING

1.	SGND1	signal ground 1	9.	OUT2A	output 2 (positive)
2.	IN1	input 1	10.	GND2	power ground 2
3.	n.c.	not connected	11.	n.c.	not connected
4.	n.c.	not connected	12.	OUT2B	output 2 (negative)
5.	Vp	supply voltage	13.	OUT1B	output 1 (negative)
6.	IN2	input 2	14.	GND1	power ground 1
7.	SGND2	signal ground 2	15.	n.c.	not connected
8.	n.c.	not connected	16.	OUT1A	output 1 (positive)

Note

The information contained within the parentheses refer to the polarity of the loudspeaker terminal to which the output must be connected.

FUNCTIONAL DESCRIPTION

The TDA7053 is a stereo output amplifier, with an internal gain of 39 dB, which is primarily for use in portable audio applications but may also be used in mains-fed applications. The current trends in portable audio application design is to reduce the number of batteries which results in a reduction of output power when using conventional output stages. The TDA7053 overcomes this problem by using the Bridge-Tied-Load (BTL) principle and is capable of delivering 1.2 W into an 8 Ω load (V_P = 6 V). The load can be short-circuited under all input conditions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	18	V
Non-repetitive peak output current		I_{OSM}	–	1.5	A
Total power dissipation		P_{tot}	see Fig. 2		
Crystal temperature		T_c	–	+150	°C
Storage temperature range		T_{stg}	−65	+150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	50	K/W

Power dissipation

Assuming: $V_P = 6$ V and $R_L = 8\ \Omega$:

The maximum sinewave dissipation is 1.8 W, therefore $T_{amb(max.)} = 150 - (50 \times 1.8) = 60$ °C.

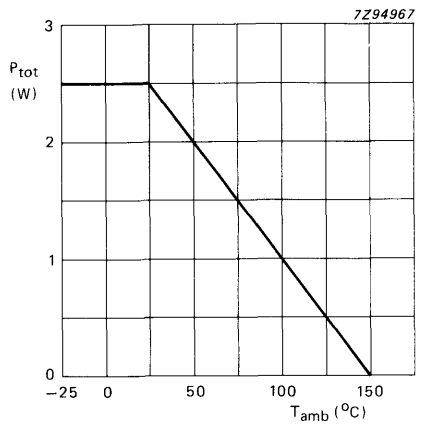


Fig. 2 Power derating curve.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; T_{amb} = 25 °C; unless otherwise specified; measured from test circuit, Fig. 7.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	R_L = ∞; note 1	I_{tot}	–	9	16	mA
Input bias current		I_{bias}	–	100	300	nA
Supply voltage ripple rejection	note 2	SVRR	40	50	–	dB
Input impedance		Z_I	–	100	–	kΩ
DC output offset voltage	note 3	ΔV_{13-16}	–	–	100	mV
		ΔV_{12-9}	–	–	100	mV
Noise output voltage (RMS value)	note 4	$V_{no(rms)}$	–	150	300	μV
	note 5	$V_{no(rms)}$	–	60	–	μV
Output power	THD = 10%	P_O	–	1.2	–	W
Total harmonic distortion	P_O = 0.1 W	THD	–	0.2	1.0	%
Internal voltage gain		G_V	38	39	40	dB
Channel balance		ΔG_V	–	–	1	dB
Channel separation	note 3	α	40	–	–	dB
Frequency response		f	–	0.02 to 20	–	kHz

Notes to the characteristics

1. With a practical load the total quiescent current depends on the offset voltage.
2. Ripple rejection measured at the output with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage (200 mV) is applied to the positive supply rail.
3. R_S = 5 kΩ.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ, unweighted and a bandwidth of 60 Hz to 15 kHz.
5. The noise output voltage (RMS value) is measured with R_S = 0 Ω and f = 500 kHz with 5 kHz bandwidth. If R_L = 8 Ω and L_L = 200 μH the noise output current is only 100 nA.

DEVELOPMENT DATA

APPLICATION INFORMATION

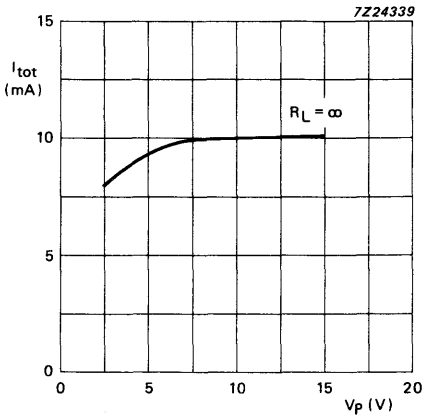


Fig. 3 Quiescent current as a function of voltage supply (V_P); T_{amb} = 60 °C.

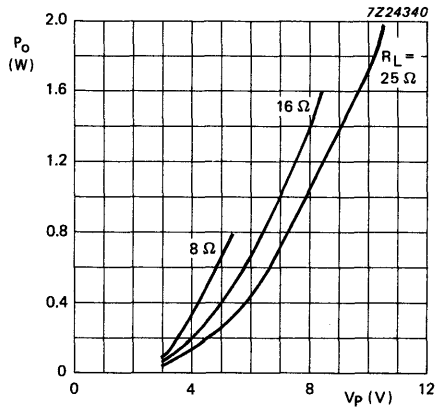
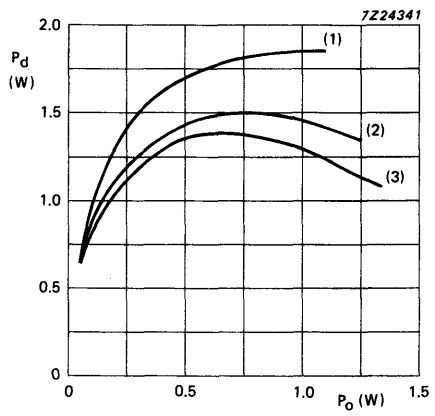
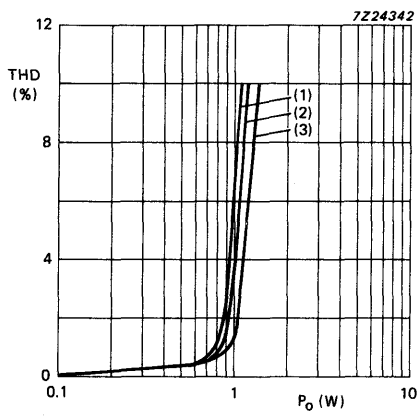


Fig. 4 Output power as a function of voltage supply (V_P); THD = 10%; f = 1 kHz; T_{amb} = 60 °C.



(1) V_P = 6.0 V; R_L = 8 Ω
(2) V_P = 7.5 V; R_L = 16 Ω
(3) V_P = 9.0 V; R_L = 25 Ω

Fig. 5 Power dissipation as a function of output power; f = 1 kHz; T_{amb} = 60 °C.



(1) V_P = 6.0 V; R_L = 8 Ω
(2) V_P = 7.5 V; R_L = 16 Ω
(3) V_P = 9.0 V; R_L = 25 Ω

Fig. 6 Total harmonic distortion as a function of output power; f = 1 kHz; T_{amb} = 60 °C.

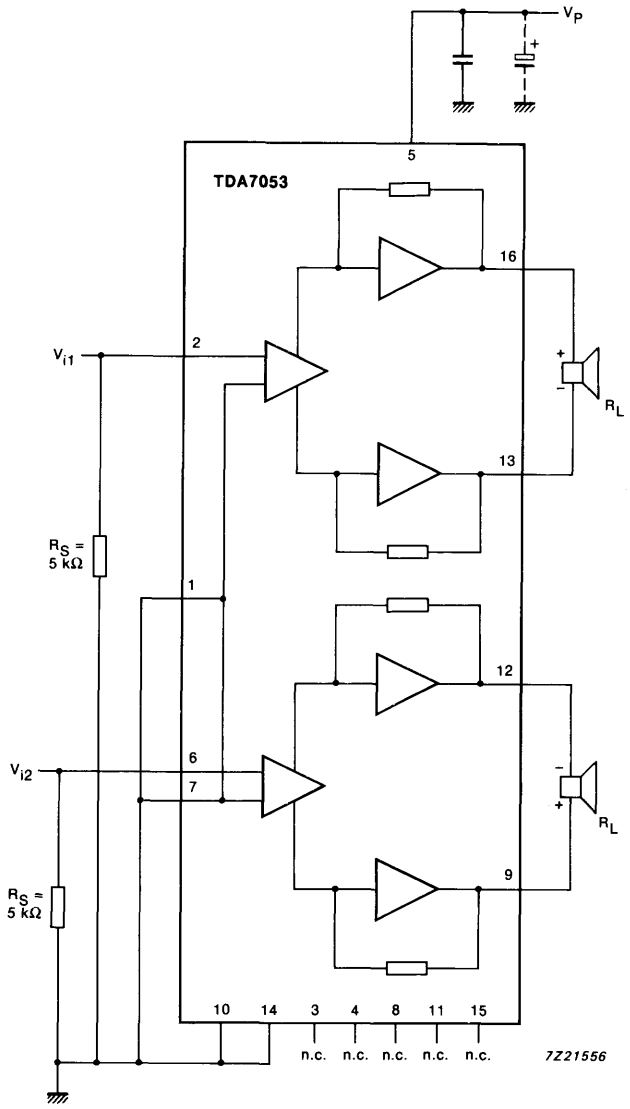


Fig. 7 Test and application circuit diagram.

APPLICATION INFORMATION (continued)

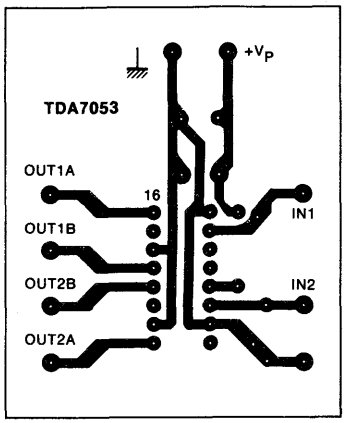


Fig. 8 Printed-circuit board, track side.

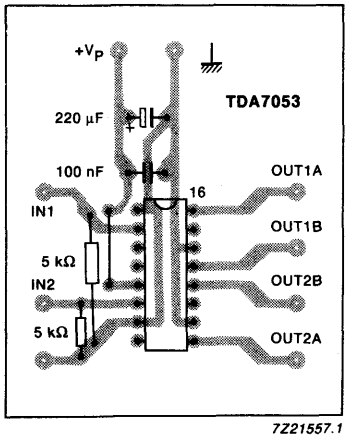


Fig. 9 Printed-circuit board, component side.

HI-FI STEREO AUDIO PROCESSOR; I²C BUS

GENERAL DESCRIPTION

The TDA8420 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel (CH1) and a headphone channel (CH2), digital controlled via the I²C bus, for application in hi-fi audio and television sound.

Features

- Input selector
- Mode selector
- Loudspeaker channel (CH1) } with volume control, balance control and mute
- Headphone channel (CH2) }
- Pseudo stereo and spatial function
- Bass and treble control

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	200	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	90	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Channel separation	α	–	75	–	dB
Volume control range CH1	G	–46	–	16	dB
Treble control range	G	–12	–	12	dB
Bass control range	G	–12	–	15	dB
Volume control range CH2	G	–62	–	0	dB

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117).

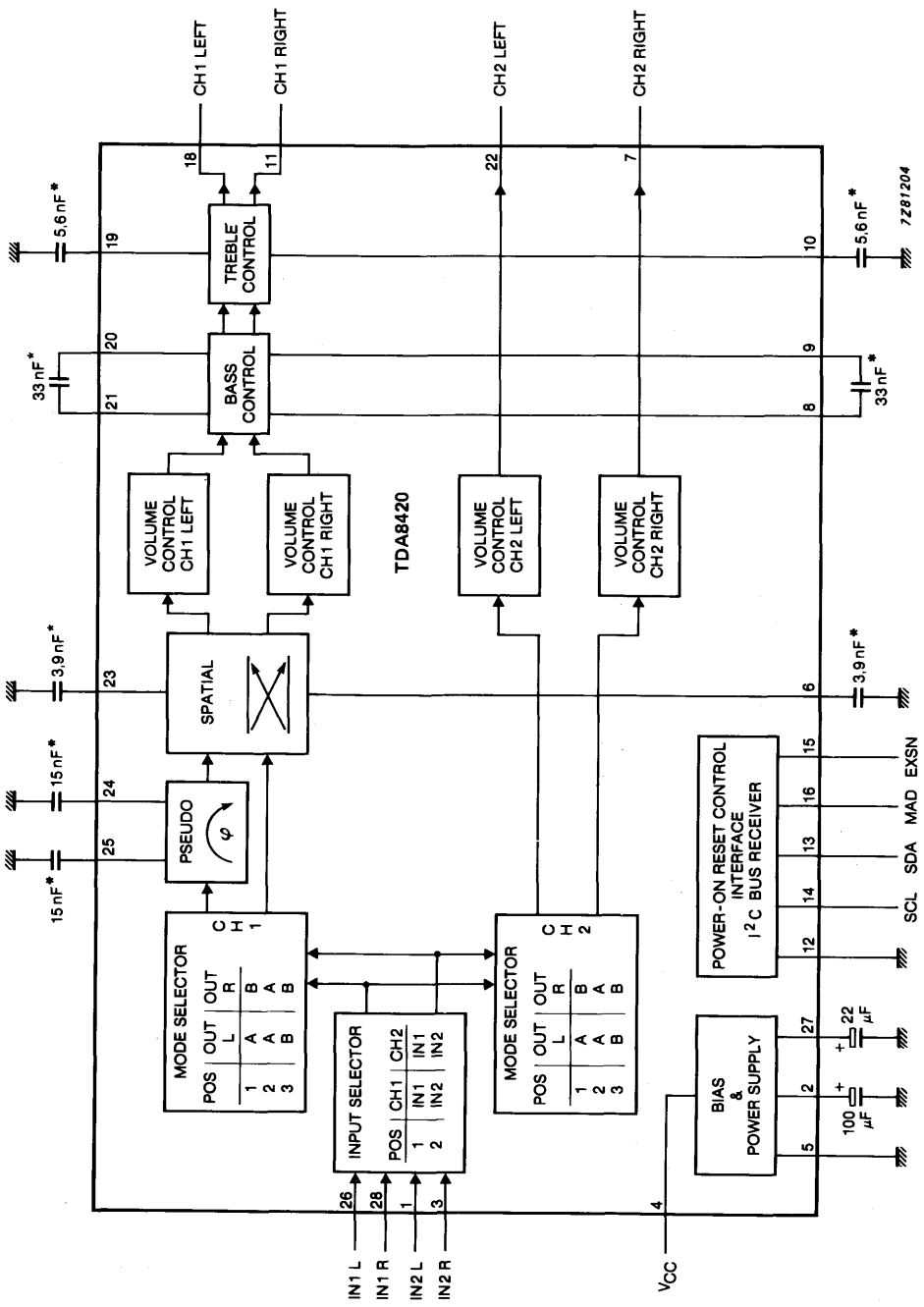


Fig. 1 Block diagram.

* These values are dependent on the required frequency response and effect.

PINNING

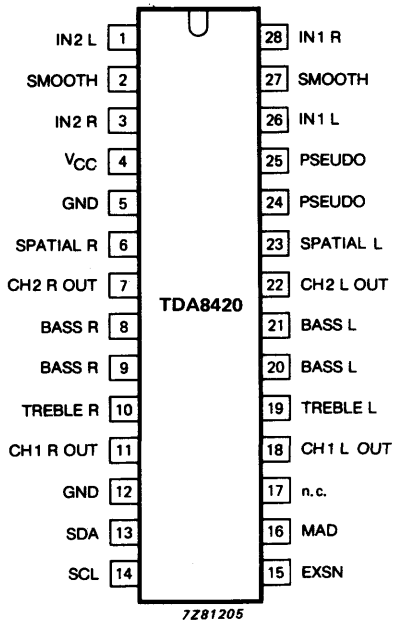


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Input selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the input selector. The selection is made from the following AF input signals:

- IN1 L (pin 26); IN1 R (pin 28)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Where IN1 is an internal input signal and IN2 an external input signal.

Mode selector

For each channel (CH1 and CH2) there is a mode selector which selects between stereo, sound A and sound B in the event of bilingual transmission. Both mode selectors can be controlled independently.

Headphone channel (CH2)

Volume control and balance

The stages for volume control for CH2 consist of two parts for left and right. In each part the gain can be adjusted between 0 and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Loudspeaker channel (CH1)

Volume control and balance

The loudspeaker channel (CH1) also consists of two parts for volume control (left and right). In each part the gain can be adjusted between + 16 dB and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Stereo/pseudo stereo/spatial stereo mode

It is possible to select three modes. Stereo, pseudo or spatial stereo. The pseudo stereo mode receives mono transmissions and the stereo and spatial stereo mode receives stereo transmissions.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8420 includes a bias and power supply stage, which generates a voltage of ½ V_{CC} with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both the loudspeaker channel (CH1) and the headphone channel (CH2). The muting can be switched by transmission of the mute bit.

I^2C bus receiver and data handling

Bus specification

The TDA8420 is controlled via the 2-wire I^2C bus by a microcomputer. The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8420 starts with the module address MAD.

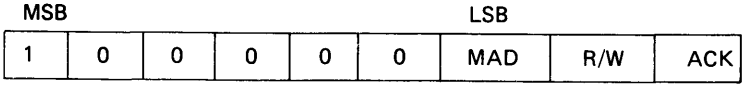


Fig. 3 TDA8420 module address.

The module address is determined by pin 16. When connected to ground MAD = 0; when connected to V_{CC} MAD = 1. Thus two TDA8420s can be selected within a system.

Subaddress

After the module address byte a second byte is used to select the functions for both channels:

- CH1 – Volume left, volume right, bass, treble and switch functions
- CH2 – Volume left, volume right and switch functions

The subaddress SAD is stored within the TDA8420. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

		128	64	32	16	8	4	2	1
	function	MSB 7	6	5	4	3	2	1	LSB 0
CH1	volume left	0	0	0	0	0	0	0	0
	volume right	0	0	0	0	0	0	0	1
	bass	0	0	0	0	0	0	1	0
	treble	0	0	0	0	0	0	1	1
	switch functions	0	0	0	0	1	0	0	0
CH2	volume left	0	0	0	0	0	1	0	0
	volume right	0	0	0	0	0	1	0	1
	switch functions	0	0	0	0	1	1	0	0
						subaddress SAD			

Definition of 3rd byte

A third byte is used to transmit data to the TDA8420. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

	function		MSB 7	6	5	4	3	2	1	LSB 0
CH1	volume left	VL1	1	1	V05	V04	V03	V02	V01	V00
	volume right	VR1	1	1	V15	V14	V13	V12	V11	V10
	bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
	treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
	switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS
CH2	volume left	VL2	1	1	V25	V24	V23	V22	V21	V20
	volume right	VR2	1	1	V35	V34	V33	V32	V31	V30
	switch functions	S2	1	1	1	1	EXS	MH1	MH0	1

Truth tables

Truth tables for the switch functions

Table 3 Input selector

function	IS
IN1	0
IN2	1

Table 4 Mode selectors

	CH1		CH2	
mode	ML0	ML1	MH0	MH1
stereo	1	1	1	1
sound A	1	0	1	0
sound B	0	1	0	1
----------	0	0	0	0

Table 5 Stereo/pseudo stereo/spatial stereo

choice	STL	EFL
spatial	1	1
stereo	1	0
pseudo	0	1
----------	0	0

Table 6 Mute

mute	MU
active; automatic after POR	1
not active	0

Where: POR = Power-On Reset.

Table 7 Output for external switch

EXSN	EXS
ground	1
open collector	0

Truth tables for the volume base and treble controls.

Table 8 Volume control

CH1	CH2	Vx5	Vx4	Vx3	Vx2	Vx1	Vx0
16	0	1	1	1	1	1	1
–46	–62	1	0	0	0	0	0
$\leqslant$ –90	$\leqslant$ –90	0	1	1	1	1	1
$\leqslant$ –90	$\leqslant$ –90	0	0	0	0	0	0

Where: The values of CH1 and CH2 are in 2 dB/step measured in dBs.

Table 9 Bass control

3dB/step (dB)	BA3	BA2	BA1	BA0
15	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
15	1	0	1	1
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Table 10 Treble control

3dB/step (dB)	TR3	TR2	TR1	TR0
12	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all eight functions have to be adjusted with eight data transmissions. It is recommended that data information for switch functions in CH1 are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 5. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

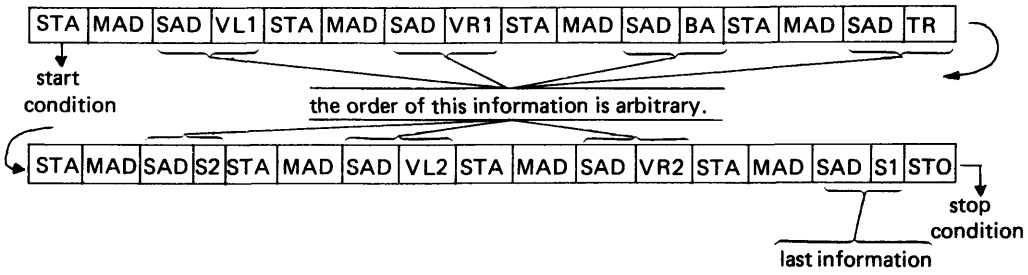


Fig. 4 Data transmission after a power-on reset.

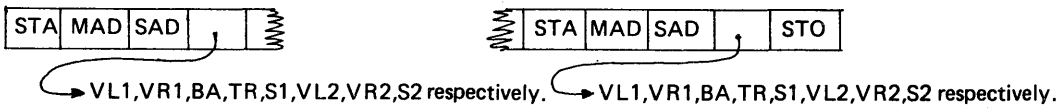


Fig. 5 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range for external capacitors				
pins 2, 6, 8 to 10, 19 to 21, 23 to 25, 27	V_{cap}	0	V_{CC}	V
pin 13	V_{SDA}	0	V_{CC}	V
pin 14	V_{SCL}	0	V_{CC}	V
pin 15	V_{EXSN}	0	V_{CC}	V
pin 16	V_{MAD}	0	V_{CC}	V
Input voltage range				
at pins 1, 3, 7, 11, 18, 22, 26, 28	V_I	0	V_{CC}	V
Output voltage range				
at pins 1, 3, 7, 11, 18, 22, 26, 28	V_O	0	V_{CC}	V
Output current at pins 7, 11, 18, 22	I_O	–	45	mA
Total power dissipation				
at $T_{amb} < 70$ °C	P_{tot}	–	1350	mW
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	–25	150	°C

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Supply current					
at V_{CC} = 12 V	I_{CC}	–	42	55	mA
Input voltage					
IN1 L, IN1 R, IN2 L, IN2 R					
DC voltage internally generated; capacitive coupling recommended	V_I	5,4	6,0	6,6	V
MAD (pin 16)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	0	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
SDA; SCL (pins 13 and 14)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
Output voltage					
CH1 (pins 11 and 18); CH2 (pins 7 and 22)	V_O	5,4	½ V_{CC}	6,6	V
External capacitors					
pins 6 to 10; 19 to 21; 23 to 25	$V_{cap.n}$	–	½ V_{CC}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0,1	–	V
External switch (pin 15)					
at I_{EXSN} = 1 mA					
Output voltage HIGH	V_{EXSNH}	–	–	16	V
Output voltage LOW	V_{EXSNL}	–	–	0,3	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 100\ pF$; T_{amb} = 25 °C unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 6)					
SDA, SCL (pin 13 and 14)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0,3	μs
Set-up time for start condition	$t_{SU;STA}$	4,7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
Input signals					
IN1 L (pin 26) IN1 R (pin 28) IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (r.m.s. value) at V_u = –4 dB; THD ≤ 0,5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_{n-5}	35	50	–	kΩ
Frequency response (–0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
LOUDSPEAKER CHANNEL OUTPUTS					
CH1 LEFT (pin 18); CH1 RIGHT (pin 11)					
Output voltage range (r.m.s. value) at THD $\leqslant$ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level weighted according to CCIR468-2					
gain = 16 dB	V_n	–	90	–	μV
gain = 0 dB	V_n	–	20	40	μV
gain = $\leqslant$ –90 dB	V_n	–	15	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz) for $V_{i(rms)}$ = 0,5 V; gain = + 16 dB to –30 dB	THD	–	0,05	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = + 2 dB to –30 dB	THD	–	0,07	0,2	%
for $V_{i(rms)}$ = 2,0 V; gain = –4 dB to –30 dB	THD	–	0,1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
VOLUME CONTROL					
For truth table see Table 8					

parameter	symbol	min.	typ.	max.	unit
Loudspeaker channel (CH1)					
Control range at f = 1 kHz					
maximum voltage gain (16 dB step)	G_{max}	15	–	–	dB
minimum voltage gain (–46 dB step)	G_{min}	–43	–	–	dB
last position	G_{off}	–80	–85	–	dB
mute position	G_{mute}	–85	–90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 16 dB to –30 dB	ΔG	–	–	0,5	dB
gain from –30 dB to –46 dB	ΔG	–	–	1	dB
TREBLE CONTROL (CH1)					
For truth table see Table 10					
Control range for $C_{10\text{-}5}$; $C_{19\text{-}5}$ = 5,6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
BASS CONTROL					
For truth table see Table 9					
Control range for $C_{8\text{-}9}$; $C_{20\text{-}21}$ = 33 nF					
Maximum emphasis at 40 kHz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial:					
Antiphase crosstalk	α	–	50	–	%
Pseudo:					
Phase shift			(see Fig. 15)		

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
HEADPHONE CHANNEL OUTPUTS					
CH2 LEFT (pin 22); CH2 RIGHT (pin 7)					
Output voltage range (r.m.s. value) at THD ⩽ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level (weighted according to CCIR468-2)					
gain = 0 dB	V_n	–	15	–	μV
gain = 16 dB	V_n	–	12	25	μV
gain = ⩽ –90 dB	V_n	–	10	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,2 V; gain = 0 dB to –30 dB	THD	–	0,01	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = 0 dB to –30 dB	THD	–	0,1	–	%
for $V_{i(rms)}$ = 2,0 V gain = –4 dB to –30 dB	THD	–	0,3	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
Crosstalk between any input/output f = 100 Hz to 12,5 kHz	α	65	70	–	dB
Crosstalk IN1/IN2 gain = 0 dB; R_G = 0	α	95	100	–	dB

parameter	symbol	min.	typ.	max.	unit
Headphone channel (CH2)					
Control range					
maximum voltage gain (0 dB step)	G_{max}	−1	–	–	dB
minimum voltage gain (−62 dB step)	G_{min}	−57	–	–	dB
last position	G_{off}	−80	−85	–	dB
mute position	G_{mute}	−85	−90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 0 dB to −40 dB	ΔG	–	–	0,5	dB
gain from −40 dB to −62 dB	ΔG	–	–	2	dB

Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels.

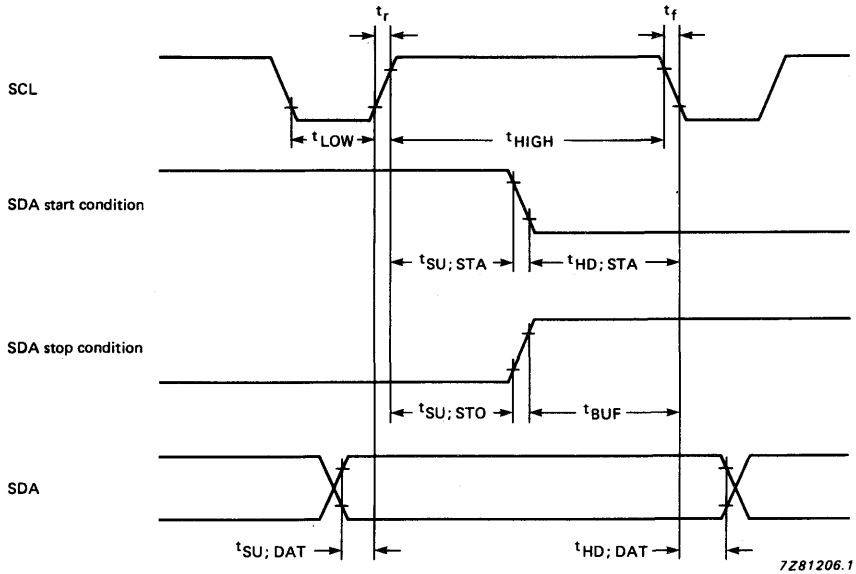


Fig. 6 Timing requirements for I^2C bus.

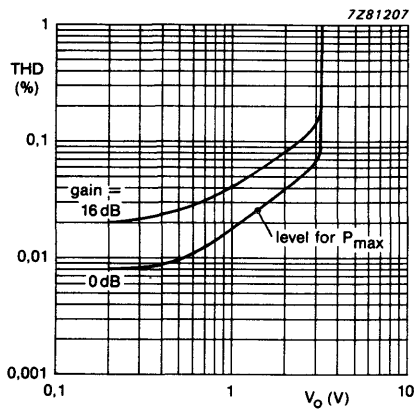


Fig. 7 Distortion loudspeaker channel CH1 as a function of the output voltage with gain as parameter.

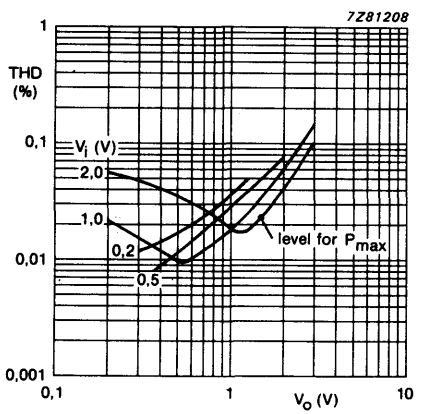


Fig. 8 Distortion loudspeaker channel CH1 as a function of the output voltage with input voltage as parameter.

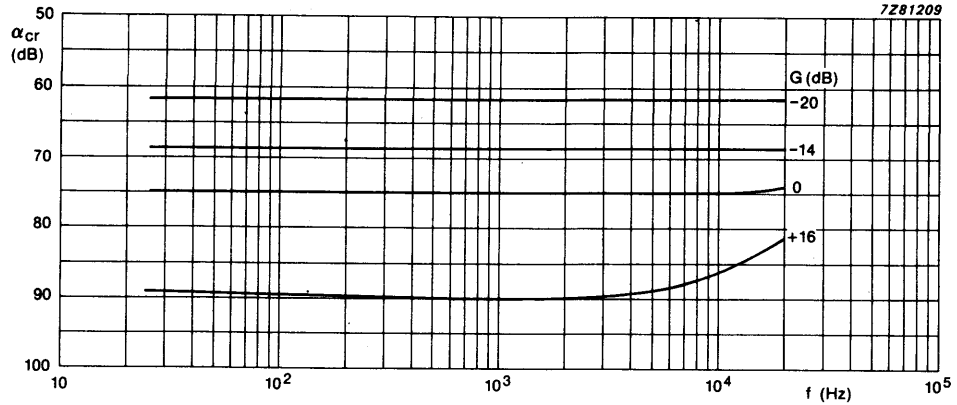


Fig. 9 Channel separation loudspeaker channel CH1 as a function of frequency.

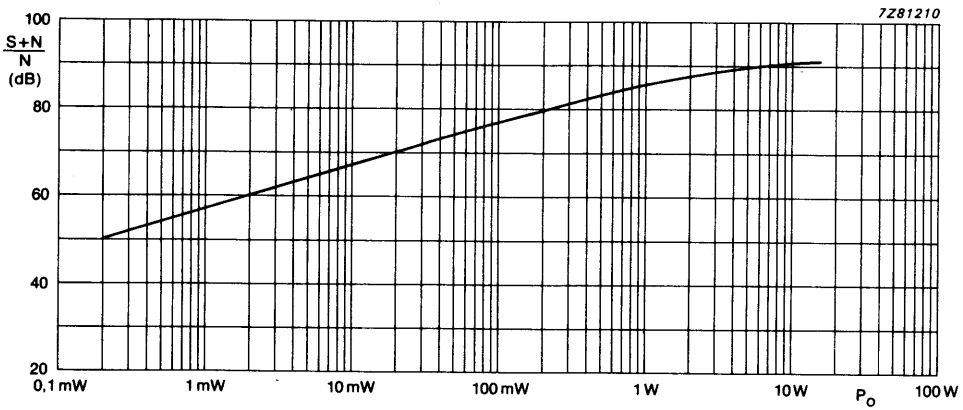


Fig. 10 Signal-to-noise ratio as a function of output power.
Input voltage V_i = 0,5 V; according to CCIR; quasi peak; P_o = 15 W.

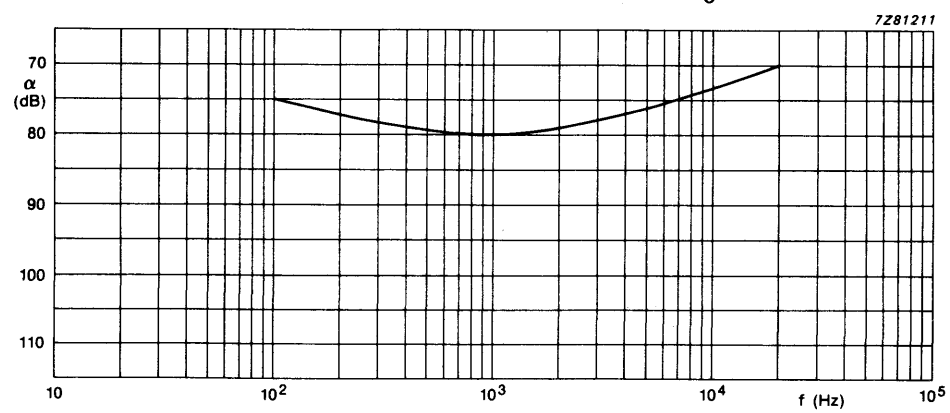


Fig. 11 Crosstalk 2-tone mode as a function of frequency.
CH1: mode AA, Gain + 16 dB; CH2: mode BB, Gain 0 dB. Signal input RIGHT; input LEFT to ground, measured at output CH1.

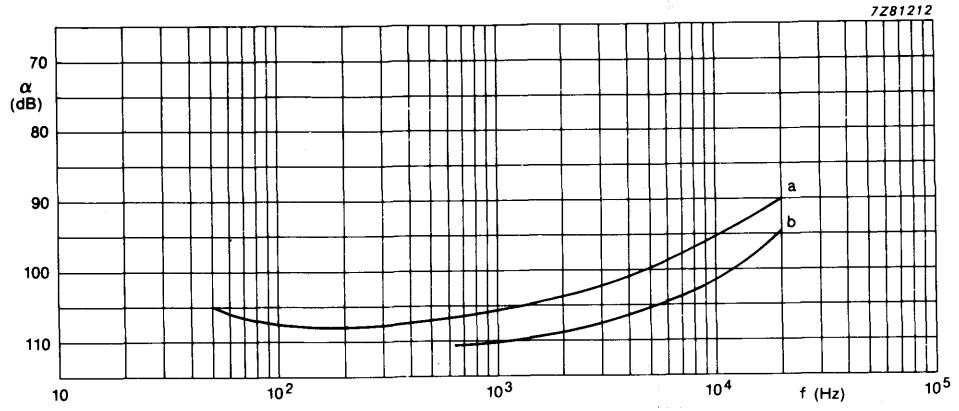


Fig. 12 Crosstalk between IN1 and IN2 as a function of frequency; measured at output CH1, $R_G = 0$.
a) Gain = + 16 dB; V_i = 200 mV. b) Gain = 0 dB; V_i = 1 V.

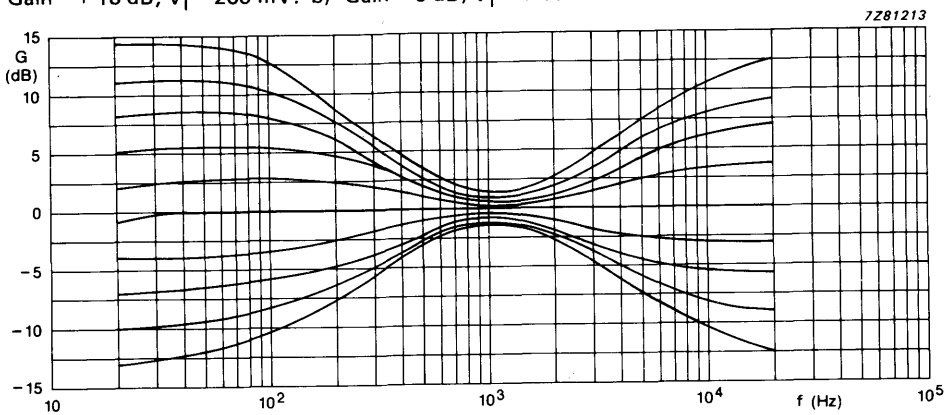


Fig. 13 Bass and treble tone control. C_{bass} = 33 nF, C_{treble} = 5,6 nF.

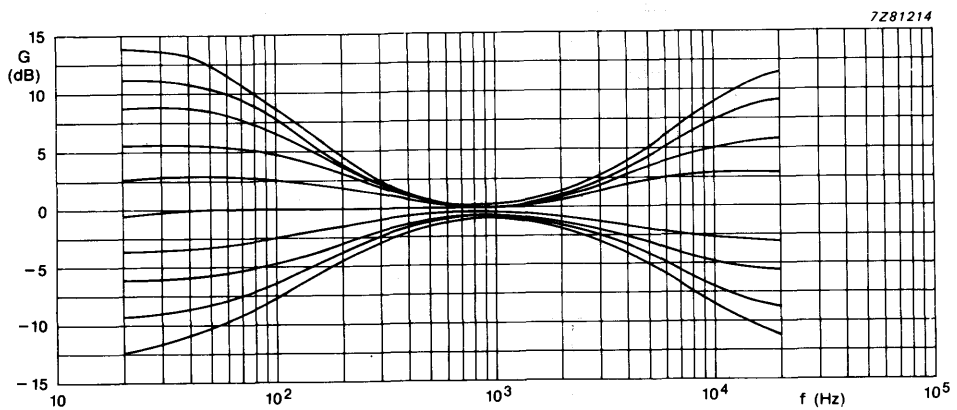
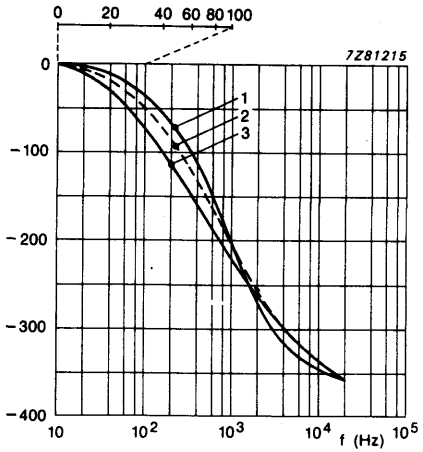


Fig. 14 Bass and treble tone control. C_{bass} = 68 nF, C_{treble} = 3,9 nF.



curve	C_{24} (nF)	C_{25} (nF)	effect
1	15	15	normal
2	5,6	47	intensified
3	5,6	68	more intensified

Fig. 15 Pseudo (phase) as a function of frequency CH1 left.

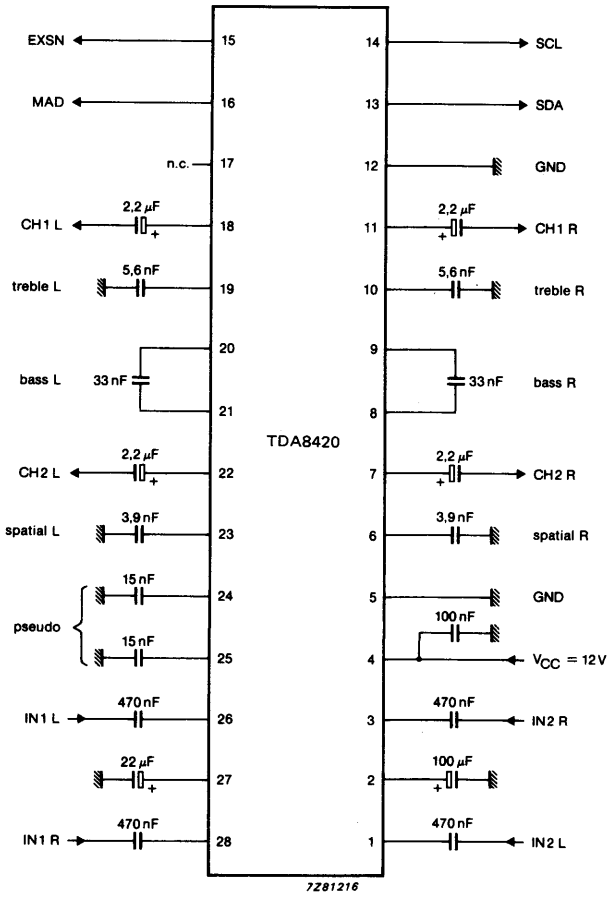
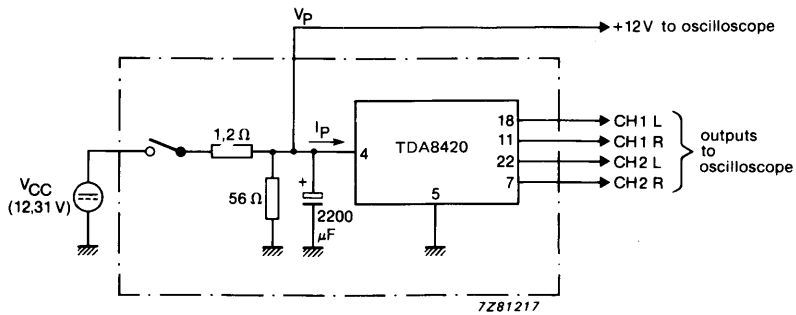


Fig. 16 Test and application circuit diagram.



I_{CC} = 45 mA;
I_{load} = 259 mA;
t_{on} = 2,64 ms;
t_{off} = 102 ms.

Fig. 17 Turn-on/off power supply circuit diagram.

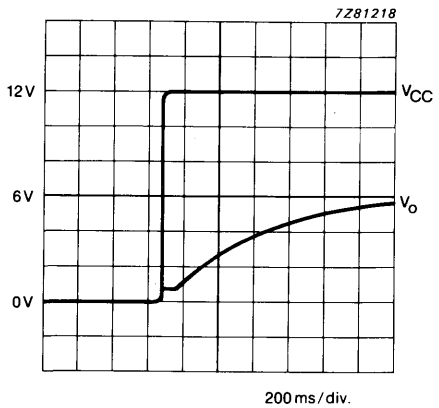


Fig. 18 Turn-on behaviour;
C = 2,2 µF; R_L = 10 kΩ.

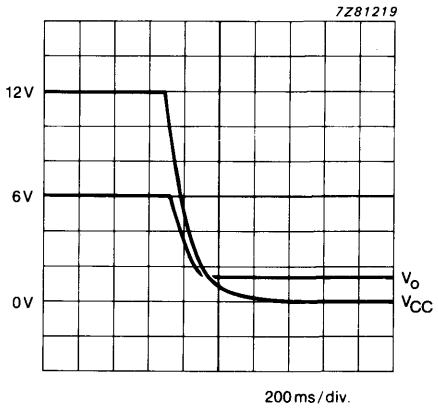


Fig. 19 Turn-off behaviour;
without modulation.

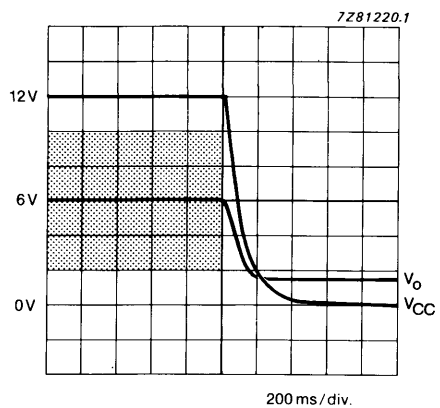


Fig. 20 Turn-off behaviour; with modulation (shaded area).

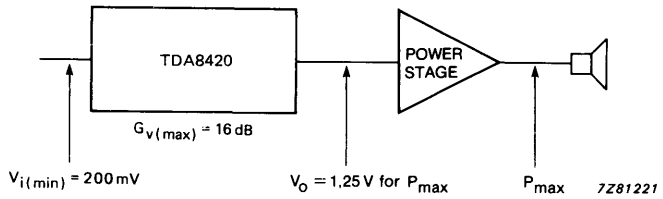


Fig. 21 Level diagram loudspeaker channel CH1 with $V_{i(min)}$ = 200 mV; V_o = 1,25 for P_{max}.

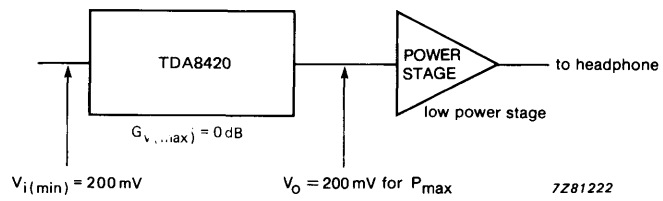


Fig. 22 Level diagram headphone channel CH2 with V_i = 200 mV; V_o = 200 mV for P_{max}.

HI-FI STEREO AUDIO PROCESSOR; I²C BUS

GENERAL DESCRIPTION

The TDA8421 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel (CH1) and a headphone channel (CH2), digital controlled via the I²C bus, for application in hi-fi audio and television sound.

Features

- Input selector
- Mode selector
- Loudspeaker channel (CH1) } with volume control, balance control and mute
- Headphone channel (CH2) }
- Pseudo stereo and spatial function
- Bass and treble control
- Electrostatic discharge protection diodes

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	200	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	90	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Channel separation	α	–	75	–	dB
Volume control range CH1	G	−62	–	16	dB
Treble control range	G	−12	–	12	dB
Bass control range	G	−12	–	15	dB
Volume control range CH2	G	−62	–	0	dB

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117).

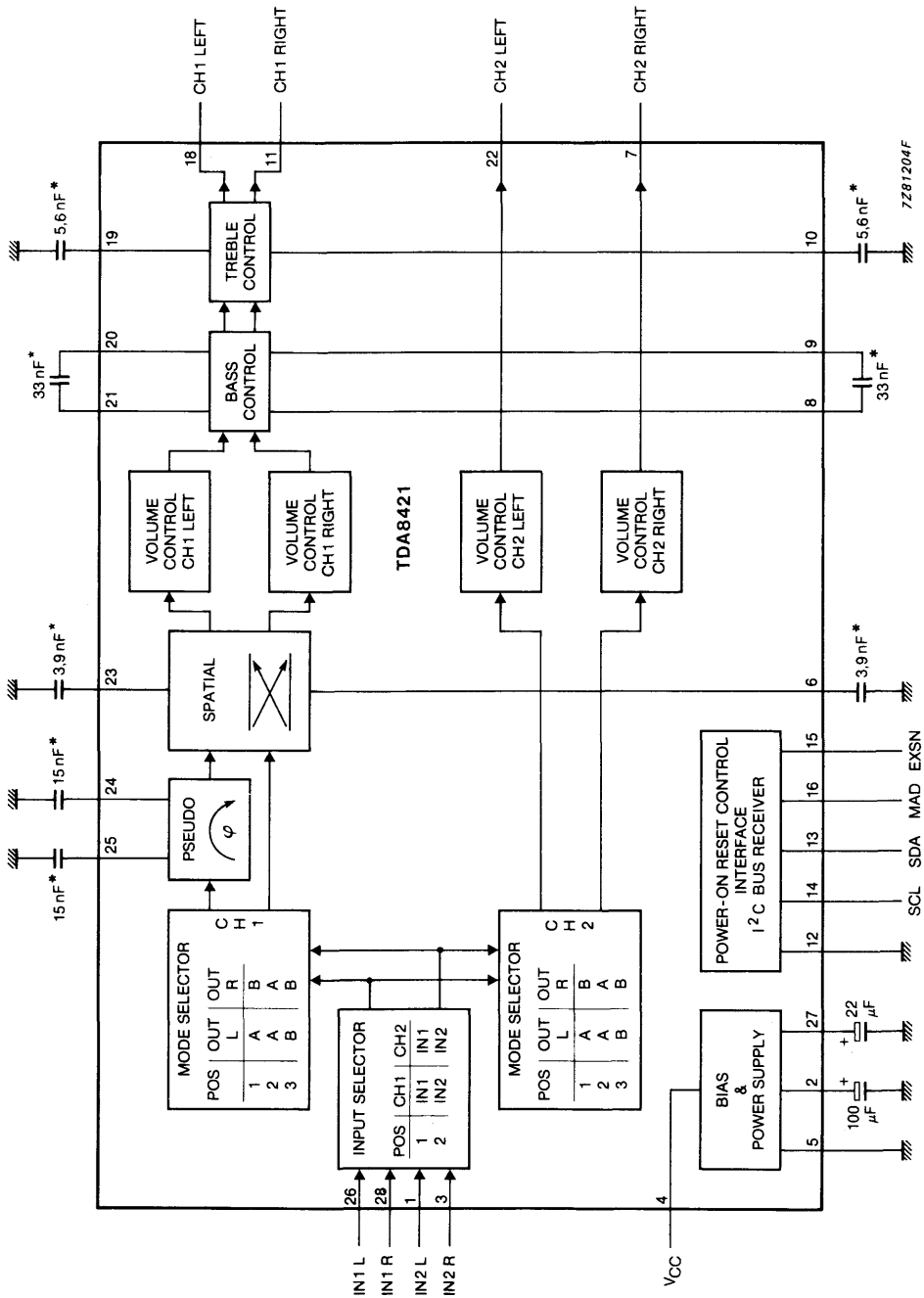


Fig. 1 Block diagram.

* These values are dependent on the required frequency response and effect.

PINNING

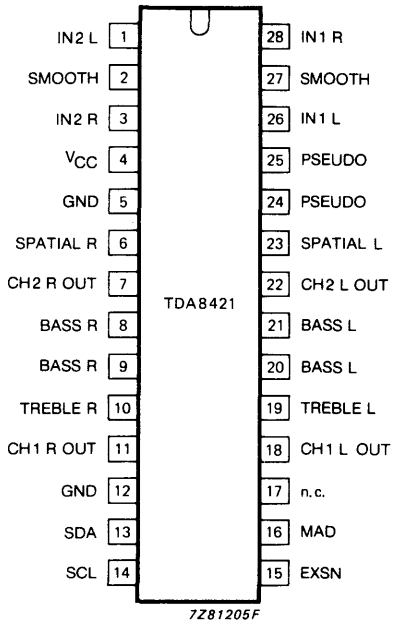


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Input selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the input selector. The selection is made from the following AF input signals:

- IN1 L (pin 26); IN1 R (pin 28)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Where IN1 is an internal input signal and IN2 an external input signal.

Mode selector

For each channel (CH1 and CH2) there is a mode selector which selects between stereo, sound A and sound B in the event of bilingual transmission. Both mode selectors can be controlled independently.

Headphone channel (CH2)

Volume control and balance

The stages for volume control for CH2 consist of two parts for left and right. In each part the gain can be adjusted between 0 and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Loudspeaker channel (CH1)

Volume control and balance

The loudspeaker channel (CH1) also consists of two parts for volume control (left and right). In each part the gain can be adjusted between + 16 dB and −62 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Stereo/pseudo stereo/spatial stereo mode

It is possible to select three modes. Stereo, pseudo or spatial stereo. The pseudo stereo mode receives mono transmissions and the stereo and spatial stereo mode receives stereo transmissions.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8421 includes a bias and power supply stage, which generates a voltage of ½ V_{CC} with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both the loudspeaker channel (CH1) and the headphone channel (CH2). The muting can be switched by transmission of the mute bit.

I^2C bus receiver and data handling

Bus specification

The TDA8421 is controlled via the 2-wire I^2C bus by a microcomputer. The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8421 starts with the module address MAD.

MSB								LSB
1	0	0	0	0	0	MAD	R/W	ACK

Fig. 3 TDA8421 module address.

The module address is determined by pin 16. When connected to ground MAD = 0; when connected to V_{CC} MAD = 1. Thus two TDA8421s can be selected within a system.

Subaddress

After the module address byte a second byte is used to select the functions for both channels:

- CH1 – Volume left, volume right, bass, treble and switch functions
- CH2 – Volume left, volume right and switch functions

The subaddress SAD is stored within the TDA8421. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

		128	64	32	16	8	4	2	1
	function	MSB 7	6	5	4	3	2	1	LSB 0
CH1	volume left	0	0	0	0	0	0	0	0
	volume right	0	0	0	0	0	0	0	1
	bass	0	0	0	0	0	0	1	0
	treble	0	0	0	0	0	0	1	1
	switch functions	0	0	0	0	1	0	0	0
CH2	volume left	0	0	0	0	0	1	0	0
	volume right	0	0	0	0	0	1	0	1
	switch functions	0	0	0	0	1	1	0	0
						subaddress SAD			

Definition of 3rd byte

A third byte is used to transmit data to the TDA8421. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

	function		MSB 7	6	5	4	3	2	1	LSB 0
CH1	volume left	VL1	1	1	V05	V04	V03	V02	V01	V00
	volume right	VR1	1	1	V15	V14	V13	V12	V11	V10
	bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
	treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
	switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS
CH2	volume left	VL2	1	1	V25	V24	V23	V22	V21	V20
	volume right	VR2	1	1	V35	V34	V33	V32	V31	V30
	switch functions	S2	1	1	1	1	EXS	MH1	MH0	1

Truth tables

Truth tables for the switch functions

Table 3 Input selector

function	IS
IN1	0
IN2	1

Table 4 Mode selectors

	CH1		CH2	
mode	ML0	ML1	MH0	MH1
stereo	1	1	1	1
sound A	1	0	1	0
sound B	0	1	0	1
----------	0	0	0	0

Table 5 Stereo/pseudo stereo/spatial stereo

choice	STL	EFL
spatial	1	1
stereo	1	0
pseudo	0	1
----------	0	0

Table 6 Mute

mute	MU
active; automatic after POR*	1
not active	0

Table 7 Output for external switch

EXSN	EXS
ground	1
open collector	0

Where: POR = Power-On Reset.

Truth tables for the volume base and treble controls.

Table 8 Volume control

CH1	CH2	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
16	0	1	1	1	1	1	1
14	−2	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
−46	−62	1	0	0	0	0	0
−48	⩽−90	0	1	1	1	1	1
.	.	.	.	.	.	.	.
−62	⩽−90	0	1	1	0	0	0
⩽−90	⩽−90	0	1	0	1	1	1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
⩽−90	⩽−90	0	0	0	0	0	0

Where: The values of CH1 and CH2 are in 2 dB/step measured in dBs.

* Attenuation ⩾ 90 dB

Table 9 Bass control

3dB/step (dB)	BA3	BA2	BA1	BA0
15	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
15	1	0	1	1
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Table 10 Treble control

3dB/step (dB)	TR3	TR2	TR1	TR0
12	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all eight functions have to be adjusted with eight data transmissions. It is recommended that data information for switch functions in CH1 are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 5. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

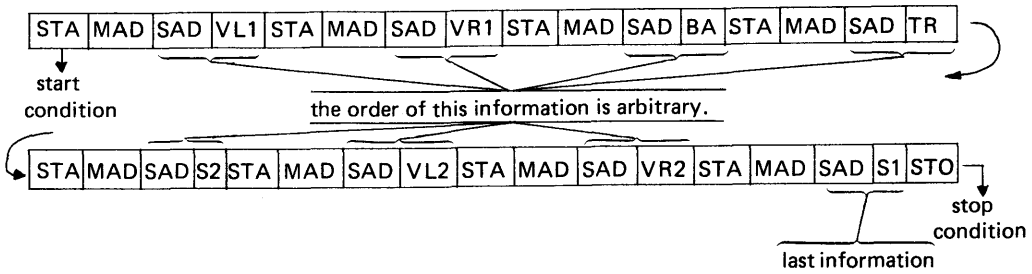


Fig. 4 Data transmission after a power-on reset.

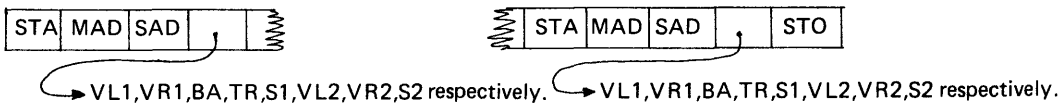


Fig. 5 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range at pins for external capacitors				
pins 2, 6, 8 to 10, 19 to 21, 23 to 25, 27	V_{cap}	0	V_{CC}	V
pin 13	V_{SDA}	0	V_{CC}	V
pin 14	V_{SCL}	0	V_{CC}	V
pin 15	V_{EXSN}	0	V_{CC}	V
pin 16	V_{MAD}	0	V_{CC}	V
Voltage range at pins 1, 3, 7, 11, 18, 22, 26, 28	V_I, V_O	0	V_{CC}	V
Output current at pins 7, 11, 18, 22	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70$ °C	P_{tot}	–	1350	mW
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	−25	150	°C
Electrostatic handling *	$\pm V_{ESD}$	–	2000	V

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ resistor.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Supply current at V_{CC} = 12 V	I_{CC}	–	42	55	mA
Internal input voltage IN1 L,R (pins 26,28) IN2 L,R (pins 1,3) DC voltage internally generated; capacitive coupling recommended	V_I	5,4	6,0	6,6	V
MAD (pin 16)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	0	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
SDA; SCL (pins 13 and 14)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	μA
input current LOW	I_{IL}	–	1	10	μA
Output voltage at CH1 (pins 11 and 18); CH2 (pins 7 and 22)	V_O	5,4	½ V_{CC}	6,6	V
pins with external capacitors					
pins 6 to 10; 19 to 21; 23 to 25	$V_{cap.n}$	–	½ V_{CC}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0,1	–	V
External switch (pin 15) at I_{EXSN} = 1 mA					
Output voltage HIGH	V_{EXSNH}	–	–	16	V
Output voltage LOW	V_{EXSNL}	–	–	0,3	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10\ k\Omega$; $C_L < 100\ pF$; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 6)					
SDA, SCL (pin 13 and 14)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0,3	μs
Set-up time for start condition	$t_{SU;STA}$	4,7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
Input signals					
IN1 L (pin 26) IN1 R (pin 28) IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (r.m.s. value) at V_u = –4 dB; THD ⩽ 0,5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_{n-5}	35	50	–	kΩ
Frequency response (–0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
LOUDSPEAKER CHANNEL OUTPUTS					
CH1 LEFT (pin 18); CH1 RIGHT (pin 11)					
Output voltage range (r.m.s. value) at THD $\leqslant$ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level weighted according to CCIR468-2					
gain = 16 dB	V_n	–	90	–	μV
gain = 0 dB	V_n	–	20	40	μV
gain = $\leqslant$ −90 dB	V_n	–	15	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,5 V; gain = + 16 dB to −30 dB	THD	–	0,05	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = + 2 dB to −30 dB	THD	–	0,07	0,2	%
for $V_{i(rms)}$ = 2,0 V; gain = −4 dB to −30 dB	THD	–	0,1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
VOLUME CONTROL					
For truth table see Table 8					

parameter	symbol	min.	typ.	max.	unit
Loudspeaker channel (CH1)					
Control range at f = 1 kHz					
maximum voltage gain (16 dB step)	G_{max}	15	–	–	dB
minimum voltage gain (–62 dB step)	G_{min}	–60	–	–	dB
last position	G_{off}	–80	–85	–	dB
mute position	G_{mute}	–85	–90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 16 dB to –30 dB	ΔG	–	–	0,5	dB
gain from –30 dB to –62 dB	ΔG	–	–	1	dB
TREBLE CONTROL (CH1)					
For truth table see Table 10					
Control range for $C_{10\text{-}5}$; $C_{19\text{-}5}$ = 5,6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
BASS CONTROL					
For truth table see Table 9					
Control range for $C_{8\text{-}9}$; $C_{20\text{-}21}$ = 33 nF					
Maximum emphasis at 40 kHz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial: Antiphase crosstalk	α	–	50	–	%
Pseudo: Phase shift (see Fig. 15)					

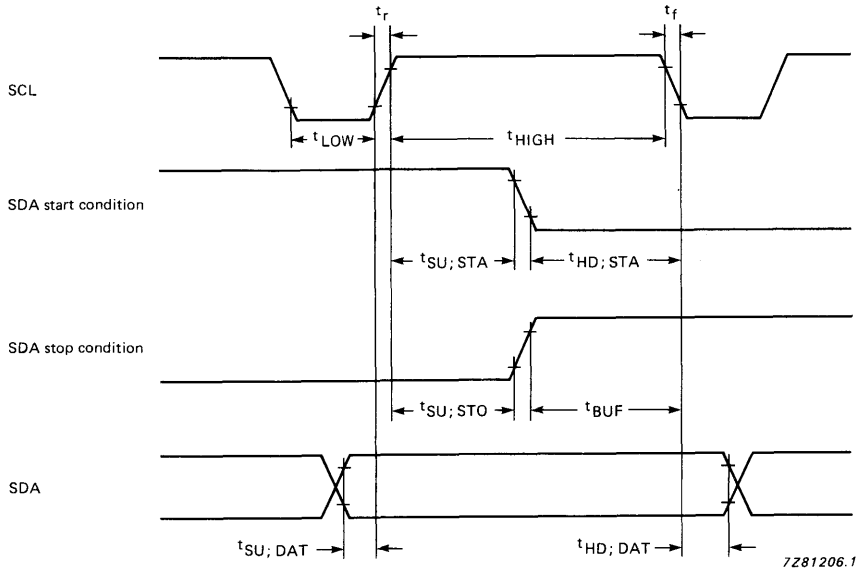
AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
HEADPHONE CHANNEL OUTPUTS					
CH2 LEFT (pin 22); CH2 RIGHT (pin 7)					
Output voltage range (r.m.s. value) at THD $\leqslant$ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level (weighted according to CCIR468-2)					
gain = 0 dB	V_n	–	15	–	μV
gain = 16 dB	V_n	–	12	25	μV
gain = $\leqslant$ −90 dB	V_n	–	10	–	μV
Total harmonic distortion (f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,2 V; gain = 0 dB to −30 dB	THD	–	0,01	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = 0 dB to −30 dB	THD	–	0,1	–	%
for $V_{i(rms)}$ = 2,0 V gain = −4 dB to −30 dB	THD	–	0,3	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
Crosstalk between any input/output f = 100 Hz to 12,5 kHz	α	65	70	–	dB
Crosstalk IN1/IN2 gain = 0 dB; R_G = 0	α	95	100	–	dB

parameter	symbol	min.	typ.	max.	unit
Headphone channel (CH2)					
Control range					
maximum voltage gain (0 dB step)	G_{max}	−1	–	–	dB
minimum voltage gain (−62 dB step)	G_{min}	−57	–	–	dB
last position	G_{off}	−80	−85	–	dB
mute position	G_{mute}	−85	−90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 0 dB to −40 dB	ΔG	–	–	0,5	dB
gain from −40 dB to −62 dB	ΔG	–	–	2	dB

Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels.



$t_{SU;STA}$ = start code set-up time
$t_{HD;STA}$ = start code hold time
$t_{SU;STO}$ = stop code set-up time
t_{BUF} = BUS free time
$t_{SU;DAT}$ = data set-up time
$t_{HD;DAT}$ = DATA hold time

Fig. 6 Timing requirements for I^2C bus.

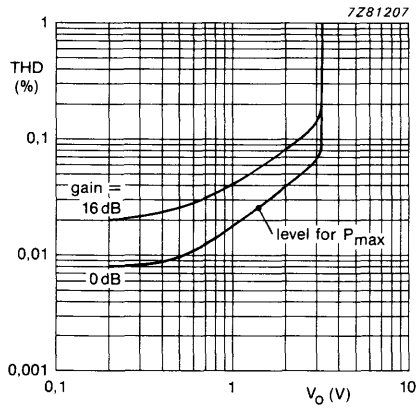


Fig. 7 Distortion loudspeaker channel CH1 as a function of the output voltage with gain as parameter.

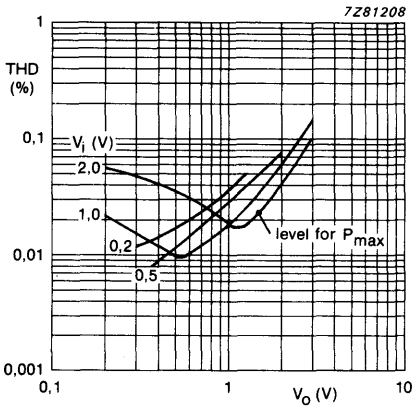


Fig. 8 Distortion loudspeaker channel CH1 as a function of the output voltage with input voltage as parameter.

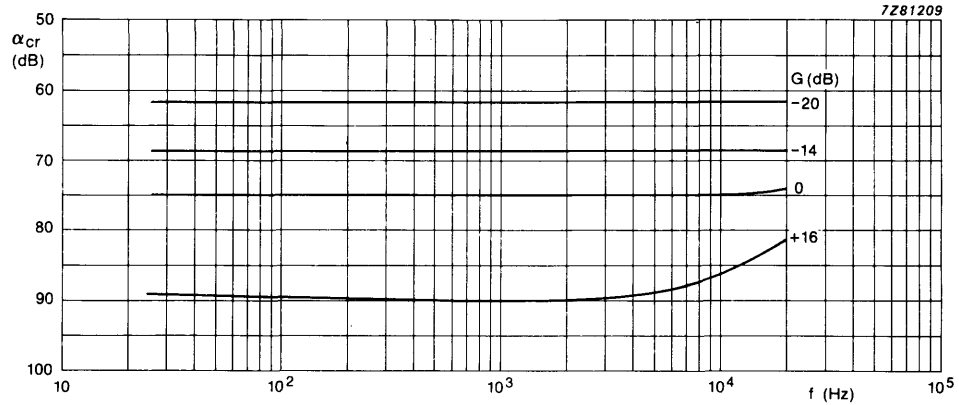


Fig. 9 Channel separation loudspeaker channel CH1 as a function of frequency.

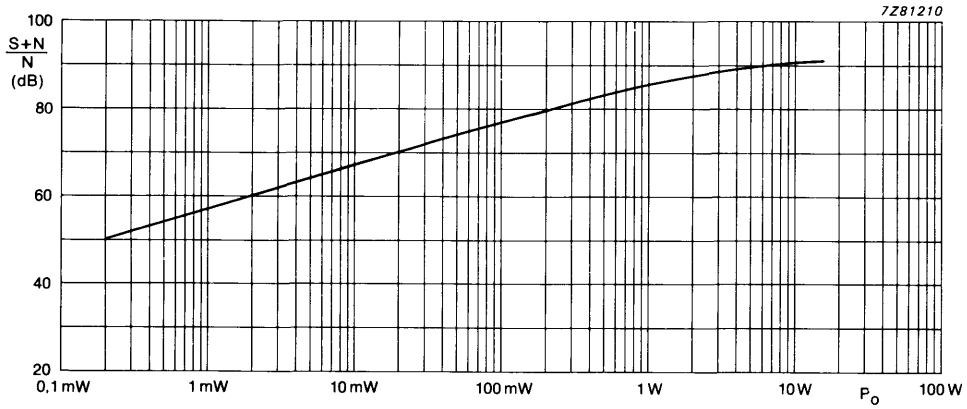


Fig. 10 Signal-to-noise ratio as a function of output power.
Input voltage V_i = 0,5 V; according to CCIR; quasi peak; P_o = 15 W.

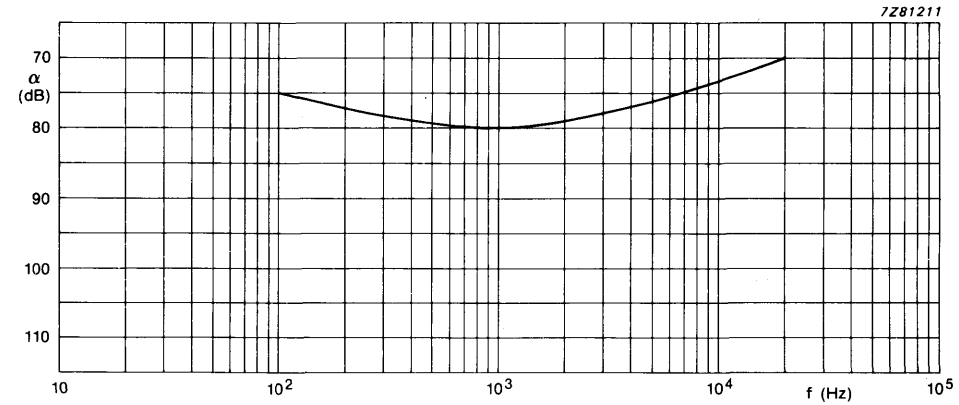


Fig. 11 Crosstalk 2-tone mode as a function of frequency.
CH1: mode AA, Gain + 16 dB; CH2: mode BB, Gain 0 dB. Signal input RIGHT; input LEFT to ground, measured at output CH1.

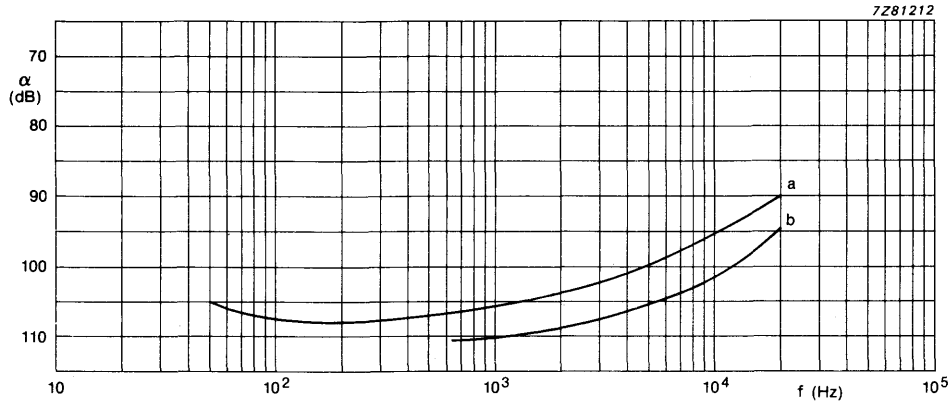


Fig. 12 Crosstalk between IN1 and IN2 as a function of frequency; measured at output CH1, $R_G = 0$.
a) Gain = + 16 dB; V_i = 200 mV. b) Gain = 0 dB; V_i = 1 V.

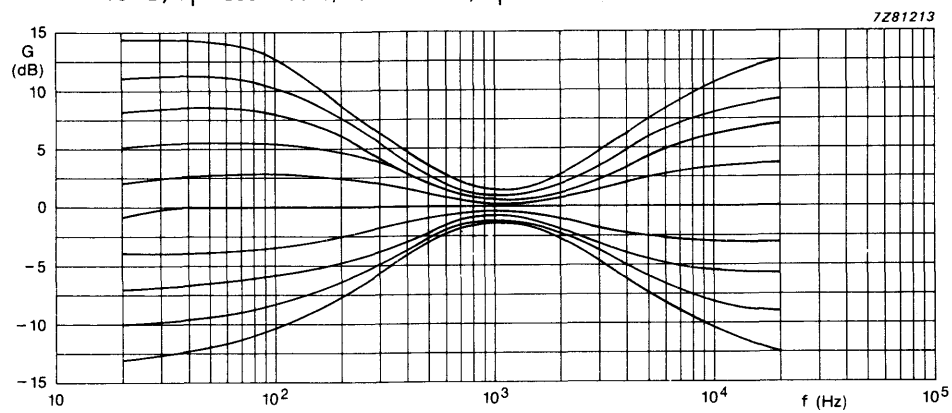


Fig. 13 Bass and treble tone control. C_{bass} = 33 nF, C_{treble} = 5,6 nF.

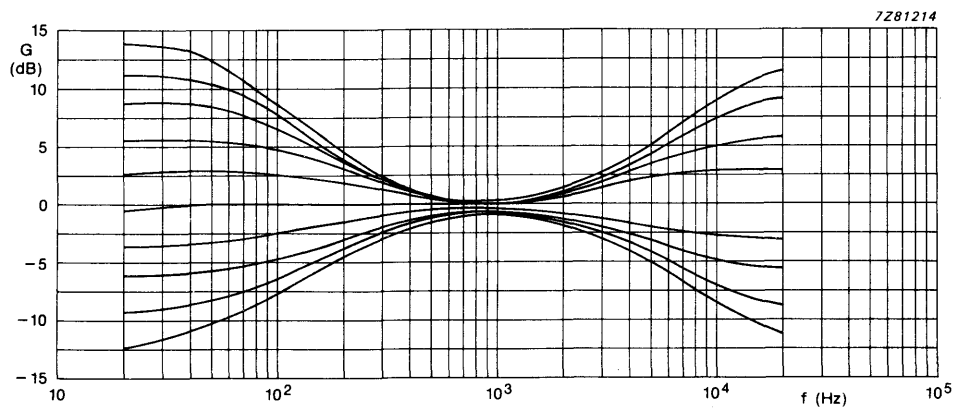
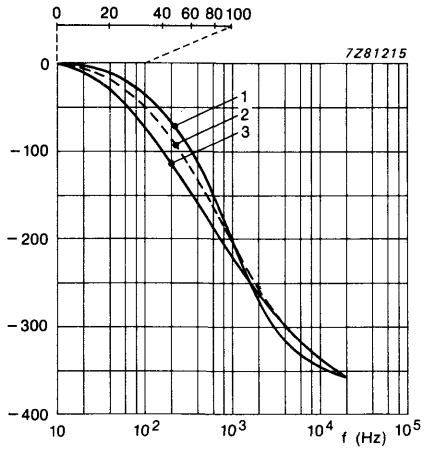


Fig. 14 Bass and treble tone control. C_{bass} = 68 nF, C_{treble} = 3,9 nF.



curve	pin 24 (nF)	pin (nF)	effect
1	15	15	normal
2	5,6	47	intensified
3	5,6	68	more intensified

Fig. 15 Pseudo (phase) as a function of frequency CH1 left.

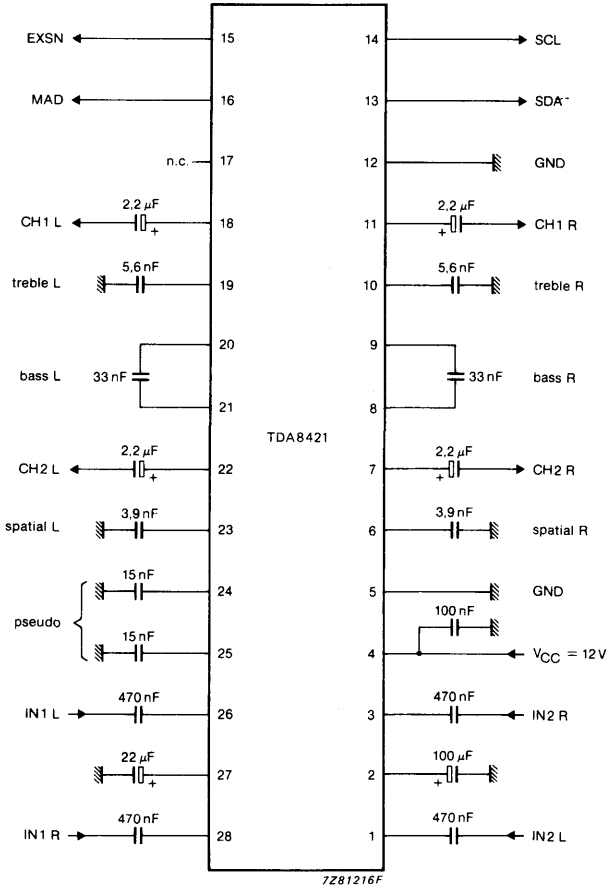
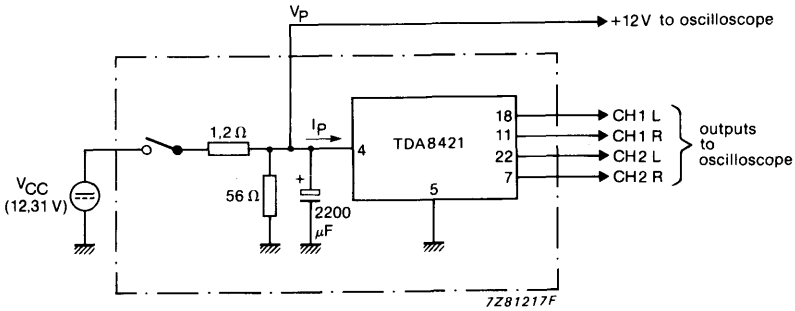


Fig. 16 Test and application circuit diagram.



I_{CC} = 45 mA;
I_{load} = 259 mA;
t_{on} = 2,64 ms;
t_{off} = 102 ms.

Fig. 17 Turn-on/off power supply circuit diagram.

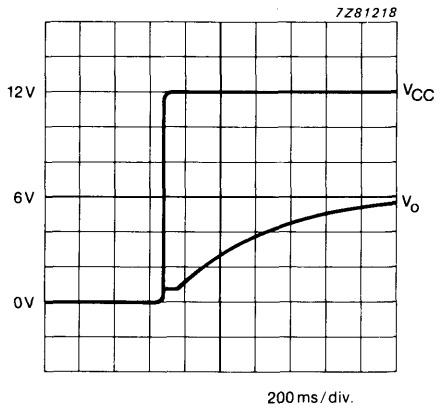


Fig. 18 Turn-on behaviour;
C = 2,2 μF; R_L = 10 kΩ.

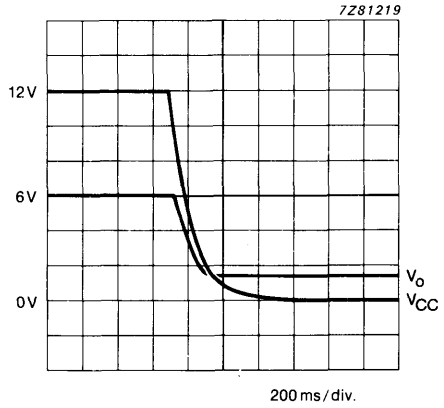


Fig. 19 Turn-off behaviour;
without modulation.

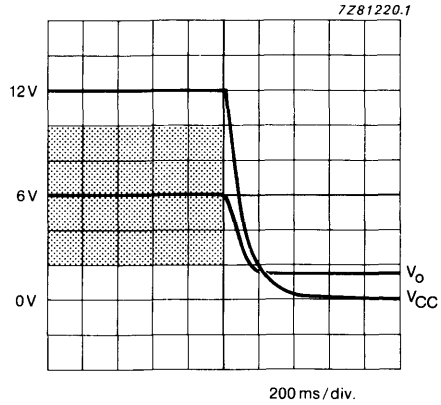


Fig. 20 Turn-off behaviour; with modulation (shaded area).

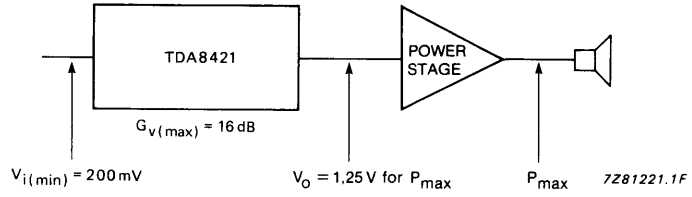


Fig. 21 Level diagram loudspeaker channel CH1 with $V_{i(min)}$ = 200 mV; V_o = 1,25 for P_{max}.

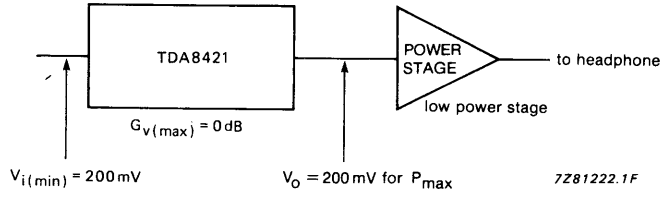


Fig. 22 Level diagram headphone channel CH2 with V_i = 200 mV; V_o = 200 mV for P_{max}.

HI-FI STEREO AUDIO PROCESSOR; I²C-BUS

GENERAL DESCRIPTION

The TDA8425 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel facility, digitally controlled via the I²C-bus for application in hi-fi audio and television sound.

Features

- Source and mode selector for two stereo channels
- Pseudo stereo, spatial stereo, linear stereo and forced mono switch
- Volume and balance control
- Bass, treble and mute control
- Power supply with power-on reset

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{CC}	10.8	12.0	13.2	V
Input signal handling	V_I	2	–	–	V
Input sensitivity full power at the output stage	V_i	–	300	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	86	–	dB
Total harmonic distortion	THD	–	0.05	–	%
Channel separation	α	–	80	–	dB
Volume control range	G	−64	–	6	dB
Treble control range	G	−12	–	12	dB
Bass control range	G	−12	–	15	dB

PACKAGE OUTLINE

20-lead dual in-line; plastic (SOT146).

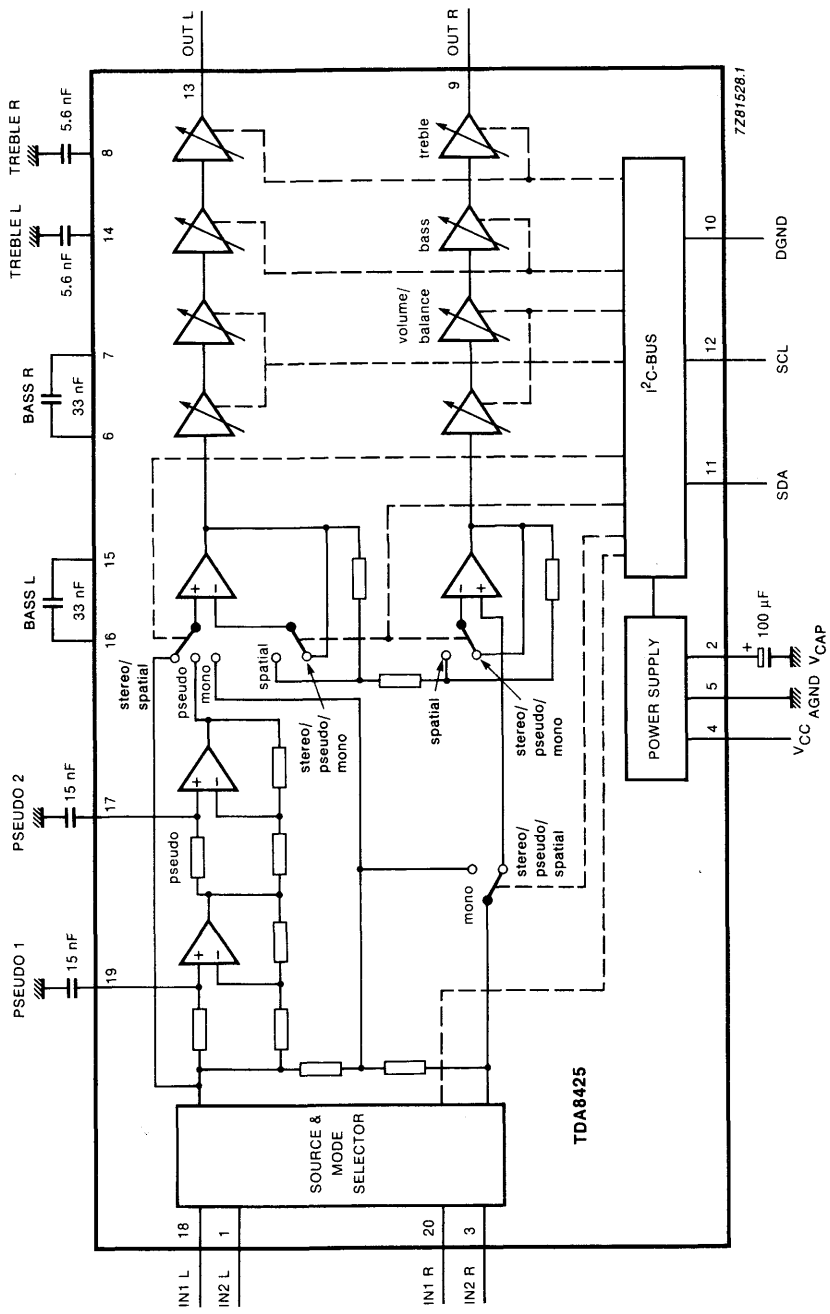


Fig. 1 Block diagram.

PINNING

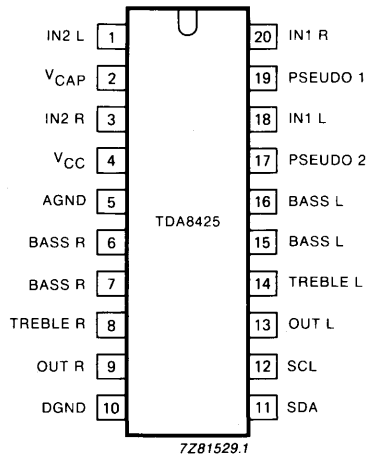


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Source selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the source selector. The selection is made from the following AF input signals:

- IN1 L (pin 18); IN1 R (pin 20)
  or
- IN2 L (pin 1); IN2 R (pin 3)

Mode selector

The mode selector selects between stereo, sound A and sound B (in the event of bilingual transmission) for OUT R and OUT L.

Volume control and balance

The volume control consists of two stages (left and right). In each part the gain can be adjusted between +6 dB and −64 dB in steps of 2 dB. An additional step allows an attenuation of $\geqslant$ 80 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right output channels.

Linear stereo, pseudo stereo, spatial stereo and forced mono mode*

It is possible to select four modes: linear stereo, pseudo stereo, spatial stereo or forced mono. The pseudo stereo mode handles mono transmissions, the spatial stereo mode handles stereo transmissions and the forced mono can be used in the event of stereo signals.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

* During forced mono mode the pseudo stereo mode cannot be used.

Treble control

The treble control stage can be switched from + 12 dB to −12 dB in steps of 3 dB.

Bias and power supply

The TDA8425 includes a bias and power supply stage, which generates a voltage of $0.5 \times V_{CC}$ with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both parts of the treble amplifier. The muting can be switched by transmission of the mute bit.

I²C-bus receiver and data handling

Bus specification

The TDA8425 is controlled via the 2-wire I²C-bus by a microcomputer.
The two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH.
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition.
A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition.
The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition.
The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8425 starts with the module address MAD.

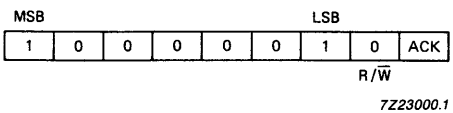


Fig. 3 TDA8425 module address.

Subaddress

After the module address byte a second byte is used to select the following functions:

- Volume left, volume right, bass, treble and switch functions

The subaddress SAD is stored within the TDA8425. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

	128	64	32	16	8	4	2	1
	MSB							LSB
function	7	6	5	4	3	2	1	0
volume left	0	0	0	0	0	0	0	0
volume right	0	0	0	0	0	0	0	1
bass	0	0	0	0	0	0	1	0
treble	0	0	0	0	0	0	1	1
switch functions	0	0	0	0	1	0	0	0
					subaddress SAD			

The automatic increment feature of the slave address enables a quick slave receiver initialization, within one transmission, by the I²C-bus controller (see Fig. 5).

Definition of 3rd byte

A third byte is used to transmit data to the TDA8425. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

function		MSB 7	6	5	4	3	2	1	LSB 0
volume left	VL	1	1	V05	V04	V03	V02	V01	V00
volume right	VR	1	1	V15	V14	V13	V12	V11	V10
bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS

DEVELOPMENT DATA

Truth tables

Truth tables for the switch functions

Table 3 Source selector

function	ML1	ML0	IS	channel
stereo	1	1	0	1
stereo	1	1	1	2
sound A	0	1	0	1
sound B	1	0	0	1
sound A	0	1	1	2
sound B	1	0	1	2

Table 4 Pseudo stereo/spatial stereo/linear stereo/forced mono

choice	STL	EFL
spatial stereo	1	1
linear stereo	1	0
pseudo stereo	0	1
forced mono*	0	0

Table 5 Mute

mute	MU
active; automatic after POR	1
not active	0

Where: POR = Power-ON Reset.

Truth tables for the volume, bass and treble controls

Table 6 Volume control

2 dB/step (dB)	V x 5	V x 4	V x 3	V x 2	V x 1	V x 0
6	1	1	1	1	1	1
4	1	1	1	1	1	0
−62	0	1	1	1	0	1
−64	0	1	1	1	0	0
⩽ −80	0	1	1	0	1	1
⩽ −80	0	0	0	0	0	0

* Pseudo stereo function is not possible in this mode.

DEVELOPMENT DATA

Table 7 Bass control

3 dB/step (dB)	BA3	BA2	BA2	BA0
15	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
15	1	0	1	1
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Table 8 Treble control

3 dB/step (dB)	TR3	TR2	TR2	TR0
12	1	1	1	1
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
12	1	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
0	0	1	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	1	0
..	..	..	..	..
..	..	..	..	..
..	..	..	..	..
−12	0	0	0	0

Sequence of data transmission

After a power-on reset all five functions have to be adjusted with five data transmissions. It is recommended that data information for switch functions are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 6. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

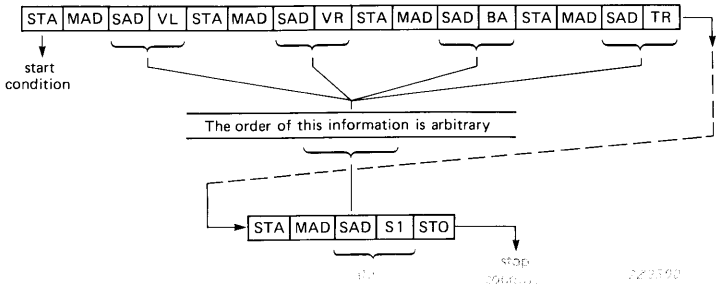


Fig. 4 Data transmission after a power-on reset.

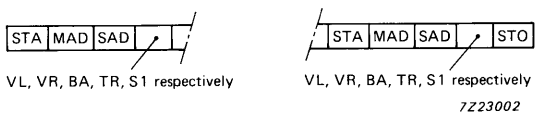


Fig. 5 Data transmission after a power-on reset with auto increment.

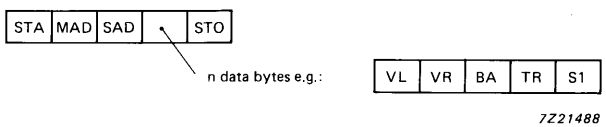


Fig. 6 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	0	16	V
Voltage range for pins with external capacitors	V_{cap}	0	V_{CC}	V
Voltage range for pins 11 and 12	$V_{SDA, SCL}$	0	V_{CC}	V
Voltage range at pins 1, 3, 9, 11, 12, 13, 18 and 20	$V_{I/O}$	0	V_{CC}	V
Output current at pins 9 and 13	I_O	–	45	mA
Total power dissipation at $T_{amb} < 70$ °C	P_{tot}	–	450	mW
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	−25	+ 150	°C
Electrostatic handling, classification A*				

DEVELOPMENT DATA

* Human body model: C = 100 pF, R = 1.5 kΩ and V ⩾ 4 kV; charge device model: C = 200 pF, R = 0 Ω and V ⩾ 500 V.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	10.8	12.0	13.2	V
Supply current at V_{CC} = 12 V	I_{CC}	–	26	35	mA
Internal reference voltage	V_{ref}	5.4	0.5 x V_{CC}	6.6	V
Internal voltage at pins 1, 3, 18 and 20 DC voltage internally generated; capacitive coupling recommended	V_I	–	V_{REF}	–	V
Internal voltage at pins 9 and 13	V_O	–	V_{REF}	–	V
SDA; SCL (pins 11 and 12)					
input voltage HIGH	V_{IH}	3.0	–	V_{CC}	V
input voltage LOW	V_{IL}	−0.3	–	1.5	V
input current HIGH	I_{IH}	–	–	+ 10	μA
input current LOW	I_{IL}	−10	–	–	μA
Output voltage at pins with external capacitors					
pins 6 to 8, 14 to 17, 19	$V_{cap.n}$	–	V_{REF}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}−0.3	–	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; $R_L > 10$ kΩ; $C_L < 1000$ pF; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I²C bus timing (see Fig. 7)					
SDA, SCL (pin 11 and 12)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
The LOW period of the clock	t_{LOW}	4.7	–	–	μs
SCL rise time	t_r	–	–	1	μs
SCL fall time	t_f	–	–	0.3	μs
Set-up time for start condition	$t_{SU;STA}$	4.7	–	–	μs
Hold time for start condition	$t_{HD;STA}$	4	–	–	μs
Set-up time for stop condition	$t_{SU;STO}$	4.7	–	–	μs
Time bus must be free before a new transmission can start	t_{BUF}	4.7	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
INPUTS					
IN1 L (pin 18) IN1 R (pin 20); IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (RMS value) at V_u = −12 dB; THD ≤ 0.5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_i	20	30	40	kΩ
Frequency response (−0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz
OUTPUTS					
OUT R (pin 9); OUT L (pin 13)					
Output voltage range (rms value) at THD ≤ 0.7%; $V_{i(max)} \leq 2$ V	$V_{o(rms)}$	0.6	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Signal plus noise-to-noise ratio (weighted according to CCIR 468-2); V_o = 600 mV					
gain = 6 dB	(S+N)/N	–	78	–	dB
gain = 0 dB	(S+N)/N	–	86	–	dB
gain = ≤ −20 dB	(S+N)/N	–	68	–	dB

DEVELOPMENT DATA

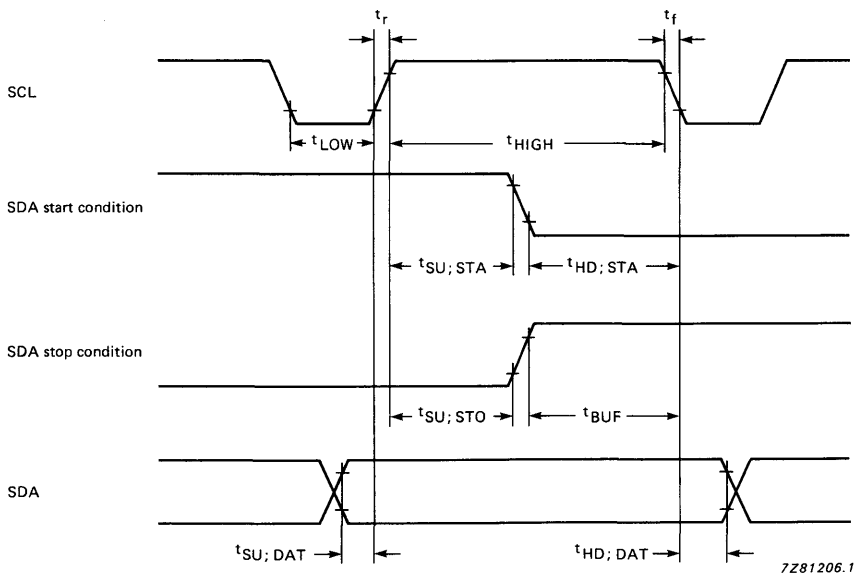
AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS (continued)					
Crosstalk between inputs at gain = 0 dB; 1 kHz; opposite inputs grounded (50 Ω); IN1L (pin 18) to IN2L (pin 1) or IN1R (pin 20) to IN2R (pin 3)	α_{cr}	–	100	–	dB
Total harmonic distortion (f = 20 Hz to 12.5 kHz)					
for $V_{i(rms)}$ = 0.3 V; gain = + 6 dB to −40 dB	THD	–	0.05	–	%
for $V_{i(rms)}$ = 0.6 V; gain = 0 dB to −40 dB	THD	–	0.07	0.4	%
for $V_{i(rms)}$ = 2.0 V; gain = −12 dB to −40 dB	THD	–	0.1	–	%
Channel separation at 10 kHz gain = 0 dB	α_{cs}	–	80	–	dB
Ripple rejection (gain = 0 dB; bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	100	–	dB
VOLUME CONTROL					
For truth table see Table 6					
Control range at f = 1 kHz (36 steps)					
maximum voltage gain (6 dB step)	G_{max}	5	6	–	dB
minimum voltage gain (−64 dB step)	G_{min}	−63	−64	–	dB
mute position	G_{mute}	−80	−90	–	dB
Gain tracking error; balance in mid-position	G	–	–	2	dB
Step resolution					
gain from 6 dB to −40 dB	G_{step}	1.5	2.0	2.5	dB/step
gain from −42 dB to −64 dB	G_{step}	1.0	2.0	3.0	dB/step
TREBLE CONTROL					
For truth table see Table 8					
Control range for $C_{8\text{-}5}$; $C_{14\text{-}5}$ = 5.6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step

parameter	symbol	min.	typ.	max.	unit
BASS CONTROL					
For truth table see Table 7					
Control range for C_{6-7}; C_{15-16} = 33 nF					
Maximum emphasis at 40 Hz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 Hz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	2.5	3.0	3.5	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial: Antiphase crosstalk	α	–	52	–	%
Pseudo: Phase shift (see Fig. 8)					

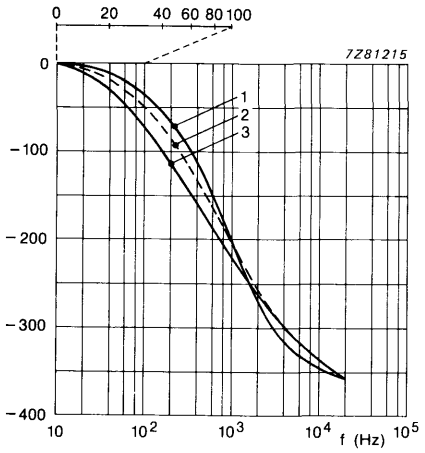
Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels (left and right).



$t_{SU;STA}$ = start code set-up time.
$t_{HD;STA}$ = start code hold time.
$t_{SU;STO}$ = stop code set-up time.
t_{BUF} = bus free time.
$t_{SU;DAT}$ = data set-up time.
$t_{HD;DAT}$ = data hold time.

Fig. 7 Timing requirements for I²C-bus.



curve	pin 17 (nF)	pin 19 (nF)	effect
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified

Fig. 8 Pseudo (phase in degrees) as a function of frequency (left output).

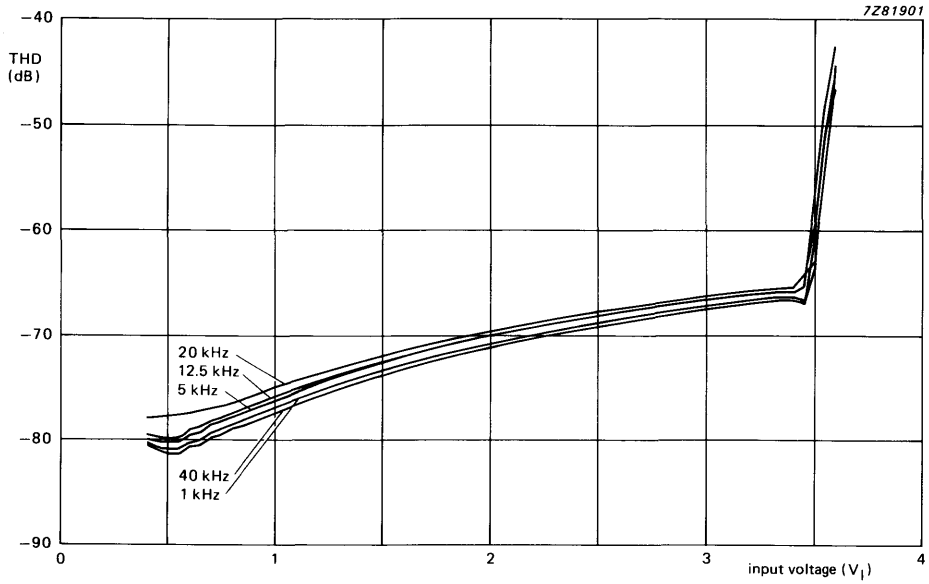


Fig. 9 Input signal handling capability; gain = −10 dB; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

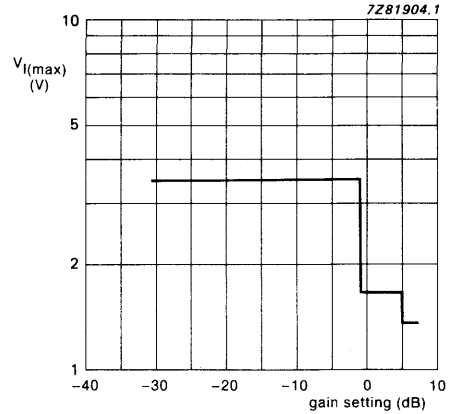


Fig. 10 Input signal handling capacility plotted against gain setting; THD = −60 dB; f = 1 kHz; R_S = 600 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

DEVELOPMENT DATA

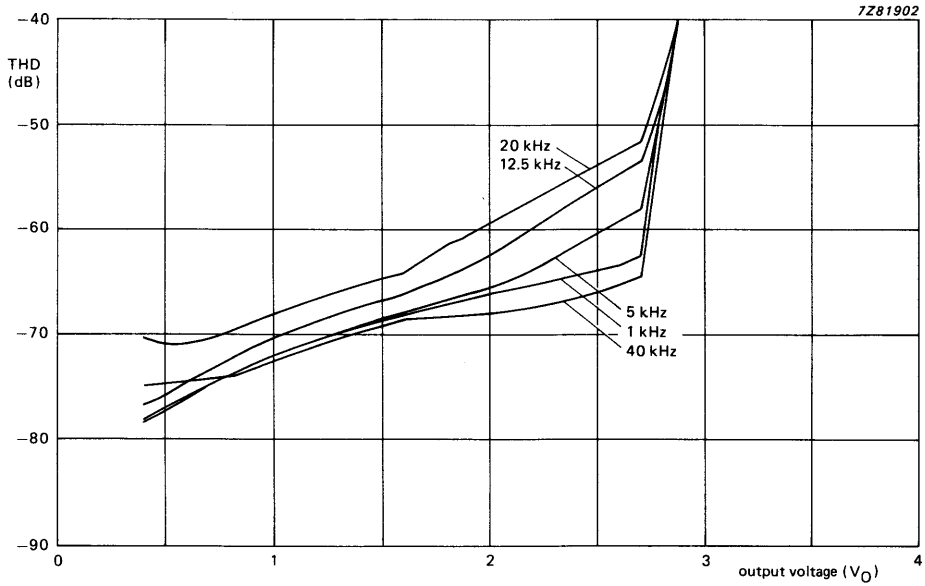


Fig. 11 Output signal handling capability; gain = 6 dB; R_S = 600 Ω, R_L = 10 kΩ, bass/trebble = 0 dB, V_{CC} = 12 V.

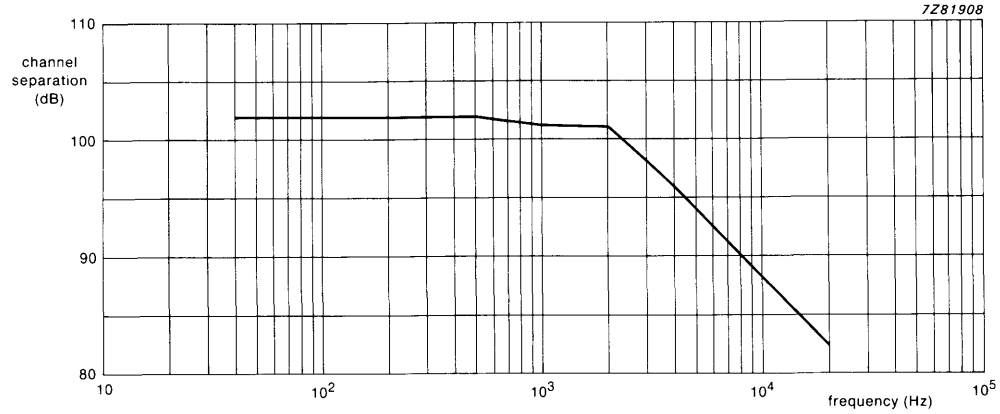
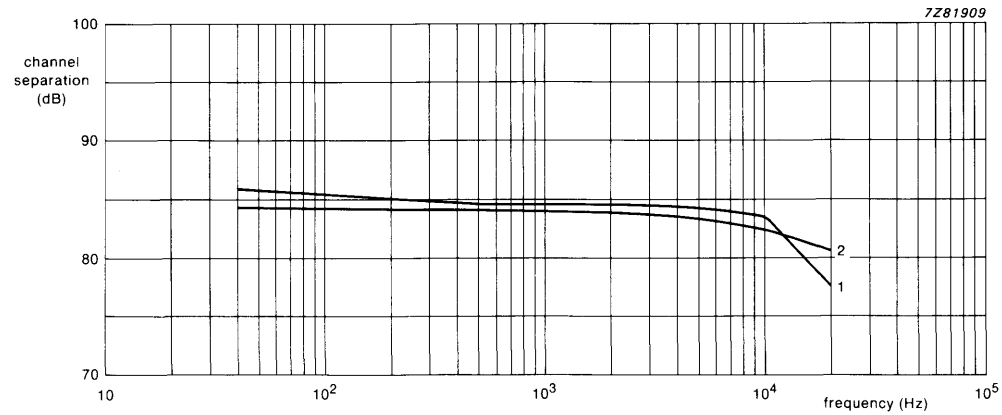


Fig. 12 Source selector separation (channel 2 and channel 1); gain = 0 dB; V_{i1} = 0 V; V_{i2} = 1 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.



(1) gain = 0 dB; V_i = 1.0 V.
(2) gain = 6 dB; V_i = 0.5 V.

Fig. 13 Stereo channel separation as a function of frequency; R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

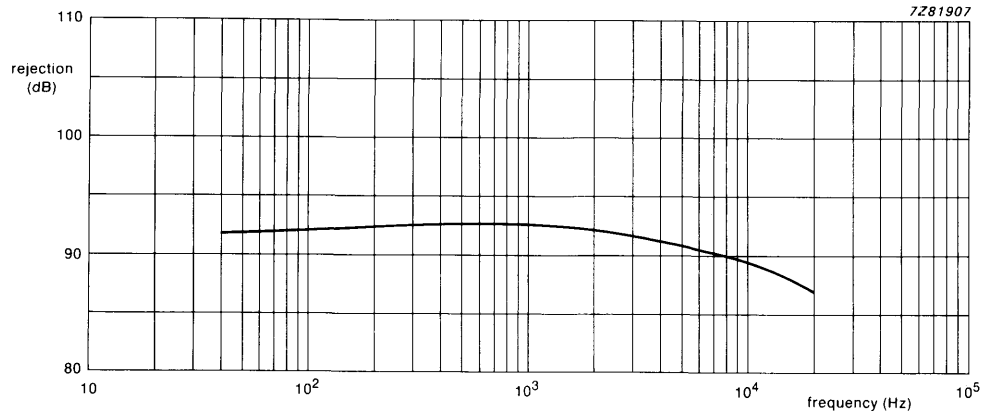


Fig. 14 Mute signal rejection as a function of frequency; gain = 0 dB; V_i = 1.0 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

DEVELOPMENT DATA

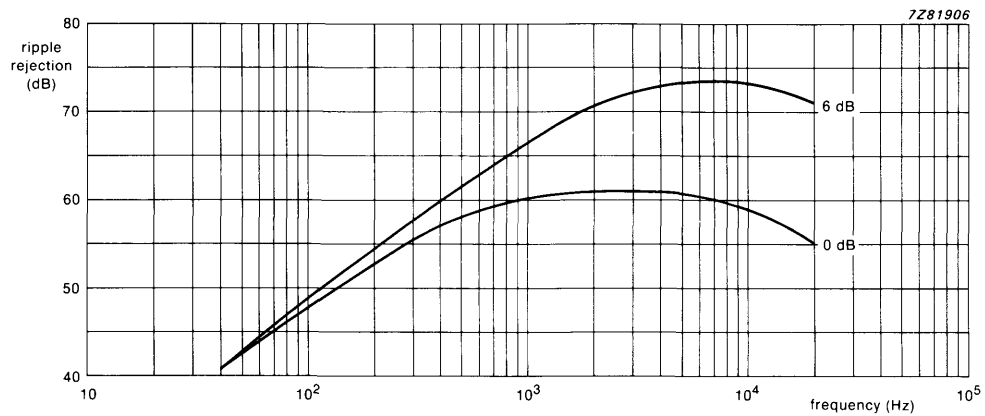


Fig. 15 Ripple rejection as a function of frequency; voltage ripple = 0.3 V (rms); R_S = 0 Ω, R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

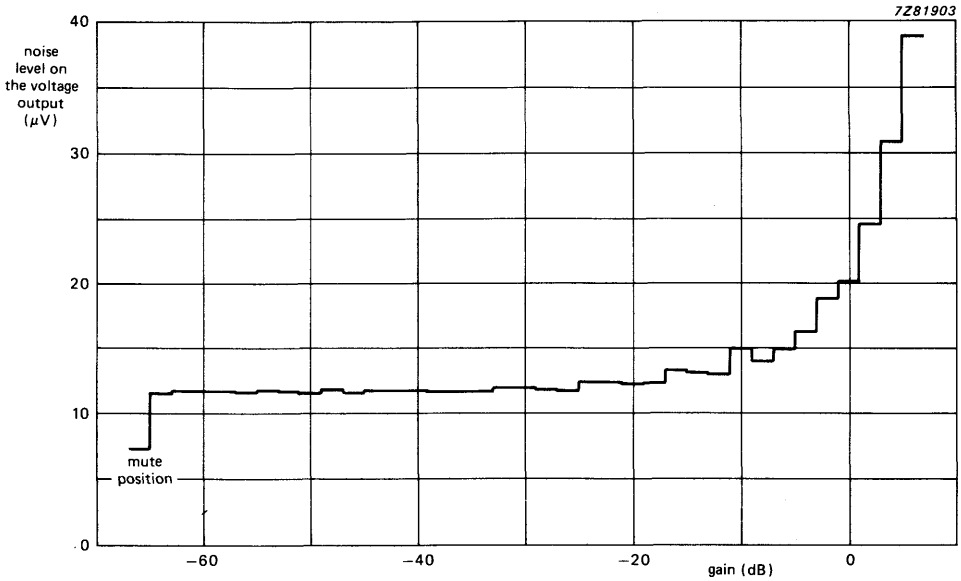


Fig. 16 Noise output voltage as a function of gain; weighted CCIR468 quasi peak gain, + 6 dB to −64 dB; V_i = 0 V, R_S = 0 Ω; R_L = 10 kΩ; bass/trebble = 0 dB; V_{CC} = 12 V.

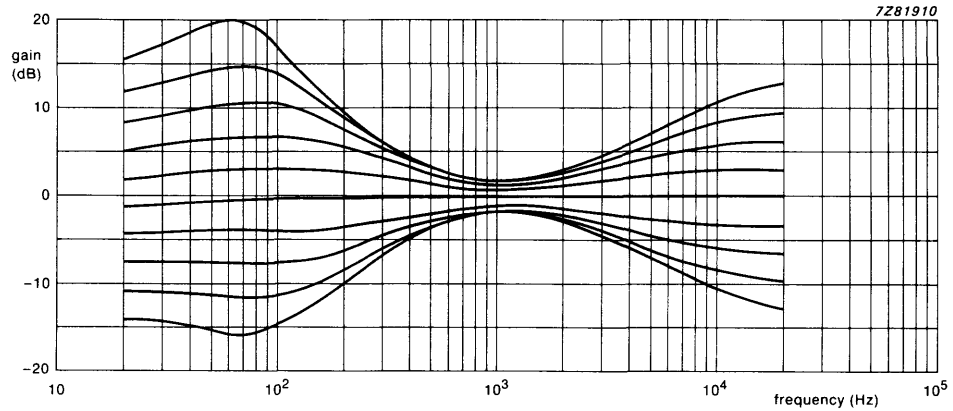


Fig. 17 Frequency response of bass and trebble control; bass and trebble gain settings = −12 to + 15 dB; gain is 0 dB; V_i = 0.1 V; R_{S9} = 600 Ω; R_L = 10 kΩ; V_{CC} = 12 V.

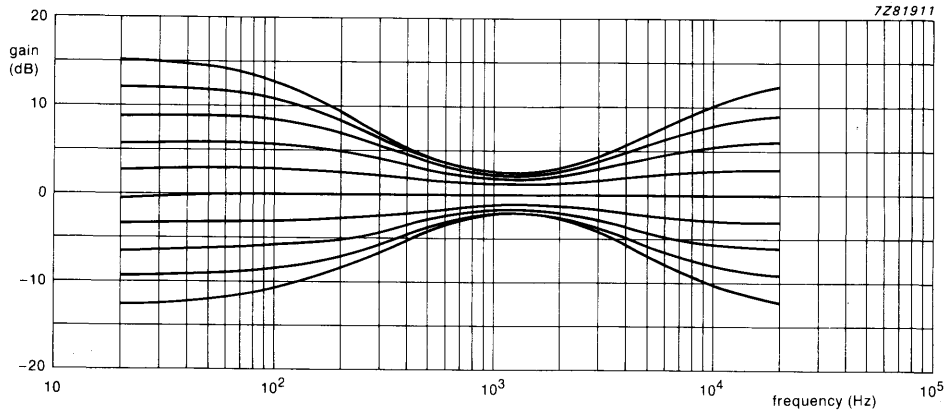


Fig. 18 Tone control with T-filter.

DEVELOPMENT DATA

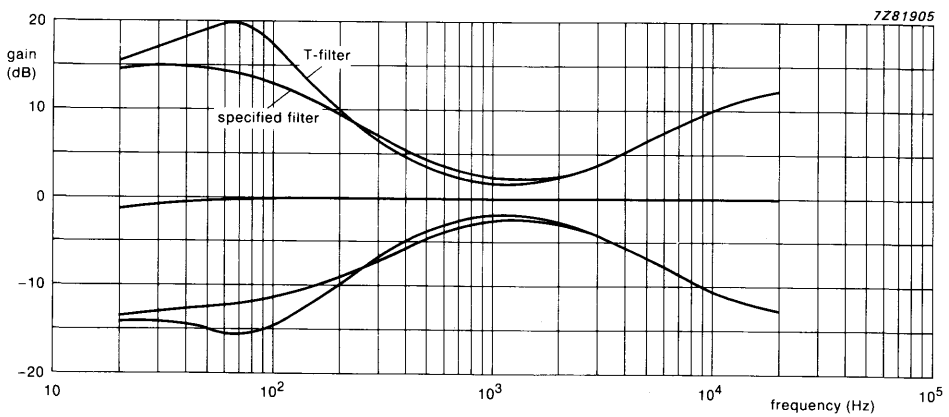


Fig. 19 Tone control.

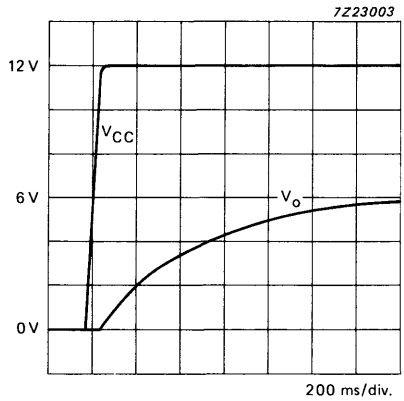


Fig. 20 Turn-on behaviour;
C = 2.2 μF; R_L = 10 kΩ.

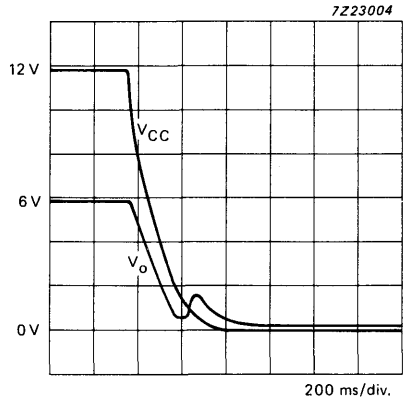


Fig. 21 Turn-off behaviour;
without modulation.

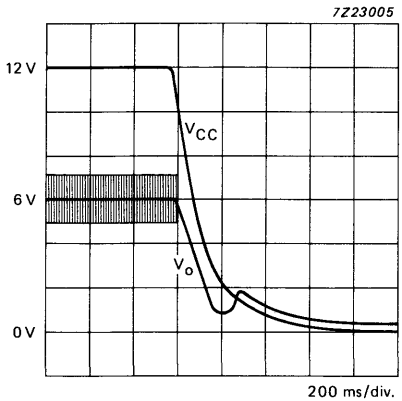
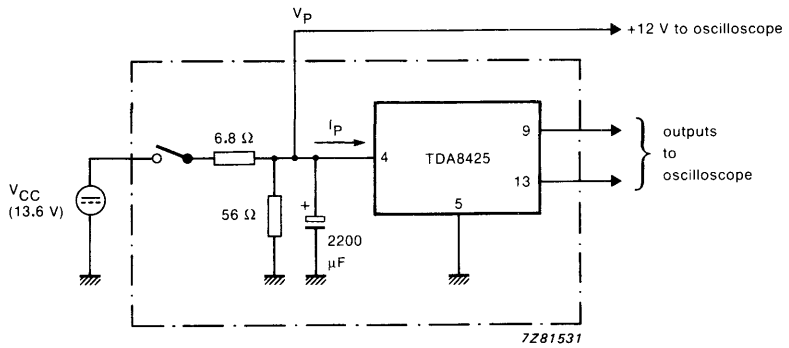


Fig. 22 Turn-off behaviour; with modulation (shaded area).



I_{CC} = 25 mA
I_{load} = 239 mA
t_{on} = 15 ms
t_{off} = 110 ms

Fig. 23 Turn-on/off power supply circuit diagram.

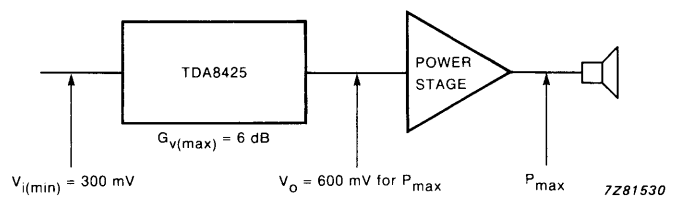


Fig. 24 Level diagram.

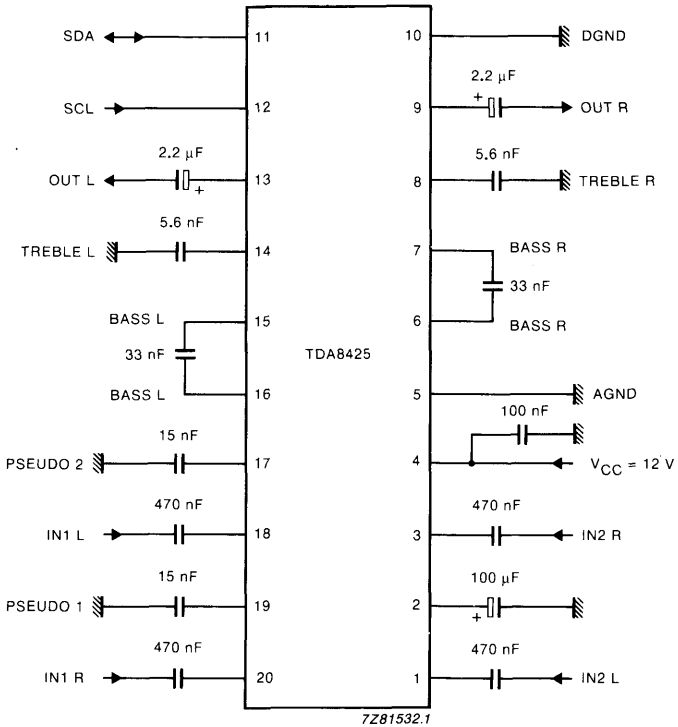


Fig. 25 Test and application circuit diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

OCTUPLE 6-BIT DAC WITH I²C-BUS

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input	V_P = 12 V	V_{max}	1	–	10.5	V
DAC output voltage range		V_O	0.1	–	V_P–0.5	V
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

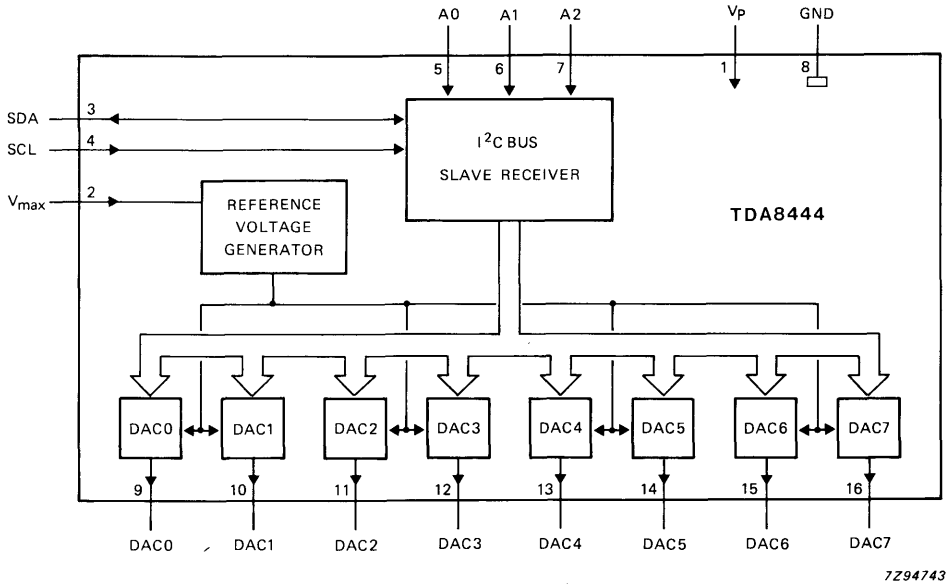


Fig. 1 Block diagram.

PINNING

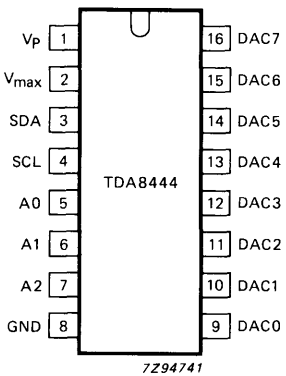


Fig. 2 Pinning diagram.

1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I^2C-bus serial data input/output
4	SCL	I^2C-bus serial data clock
5	A0	programmable address bits for I^2C-bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

FUNCTIONAL DESCRIPTION

I²C-bus

The TDA8444 I²C-bus interface is a receive-only slave. Data is accepted from the I²C-bus in the following format:

S	0 1 0 0 A2 A1 A0 0	A	I3 I2 I1 I0 SD SC SB SA	A	X X D5 D4 D3 D2 D1 D0	A	P
	← address byte →		← instruction byte →		← first data byte →		

Where:

S	= start condition	A2, A1, A0	= pfogrammable address bits
P	= stop condition	I3, I2, I1, I0	= instruction bits
A	= acknowledge	SD, SC, SB, SA	= subaddress bits
X	= don't care	D5, D4, D3, D2, D1, D0	= data bits

Fig. 3 Data format.

Address byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E (hexadec), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight TDA8444 ICs can be operated independently from one I²C-bus. No other addresses are acknowledged by the TDA8444.

Instruction and data bytes

Valid instructions are 00 to 0F and F0 to FF (hexadec); the TDA8444 will not respond to other instruction values.

Instructions 00 to 0F cause auto-incrementing of the subaddress (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addressed by bits SD to SA and then the subaddress is automatically incremented by one position for the next data byte in the series.

Auto-incrementation does not occur with instructions F0 to FF. Other than auto-incrementation there is no difference between instructions 00 to 0F and F0 to FF. When only one data byte per transmission is present, the DAC addressed by the subaddress will always receive the data.

Valid subaddresses (bits SD to SA) are 0 to 7 (hexadec) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the subaddress will sequence through all possible values (0 to F, 0 to F, etc.).

I²C-bus

Input SCL (pin 3) and input/output SDA (pin 4) conform to I²C-bus specifications.* Pins 3 and 4 are protected against positive voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1, A2 are programmed by a connection to GND for An = 0 or to Vp for An = 1. If the inputs are left floating, An = 1 will result.

FUNCTIONAL DESCRIPTION (continued)

Input V_{max}

Input V_{max} (pin 2) provides a means of compressing the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately V_{max} while the 6-bit resolution is maintained, so giving a finer voltage resolution of smaller output swings.

Digital-to-analogue converters

Each DAC comprises a 6-bit data latch, current switches and an output driver. Current sources with values weighted by 2^0 up to 2^5 are switched according to the data input so that the sum of the selected currents gives the required analogue voltage from the output driver. The range of the output voltage is approximately 0.5 to 10.5 V when $V_{max} = V_P$.

The DAC outputs are protected against short-circuits to V_P and GND.

To avoid the possibility of oscillations, capacitive loading at the DAC outputs should not exceed 2 nF.

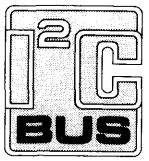
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_1$	−0.5	18	V
Supply current (source)		$I_p = I_1$	–	−10	mA
		$I_P = I_I$	–	40	mA
I^2C-bus line voltage		$V_{3,4}$	−0.5	5.9	V
Input voltage		V_I	−0.5	$V_P + 0.5$	V
Output voltage		V_O	−0.5	$V_P + 0.5$	V
Maximum current on any pin (except pins 1 and 8)		$\pm I_{max}$	–	10	mA
Total power dissipation		P_{tot}	–	500	mW
Operating ambient temperature range		T_{amb}	−20	+ 70	°C
Storage temperature range		T_{stg}	−65	+ 150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 75 K/W



Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CHARACTERISTICS

All voltages are with respect to GND; T_{amb} = 25 °C; V_P = 12 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Voltage level for power-on reset		V_1	1	–	4.8	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	$I_P = I_1$	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input (pin 2)	V_P = 12 V	$V_{max} = V_2$	1.0	–	10.5	V
Pin 2 current	V_2 = 1 V	I_2	–	–	−10	μA
	$V_2 = V_P$	I_2	–	–	10	μA
SDA, SCL inputs (pins 3 and 4)						
Input voltage range		V_I	0	–	5.5	V
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	–	V
Input current LOW	$V_{3;4}$ = 0.3 V	I_{IL}	–	–	−10	μA
Input current HIGH	$V_{3;4}$ = 6 V	I_{IH}	–	–	±10	μA
SDA output (pin 3)						
Output voltage LOW	I_3 = 3 mA	V_{OL}	–	–	0.4	V
Sink current		I_O	3	8	–	mA
Address inputs (pins 5 to 7)						
Input voltage range		V_I	0	–	V_P	V
Input voltage LOW		V_{IL}	–	–	1	V
Input voltage HIGH		V_{IH}	2.1	–	–	V
Input current LOW		I_{IL}	–	−7	−12	μA
Input current HIGH		I_{IH}	–	–	1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
DAC outputs (pins 9 to 16)						
Output voltage range		V_O	0.1	–	V_P–0.5	V
Minimum output voltage	data = 00; I_O = –2 mA	V_{Omin}	0.1	0.4	0.8	V
Maximum output voltage	data = 3F; I_O = –2 mA					
at $V_{max} = V_P$		V_{Omax}	10	10.5	11.5	V
at $1 < V_{max} < 10.5$ V		V_{Omax}		see note		V
Output sink current	V = V_P; data = 1F	I_O	2	8	15	mA
Output source current	V = 0V; data = 1F	I_O	–2	–	–6	mA
Output impedance	data = 1F; $-2 < I_O < +2$ mA	Z_O	–	4	50	Ω
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV
Deviation from linearity	I_O = –2 mA; N ≠ 32		0	–	50	mV
Deviation from linearity	I_O = –2 mA; N = 32		0	–	70	mV

Note to the characteristics

$V_O = 0.95\ V_{max} + V_{Omin}$.

APPLICATION INFORMATION

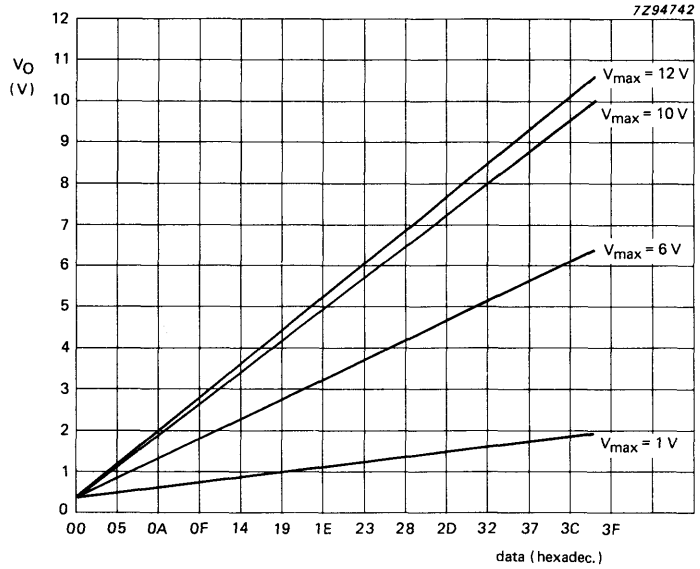


Fig. 4 Graph showing output voltage as a function of the input data value for V_{max} values of 1, 6, 10 and 12 V; V_P = 12 V.

PHOTO DIODE SIGNAL PROCESSOR FOR COMPACT DISC PLAYERS

GENERAL DESCRIPTION

The TDA8808 is a bipolar integrated circuit designed for use in compact disc players with a single spot read-out system. It amplifies the photo-diode signals and processes the error signals for the focus- and radial control network.

Features

- Data amplifier with equalizer and AGC
- Offset-free pre-amplifier with AGC for the servo signals
- Trackloss and drop-out detection
- Start-up procedure for focus
- Normalizing focus error output signal to minimize radial error interference
- Laser supply amplifier and reference source
- Both TDA8808T and TDA8808AT versions suitable for car, portable and home applications
- Single and dual supply application
- Focus in-lock signal; ready signal output (RD)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range						
TDA8808T		V_{ext}	−5,5	−5,0	0	V
TDA8808AT		V_{ext}	V_P	10	12	V
Quiescent supply current	Si/$\overline{RD}$ = 0 V	I_Q	7,5	10	12,5	mA
HF input current (peak-to-peak value)	f_{HFin} = 100 kHz	$I_{HFin(p-p)}$	3	–	10	μA
LF input current (for each diode input)		I_D	0	–	6	μA
Laser supply output current	Si/$\overline{RD}$ = HIGH Z	I_{LO}	−8	−4	−2	mA
Operating ambient temperature range		T_{amb}	−30	–	+85	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

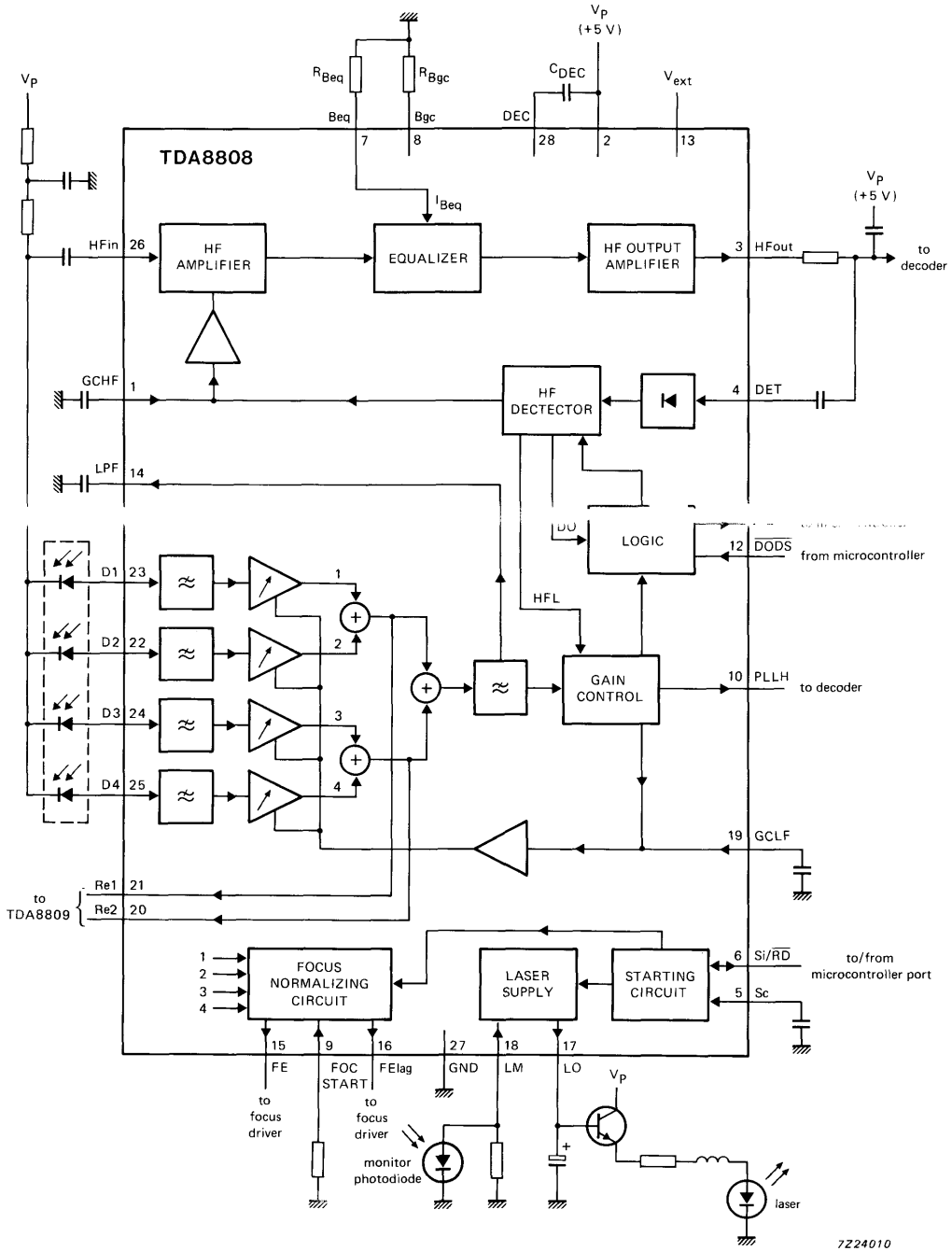


Fig. 1 Block diagram.

PINNING

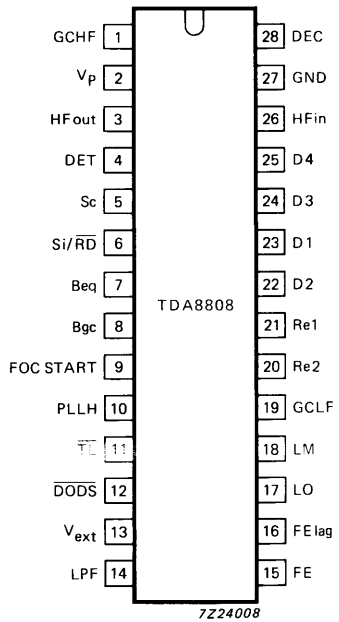


Fig. 2 Pinning diagram.

Pin functions

pin	mnemonic	description
1	GCHF	Gain control input of HF amplifier. Current output from HF amplitude detector
2	V_P	Positive supply voltage
3	HFout	HF amplifier and equalizer voltage output
4	DET	HF detector voltage input
5	Sc	Starting up capacitor input
6	Si/$\overline{RD}$	On/off control (start input); ready signal output (starting up procedure successful)
7	Beq	Equalizer reference current input
8	Bgc	DC and LF gain control reference current input
9	FOC START	Focus normalizing circuit starting current
10	PLLH	PLL on hold output
11	$\overline{TL}$	Track loss output
12	$\overline{DODS}$	Drop out detector suppression input
13	V_{ext}	TDA8808T Negative supply connection for FE and FElag output stage; also substrate connection TDA8808AT Positive supply connection for FE and FElag output stage
14	LPF	Low pass filter for I_{ret}, used in track loss ($\overline{TL}$) detector and LF gain control
15	FE	Current output of normalized, switched focus error signal
16	FElag	Current output of switched focus error signal, intended for lag network
17	LO	Laser amplifier current output
18	LM	Laser monitor diode input
19	GCLF	Gain control input for AC and LF amplifiers. Current output from LF amplitude detector
20	Re2	Summation of amplified currents from D3 and D4
21	Re1	Summation of amplified currents from D1 and D2
23, 22	D1, D2	Current inputs to DC and LF photo diode amplifier
24, 25	D3, D4	Current inputs to DC and LF photo diode amplifier
26	HFin	Current input to HF amplifier
27	GND	Ground connection of device: also substrate connection for TDA8808AT
28	DEC	Decoupling input (internal bypass)

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage ranges (see Fig. 3)				
TDA8808T				
pin 2 to pin 13	$V_P - V_{(ext)}$	−0,3	13	V
pin 27 to pin 13	$V_{GND} - V_{(ext)}$	−0,3	13	V
TDA8808AT				
pin 13 to 27	$V_{ext} - V_{GND}$	−0,3	13	V
pin 2 to pin 27	$V_P - V_{GND}$	−0,3	13	V
Output voltage ranges				
except FE and FE_{lag}	V_O	0	V_P	V
FE and FE_{lag} (TDA8808T)	V_O	V_{ext}	V_P	V
FE and FE_{lag} (TDA8808AT)	V_O	V_{GND}	V_{ext}	V
LM (open loop)	V_O	V_{GND}	V_P	V
Total power dissipation	P_{tot}	see Fig. 4		
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 85	°C
Operating junction temperature	T_j	−	150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 140 K/W

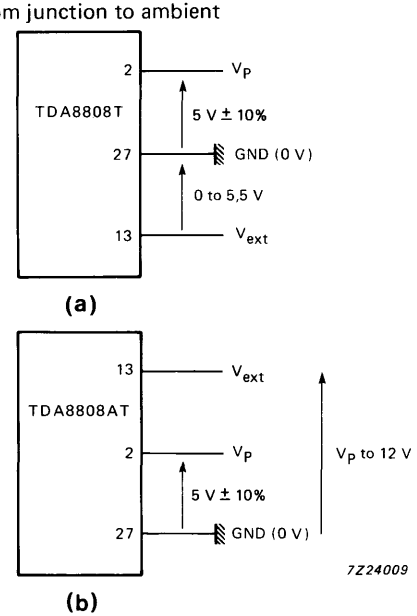


Fig. 3 Supply voltages; (a) TDA8808T, (b) TDA8808AT.

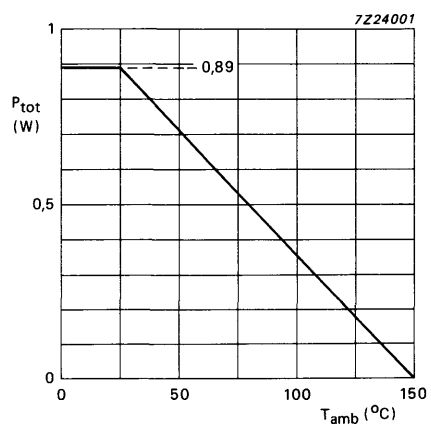


Fig. 4 Power derating curve.

CHARACTERISTICS

V_P = + 5 V; V_{GND} = 0 V; V_{ext} = −5 V (TDA8808T); V_{ext} = + 10 V (TDA8808AT); $V_{RE1} = V_{RE2}$ = 3,5 V; $V_{FE} = V_{FElag}$ = 0 V (TDA8808T); $V_{FE} = V_{FElag}$ = 5 V (TDA8808AT); $R_{FOC\ START}$ = 3,3 kΩ; $I_{Beq} = I_{Bgc}$ = 50 μA (current sources); T_{amb} = 25 °C; all voltages measured with respect to V_{GND}, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range						
TDA8808T		V_{ext}	−5,5	−5,0	0	V
TDA8808AT		V_{ext}	V_P	10	12	V
Quiescent supply current	$V_{Si/\overline{RD}}$ = 0 V	I_Q	7,5	10	12,5	mA
Reference input (Beq)						
Input voltage level		V_{Beq}	500	560	620	mV
Input current		I_{Beq}	–	−50	–	μA
Reference input (Bgc)						
Input voltage level		V_{Bgc}	1,15	1,25	1,35	V
Input current		I_{Bgc}	–	−50	–	μA
Decoupling input (DEC)						
Input voltage level		V_{DEC}	–	V_P−1,4	–	V
Input impedance		$\lvert Z_{DEC}\rvert$	–	2	–	kΩ
HF input (HFin)						
Input voltage level		V_{HFin}	–	1,4	–	V
HF input current (peak-to-peak value)	f_{HFin} = 100 kHz	$I_{HFin(p-p)}$	3	–	10	μA
Input impedance		$\lvert Z_{HFin}\rvert$	0,5	1	2	kΩ
HF part						
DC characteristics						
Gain (G1) = $\frac{\Delta V_{HFout}}{\Delta I_{HFin}}$	I_{HFin} = ± 1 μA					
Maximum gain	V_{GCHF} = 4 V	G1(max)	390	480	570	mV/μA
Minimum gain	V_{GCHF} = 1,5 V	G1(min)	−5	0	5	mV/μA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
HF part (continued)						
AC characteristics						
Gain (G2) = 20 log $\frac{V_{O1}}{V_{O2}}$	note 1	G2	2	3,5	5	dB
Gain (G3) = 20 log $\frac{V_{O1}}{V_{O2}}$	note 2	G3	4	5,5	7	dB
Phase of input/output signal at 1 MHz	note 3	ϕ	–	$\pi/2$	–	rad.
Group delay at f_{HFin} = 300 kHz + Δf	note 3	$\tau 300$	–	290	–	ns
Flatness between 0,1 and 1 MHz	note 3	$\Delta\tau$	*	9	*	ns
HF output (HFout)						
Output voltage at I_{HFin} = 0	V_{GCHF} = 4 V	V_{HFout}	1,5	2,4	3,3	V
Output voltage (peak-to-peak value)						
at $I_{HFin(p\text{-}p)}$ = 7 μA	note 4	$V_{O1(p\text{-}p)}$	1	1,20	–	V
at $I_{HFin(p\text{-}p)}$ = 4 to 10 μA	note 5	$V_{O(p\text{-}p)}$	−20%	M_1	+20%	V
Output impedance		$\lvert Z_{HFout}\rvert$	–	60	–	Ω
HF detector input (DET)	see Fig. 5					
DC voltage level	I_{DET} = 0	V_{DET0}	–	2,2	–	V
Positive reference voltage V_{DET} to V_{DET0}		V_{refp}	−10%	540	+10%	mV
Negative reference voltage V_{DET} to V_{DET0}		V_{refn}	−5%	$-V_{refp}$	+5%	mV
Input impedance		$\lvert Z_{DET}\rvert$	–	9	–	kΩ

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Gain control (GCHF)						
Input voltage for:						
minimum HF gain		V_{GCHF}	–	1,8	–	V
maximum HF gain		V_{GCHF}	–	3,4	–	V
Input impedance						
at V_{GCHF} = 1,5 to 4 V		$\lvert Z_{GCHF}\rvert$	–	25	–	MΩ
Output current (see Fig. 5)						
$\Delta V_{DET} < V_{refn}$ or $\Delta V_{DET} > V_{refp}$	$\overline{DODS}$ = LOW	I_{GCHF}	90	100	110	μA
$\Delta V_{DET} < V_{refn}$ or $\Delta V_{DET} > V_{refp}$	$\overline{DODS}$ = HIGH	I_{GCHF}	86	96	106	μA
$V_{refn} < \Delta V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{refp}$	$\overline{DODS}$ = LOW	I_{GCHF}	−0,65	−0,35	−0,2	μA
$V_{refn} < \Delta V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{refp}$	$\overline{DODS}$ = HIGH	I_{GCHF}	−5,0	−4,4	−3,8	μA
$V_{DETn1} < \Delta V_{DET} < V_{DETp1}$	$\overline{DODS}$ = X*	I_{GCHF}	−0,65	−0,35	−0,2	μA
V_{DETp1}/V_{refp}; V_{DETn1}/V_{refn}			10	12,5	15	%
PLLH output (pin 10)						
Output voltage LOW						
I_{PLLH} = 400 μA (sink current)		V_{PLLHL}	–	–	0,4	V
Output voltage HIGH						
I_{PLLH} = −50 μA (source current)		V_{PLLHH}	2,4	–	–	V
Output sink current		I_{PLLH}	0,5	1,5	–	mA
Output source current		I_{PLLH}	–	−100	−50	μA
Threshold total LF current	V_{GCLF} = 3,5 V	I_{DT1}	–	2,0	–	μA
V_{DETp2}/V_{refp}; V_{DETn2}/V_{refn}			57,5	62,5	67,5	%
LF photo diode inputs (pins 22 to 25) (values given for each input)						
DC voltage level		V_D	–	1,2	–	V
Input current range		I_D	0	–	6	μA
Input impedance at 1 MHz	I_D = 1 μA	$\lvert Z_D\rvert$	–	10	–	kΩ

* X = don't care.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
LF gain						
Maximum DC gain						
for: $A_1 = \left\lvert \frac{I_{Re1}}{I_{D1} + I_{D2}} \right\rvert$;						
$I_{D3} = I_{D4} = 0$	V_{GCLF} = 3,5 V					
at $I_{D1} = 0\ \mu A$; $I_{D2} = 1\ \mu A$		A_{11}	S_1−10%	S_1	S_1	
at $I_{D1} = 1\ \mu A$; $I_{D2} = 0\ \mu A$		A_{12}	S_1 or 55	S_1	S_1	
for: $A_2 = \left\lvert \frac{I_{Re2}}{I_{D3} + I_{D4}} \right\rvert$;						
$I_{D1} = I_{D2} = 0$	V_{GCLF} = 3,5 V					
at $I_{D3} = 0\ \mu A$; $I_{D4} = 1\ \mu A$		A_{21}	S_1−10%	S_1	S_1	
at $I_{D3} = 1\ \mu A$; $I_{D4} = 0\ \mu A$		A_{22}	S_1 or 55	S_1	S_1	
S_1 mean value of A_{11}, A_{12}, A_{21}, A_{22}			55	64	84	
Minimum DC gain						
for: $A_3 = \left\lvert \frac{I_{Re1}}{I_{D1} + I_{D2}} \right\rvert$;						
$I_{D3} = I_{D4} = 0$	V_{GCLF} = 0,8 V					
at $I_{D1} = 0\ \mu A$; $I_{D2} = 1\ \mu A$		A_{31}	S_2−1	S_2	S_2+1	
at $I_{D1} = 1\ \mu A$; $I_{D2} = 0\ \mu A$		A_{32}	S_2−1	S_2	S_2+1	
for: $A_4 = \left\lvert \frac{I_{Re2}}{I_{D3} + I_{D4}} \right\rvert$;						
$I_{D1} = I_{D2} = 0$	V_{GCLF} = 0,8 V					
at $I_{D3} = 0\ \mu A$; $I_{D4} = 1\ \mu A$		A_{41}	S_2−1	S_2	S_2+1	
at $I_{D3} = 1\ \mu A$; $I_{D4} = 0\ \mu A$		A_{42}	S_2−1	S_2	S_2+1	
S_2 mean value of A_{31}, A_{32}, A_{41}, A_{42}			−0,1	0,7	3	

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
LF gain (continued)						
AC gain for:						
$G_4 = 20 \log P_1$; $I_{D3} = I_{D4} = 0$						
at $I_{D1} = 0$; $I_{D2(p-p)} = 1\ \mu A + 2\ \mu ADC$	note 6	G_4	−4,5	−3	−1,5	dB
at $I_{D1(p-p)} = 1\ \mu A + 2\ \mu ADC$; $I_{D2} = 0$	note 6	G_4	−4,5	−3	−1,5	dB
$G_5 = 20 \log P_2$; $I_{D1} = I_{D2} = 0$						
at $I_{D3} = 0$; $I_{D4(p-p)} = 1\ \mu A + 2\ \mu ADC$	note 7	G_5	−4,5	−3	−1,5	dB
at $I_{D3(p-p)} = 1\ \mu A + 2\ \mu ADC$; $I_{D4} = 0$	note 7	G_5	−4,5	−3	−1,5	dB
Gain control (GCLF)						
Input voltage for:						
minimum LF gain		V_{GCLF}	–	1	–	V
maximum LF gain		V_{GCLF}	–	2,8	–	V
Input impedance		$\lvert Z_{GCLF} \rvert$	–	25	–	MΩ
Threshold total LF current	I_{DT3}		–	1,6	–	mA
Output current (see Fig. 7)						
$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	$I_{DT} < I_{DT3}$	I_{GCLF}	–	$-0,6\ I_{Bgc}$	± 10	μA
	$I_{DT} > I_{DT3}$; note 8	I_{GCLF}	S_6-10	S_6	S_6+10	μA
$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$		I_{GCLF}	–	$-0,2\ I_{Bgc}$	± 2	μA
Re1, Re2 outputs (pin 21, pin 20)						
Output current	V_{GCLF} = 3,5 V					
at $I_{D1} = I_{D2} = 1\ \mu A$; $I_{D3} = I_{D4} = 0$		I_{Re1}	110	128	168	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$		I_{Re1}	–	0	–	μA
at $I_{D1} = I_{D2} = 0$; $I_{D3} = I_{D4} = 1\ \mu A$		I_{Re2}	110	128	168	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$		I_{Re2}	–	0	–	μA
Output voltage						
pin 21		V_{Re1}	1	–	V_P	V
pin 20		V_{Re2}	1	–	V_P	V
Output impedance						
pin 21		$\lvert Z_{Re1} \rvert$	–	1	–	MΩ
pin 20		$\lvert Z_{Re2} \rvert$	–	1	–	MΩ

parameter	conditions	symbol	min.	typ.	max.	unit
Reference current (I_{ret})						
$I_{ret} = I_{Re1} = I_{Re2}$	note	I_{ret}	200	220	240	μA
LPF output (pin 14)						
DC voltage level	note 9	V_{LPF}	$V_P-2,1$	$V_P-1,7$	$V_P-1,4$	V
Input impedance		$\lvert Z_{LPF}\rvert$	–	3	–	kΩ
FOC START input (pin 9)						
Start current (ST) for FE ($-I_{FOC\ START} = I_{ST}$)	Si/$\overline{RD}$ = HIGH Z	I_{ST}	75	150	500	μA
	Si/$\overline{RD}$ = LOW	I_{ST}	–	0	–	μA
Start voltage (ST) for FE ($V_{FOC\ START} = V_{ST}$)	Si/$\overline{RD}$ = HIGH Z	V_{ST}	430	530	630	mV
	Si/$\overline{RD}$ = LOW	V_{ST}	−20	0	20	mV
FElag output (pin 16)	see Fig. 8					
Output voltage						
TDA8808T		V_{FElag}	$V_{ext}+1,5$	–	$V_P-1,5$	V
TDA8808AT		V_{FElag}	+1,5	–	$V_{ext}-1,5$	V
Output impedance		$\lvert Z_{FElag}\rvert$	–	8	–	MΩ
Output current	Si/$\overline{RD}$ = HIGH Z; V_{GCLF} = 3,5 V					
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	$I_{FElag} = I_O$	−10	0	+10	μA
$I_{D2} = I_{D3} = 1\ \mu A$; $I_{D1} = I_{D4} = 2\ \mu A$	$V_{Sc} = V_P$	I_{FElag}	−10%	$-2S_1 + I_O$	+10%	μA
$I_{D2} = I_{D3} = 2\ \mu A$; $I_{D1} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	I_{FElag}	−10%	$-2S_1 + I_O$	+10%	μA
$I_{D2} = I_{D3} = 2\ \mu A$; $I_{D1} = I_{D4} = 1\ \mu A$	V_{Sc} = 1,5 V	I_{FElag}	−5	0	+5	μA
$I_{D2} = I_{D3} = 1\ \mu A$; $I_{D1} = I_{D4} = 2\ \mu A$	V_{Sc} = 1,5 V	I_{FElag}	−5	0	+5	μA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
FE output (pin 15)	see Fig. 8					
Output voltage						
TDA8808T		V_{FE}	$V_{ext}+1,5$	–	$V_P-1,5$	V
TDA8808AT		V_{FE}	+1,5	–	$V_{ext}-1,5$	V
Output impedance		$\|Z_{FE}\|$	–	8	–	MΩ
Output current	note 10					
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 0$	I_{FE}	−10%	$-2S_1-134-I_{ST}$	+10%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 0$	I_{FE}	−10%	$-4S_1-67-I_{ST}$	+10%	μA
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 1,25$ V	I_{FE}	−10%	$-2S_1-134+I_{ST}$	+20%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 1,25$ V	I_{FE}	−10%	$-4S_1-67+I_{ST}$	+20%	μA
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 1,75$ V	I_{FE}	−20%	$-2S_1+67+I_{ST}$	+10%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 1,75$ V	I_{FE}	−10%	$-4S_1-67+I_{ST}$	+20%	μA
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = V_P$	$I_{FE} = S_6$	−20%	67	+20%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = V_P$	I_{FE}	−15%	$-S_6$	+15%	μA
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	I_{FE}	−10	0	+10	μA
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$	$V_{Sc} = V_P$	I_{FE}	−5	0	+5	μA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{\text{DODS}}$ logic input (pin 12)						
Switching levels						
input voltage LOW		$V_{\overline{DODS}}$	–	–	+0,8	V
input voltage HIGH		$V_{\overline{DODS}}$	+2	–	–	V
Input source current		$I_{\overline{DODS}}$	–35	–25	–15	μA
Starting input (Sc)	see Fig. 9					
Output voltage	Si/$\overline{\text{RD}}$ = LOW	V_{Sc}	–	0	–	V
Output voltage	S1/$\overline{\text{RD}}$ = HIGH Z	V_{Sc}	–	–	V_P–0,5	V
Output impedance		$\lvert Z_{Sc} \rvert$	–	*	–	MΩ
Output source current	Si/$\overline{\text{RD}}$ = HIGH Z; V_{Sc} = 1,5 V	I_{Sc}	–1,2	–1	–0,8	μA
Output sink current	Si/$\overline{\text{RD}}$ = LOW	I_{Sc}	0,5	1,2	2,0	mA
Si/$\overline{\text{RD}}$ logic input/output (pin 20)	see Fig. 9					
Voltage "forced LOW"	$I_{Si/\overline{RD}}$ = 400 μA; V_{Sc} = 2,5 V; V_{GCLF} < 2,8 V	$V_{Si/\overline{RD}}$	–	0,15	0,4	V
Switching levels						
input voltage LOW		$V_{Si/\overline{RD}}$	–	–	+0,8	V
input voltage HIGH Z	$I_{Si/\overline{RD}}$ = –5 μA	$V_{Si/\overline{RD}}$	2,4	2,8	–	V
Input source current LOW		$I_{Si/\overline{RD}}$	–35	–25	–15	μA
$\overline{\text{TL}}$ logic output (pin 11)	see Fig. 6					
Output voltage level LOW	$I_{\overline{TL}}$ = 400 μA; (sink current)	$V_{\overline{TL}}$	–	0,15	0,4	V
Output voltage level HIGH	$I_{\overline{TL}}$ = –50 μA; (source current)	$V_{\overline{TL}}$	2,4	–	–	V
Threshold total LF current	I_{DT2}		–	3,9	–	μA
Output voltage	DODS = HIGH (≥ 2,4 V)					
$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	I_{DT} don't care	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn1} < \Delta V_{DET} < V_{DETp1}$	I_{DT} don't care	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} < I_{DT2}$	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < V_{DET} < V_{DETn1}$ or $V_{DETp1} < V_{DET} < V_{DETp2}$	$I_{DT} > I_{DT2}$	$V_{\overline{TL}}$	–	0,15	0,4	V

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{TL}$ logic output (continued)						
Output voltage	$\overline{DODS}$ = LOW ($\leqslant$ 0,8 V)					
$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	I_{DT} don't care	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} < I_{DT2}$	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} > I_{DT2}$	$V_{\overline{TL}}$	–	0,15	0,4	V
Output sink current	$V_{\overline{TL}}$ = LOW	$I_{\overline{TL}}$	1	2,2	–	mA
Output source current	$V_{\overline{TL}}$ = HIGH	$I_{\overline{TL}}$	–	−100	−50	μA
Delay times (see Fig. 10)	see Fig. 6	$\tau 1$	7	8,5	10	μs
		$\tau 2$	$\tau 1$−15% or 6,5	–	$\tau 1$+ 5% or 10	μs
		$\tau 3$	7	8,5	10	μs
		$\tau 4$	$\tau 3$−10% or 7	–	$\tau 3$+10% or 10	μs
LO output (pin 17)						
Output voltage		V_{LO}	–	–	V_P − 0,5	V
Output impedance		$\lvert Z_{LO} \rvert$	–	95	–	kΩ
Output leakage current	Si/$\overline{RD}$ = LOW	I_{LO}	−10	−0,1	0	μA
Maximum output current	Si/$\overline{RD}$ = HIGH Z	I_{LO}	−8	−4	−2	mA
LM input (pin 18)						
Input voltage	closed loop	V_{LM}	185	205	225	mV
Input bias current		I_{LM}	−2	–	–	μA
Laser supply						
Transconductance						
For DC (note 11)	Si/$\overline{RD}$ = HIGH Z	G_{LDC}	–	0,5	–	A/V
	Si/$\overline{RD}$ = LOW	G_{LDC}	–	0	–	A/V
For AC (note 12) delay time		τLO	–	*	–	ns

* Value to be fixed.

Notes to the characteristics

1. Voltage output signal V_{O1} measured at f_{HFin} = 700 kHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
   Voltage output signal V_{O2} measured at f_{HFin} = 100 kHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
2. Voltage output signal V_{O1} measured at f_{HFin} = 1 MHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
   Voltage output signal V_{O2} measured at f_{HFin} = 100 kHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
3. Phase of input/output signal, group delay and flatness measured at $I_{HFin(p-p)}$ = 1 μA; V_{GCHF} = 4 V.

   Group delay: $\tau = \frac{d\phi}{dw}$; $\Delta f \approx 50$ kHz.

   Flatness: $\Delta\tau = \tau_{max} - \tau_{min}$.
4. HF part output vpltage for closed loop conditions; f_{HFin} = 500 kHz.
5. HF part output voltage for closed loop conditions; f_{HFin} = 0,1 to 1 MHz.
   M_1 is the measured value of V_{O1}.
6. P_1 is the measured value of $\frac{I_{Re1}(1)}{I_{D1}(1) + I_{D2}(1)} \cdot \frac{I_{D1}(2) + I_{D2}(2)}{I_{Re1}(2)}$

   Where:

   (1) are the current levels at f_i = 25 kHz.
   (2) are the current levels at f_i = 1 kHz.

   Measurement taken at V_{GCLF} = 3,5 V.
7. P_2 is the measured value of $\frac{I_{Re2}(1)}{I_{D3}(1) + I_{D4}(1)} \cdot \frac{I_{D3}(2) + I_{D4}(2)}{I_{Re2}(2)}$

   Where:

   (1) are the current levels at f_i = 25 kHz.
   (2) are the current levels at f_i = 1 kHz.

   Measurement taken at V_{GCLF} = 3,5 V.
8. S_6 is the measured value of $S_1 \cdot \frac{I_{DT}}{4} - 1{,}1\ I_{Bgc}$

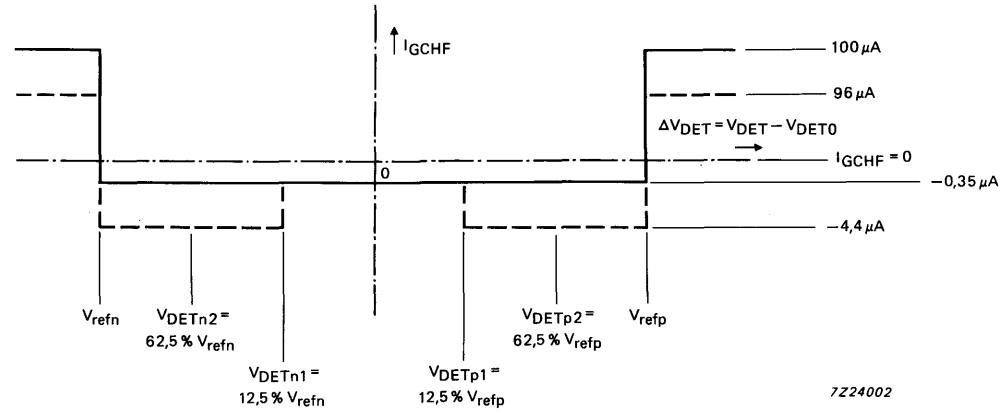
   Measurement taken at V_{GCLF} = 3,5 V.
9. LF part reference current I_{ret} and low-pass filter output voltage for closed loop conditions.
   Measurement taken at $I_{DT} > I_{DT3}$; $\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$.
10. FE output current measured at V_{GCLF} = 3,5 V and Si/$\overline{RD}$ = HIGH Z; $I_{ST} = \frac{V_{FOC\ START}}{R_{FOC\ START}}$.
11. Laser supply transconductance for DC

    $G_{LDC} = \frac{\Delta I_{LO}}{\Delta V_{LM}}$ $(0 < -I_{LO} < 2$ mA).
12. Laser supply transconductance for AC

    $G_{LAC} = G_{LO} \cdot \frac{1}{1 + S \cdot \tau LO}$

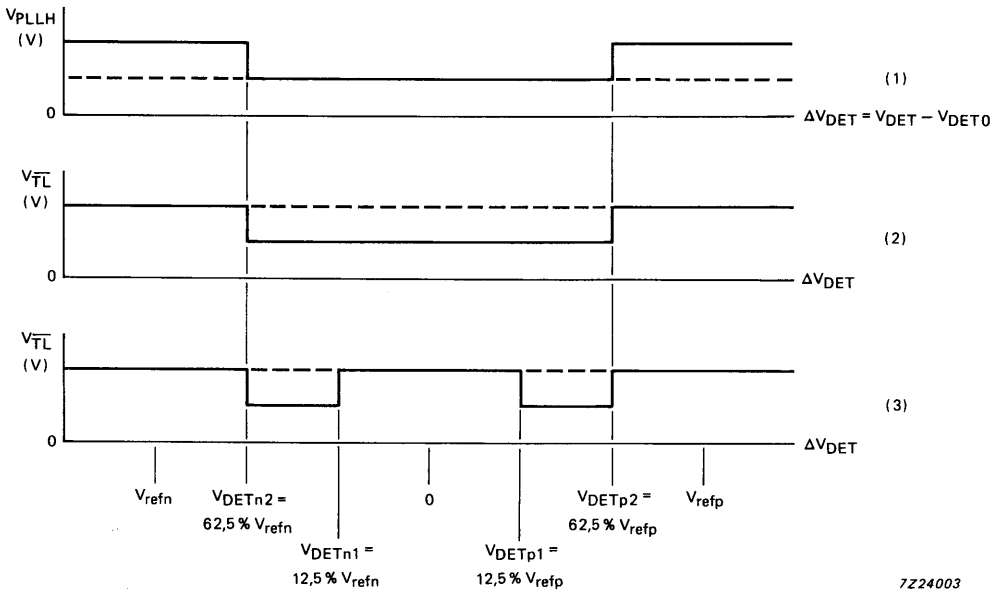
    Where: S is the laplace operator in the frequency domain.

DEVELOPMENT DATA



---------- $\overline{DODS}$ = HIGH
——— $\overline{DODS}$ = LOW

Fig. 5 HF gain control current (I_{GCHF}) as a function of input voltage ΔV_{DET}.



(1)

——— $I_{DT} > I_{DT1}$

--------- $I_{DT} < I_{DT1}$

$I_{DT} = I_{D1} + I_{D2} + I_{D3} + I_{D4}$

$I_{DT1} = 2{,}67\ I_{Bgc}/S_1$

$I_{DT2} = 5\ I_{Bgc}/S_1$

S_1 = average maximum LF gain

(2)

——— $I_{DT} > I_{DT2}$

--------- $I_{DT} < I_{DT2}$

$\overline{DODS}$ = LOW

(3)

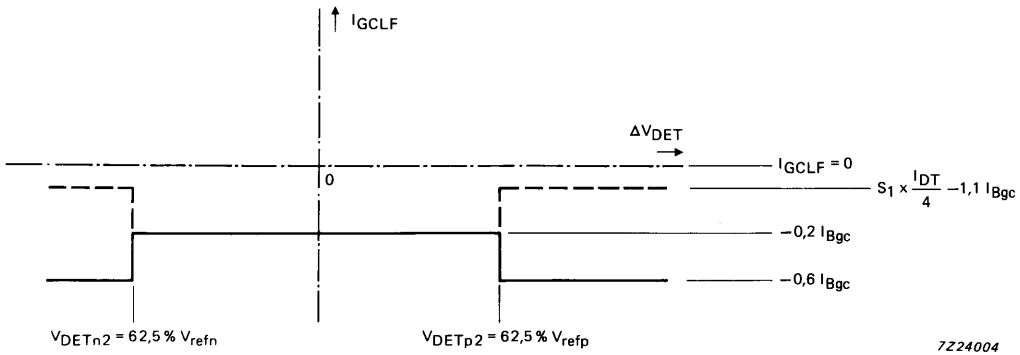
——— $I_{DT} > I_{DT2}$

--------- $I_{DT} < I_{DT2}$

$\overline{DODS}$ = HIGH

Fig. 6 $\overline{TL}$ voltage as a function of input voltage ΔV_{DET}.

DEVELOPMENT DATA



---------- $I_{DT} > I_{DT3}$

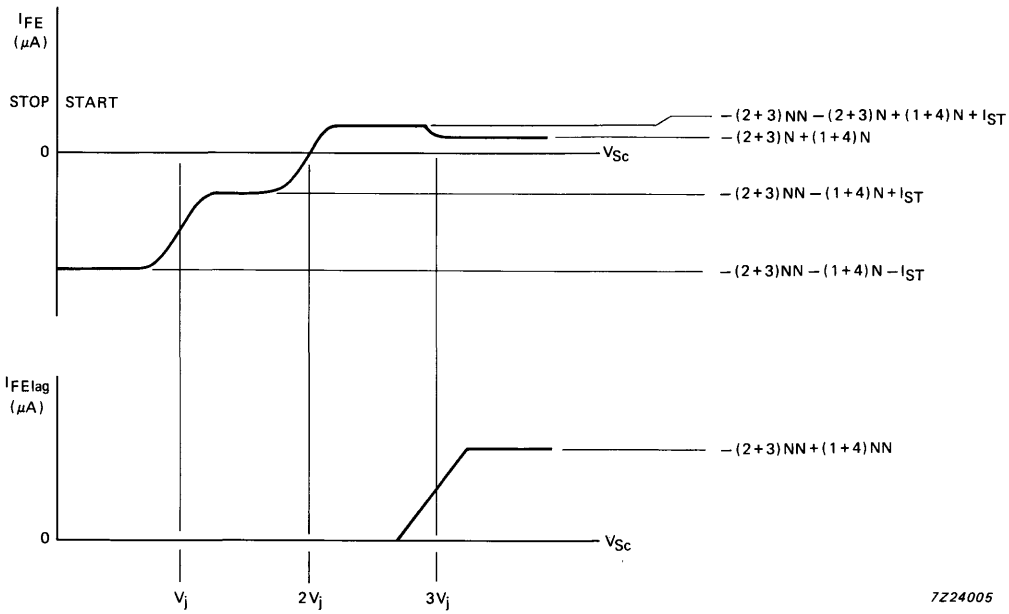
——— $I_{DT} < I_{DT3}$

$I_{DT} = I_{D1} + I_{D2} + I_{D3} + I_{D4}$

$I_{DT3} = 2\ I_{Bgc}/S_1$

S_1 = average maximum LF gain

Fig. 7 LF gain control current (I_{GCLF}) as a function of input voltage ΔV_{DET}.



DEVELOPMENT DATA

I_{ST} = $-I_{FOC\ START}$

I_{cont} = $2\ I_{Bgc}$ if $I_{DT} > I_{DT3}$

I_{cont} = $I_{DT} \times S_1$ if $I_{DT} < I_{DT3}$

I_{DT} = $I_{D1} + I_{D2} + I_{D3} + I_{D4}$

I_{DT3} = $2\ I_{Bgc}/S_1$

S_1 = average maximum LF gain

(1 + 4)NN = not normalized currents = $(I_{D1} + I_{D4})\ S_1$

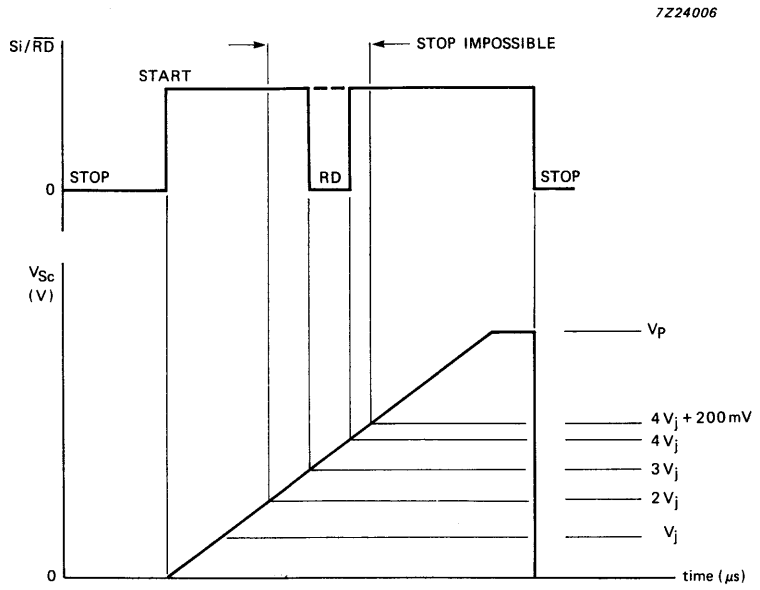
(2 + 3)NN = not normalized currents = $(I_{D2} + I_{D3})\ S_1$

(1 + 4)N = normalized currents = $\left(\frac{I_{D1}}{I_{D1} + I_{D2}} + \frac{I_{D4}}{I_{D3} + I_{D4}}\right) \times I_{cont}$

(2 + 3)N = normalized currents = $\left(\frac{I_{D2}}{I_{D1} + I_{D2}} + \frac{I_{D3}}{I_{D3} + I_{D4}}\right) \times I_{cont}$

V_j is the junction voltage (0,7 V typ.).

Fig. 8 FElag current output as a function of starting voltage input (V_{Sc}).



RD : Si/$\overline{RD}$ forced LOW for ready signal

——— $V_{GCLF} < 2{,}8$ V

---------- $V_{GCLF} > 3{,}5$ V

V_j is the junction voltage (0,7 V typ.)

Fig. 9 Si/$\overline{RD}$ signal as a function of V_{Sc}.

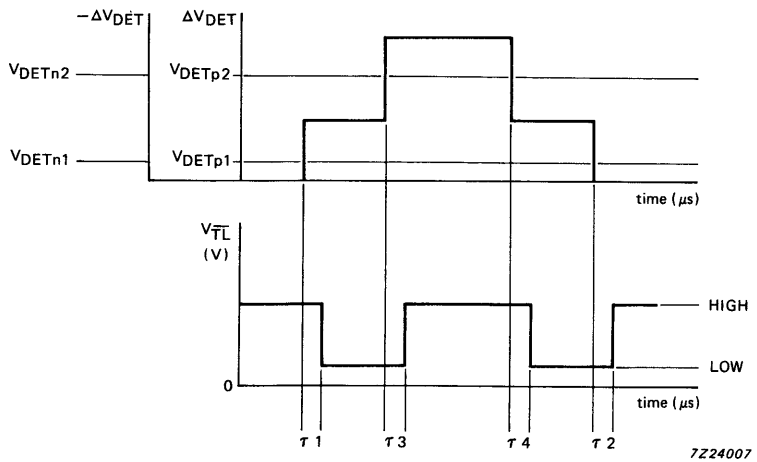


Fig. 10 Delay times between ΔV_{DET} and $V_{\overline{TL}}$.

TRANSFER FUNCTIONS OF THE TDA8808

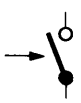
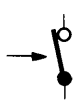
GENERAL

A description of several transfer functions is given on the following pages. These transfer functions will provide application engineers with a full understanding of the operation of the integrated circuit. A number of general parameters are used to aid the explanation. Their given values are typical. Tolerance values are detailed in the TDA8808 data sheet.

General parameters

parameter	description
V_j	junction voltage, 0,7 V at T_{amb} = 25 °C; temperature coefficient approximately −2 mV/°C
V_T	$V_T = \frac{k \cdot T}{q}$ = 25,86 mV at 300 K where: k = Boltzmann constant T = absolute temperature q = charge of one electron
S	the Laplace operator in the frequency domain
I_{int}	internal reference current (100 μA, typ.), which has a negative temperature coefficient
I_{Bgc}	internal reference current, externally fixed by resistor R_{Bgc}. This current is temperature independent. $I_{Bgc} \approx 50\ \mu A$ with $R_{Bgc} = 24\ k\Omega$
I_{Beq}	internal reference current, externally fixed by resistor R_{Beq}. This current has a positive temperature coefficient $I_{Beq} \approx 50\ \mu A$ with $R_{Beq} = 12\ k\Omega$

Table 1 Control of switches

symbol/control	control 	control 
control = 0	open	closed
control = 1	closed	open

Voltages indicated are measured with respect to V_{GND}.

Reference currents (I_{int}, I_{Bgc}, I_{Beq})

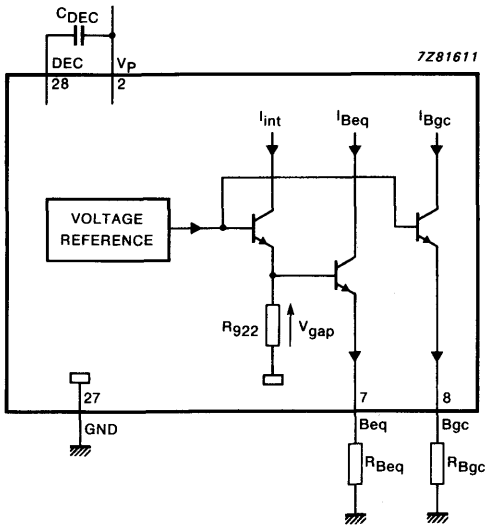


Fig. 1 Block diagram; reference currents I_{int}, I_{Bgc} and I_{Beq}.

Where:

Voltage reference level = $V_{gap} \approx 1{,}2$ V

$$I_{int} = \frac{V_{gap}}{R_{922}} \approx \frac{1{,}2\ V}{R_{922}} \qquad \text{at } R_{922} = 12\ k\Omega\ (I_{int} \approx 100\ \mu A)$$

$$I_{Bgc} = \frac{V_{gap}}{R_{Bgc}} \approx \frac{1{,}2\ V}{R_{Bgc}} \qquad \text{at } R_{Bgc} = 24\ k\Omega\ (I_{Bgc} \approx 50\ \mu A)$$

$$I_{Beq} = \frac{V_{gap} - 1\ V_j}{R_{Beq}} \approx \frac{1{,}2\ V - V_j}{R_{Beq}} \qquad \text{at } R_{Beq} = 12\ k\Omega\ (I_{Beq} \approx 50\ \mu A)$$

HF part

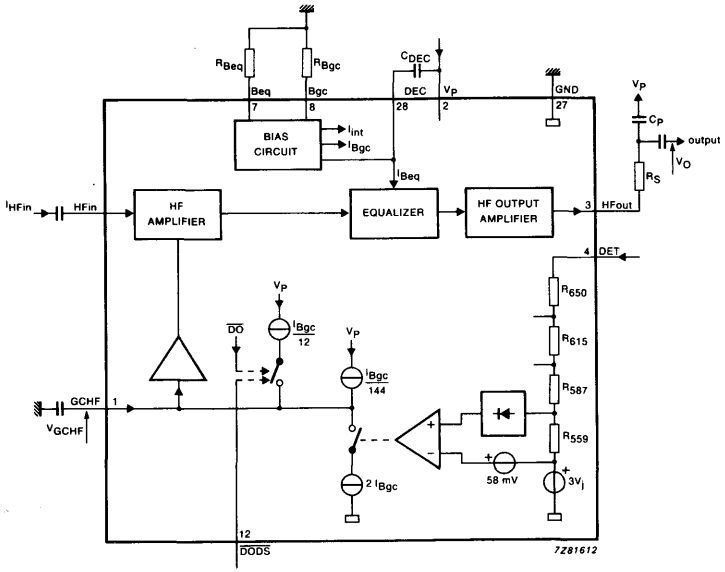


Fig. 2 Block diagram; HF amplifier.

The transfer function from HFin (pin 26) to HFout (pin 3) with V_{GCHF} as parameter is given by:

$$\frac{V_O}{I_{HFin}} = G1 \cdot G2 \ (V/A)$$

Where:

$$G1 = R_T \cdot \left(\frac{V_{GCHF} - 3\,V_j}{4 \cdot R_{504} \cdot \frac{V_{gap}}{R_{922}}} \right) \quad \text{with: } 0 \leqslant \frac{V_{GCHF} - 3\,V_j}{4 \cdot R_{504} \cdot \frac{V_{gap}}{R_{922}}} \leqslant 1$$

$$G2 = \frac{1 - 4\,(S/\omega_o)^2}{1 + 1{,}45\,(S/\omega_o) + (S/\omega_o)^2} \cdot \frac{1}{1 + S \cdot R_S \cdot C_P}$$

R_{504} = integrated resistor 3,5 kΩ (typ.).
R_T = transfer resistance 480 kΩ (typ.).
V_{GCHF} = gain control voltage; active range 1,8 to 3,4 V.
ω_o = $1{,}02\ 10^{11} \times \frac{1}{R_{Beq}}$ (rad/s).
R_{Beq} = external resistor (12 kΩ; typ.) connected to pin Beq.
R_S = external resistor (1 kΩ ± 2%) connected to pin HFout.
C_P = external capacitor (100 pF ± 2%) connected to pin HFout via R_S. R_S and C_P are typical applications.
R_{559} = integrated resistor 1055 Ω (typ.).
R_{587} = integrated resistor 632 Ω (typ.).
R_{615} = integrated resistor 6749 Ω (typ.).
R_{650} = integrated resistor 564 Ω (typ.).

DEVELOPMENT DATA

HF level detector

The HF level detector comprises three temperature compensated rectifier comparators.

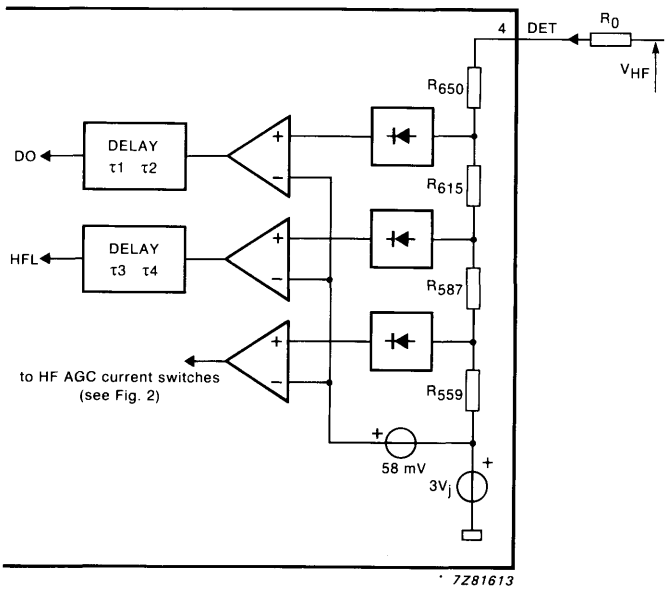


Fig. 3 Block diagram; HF level detector.

Transfer functions:

$$|\text{HFL trigger level}| = \frac{9\,k + R_O}{R_{559} + R_{587}} \cdot 0{,}058\ \text{V} = 0{,}625\ V_{ref}$$

$$|\text{DO trigger level}| = \frac{9\,k + R_O}{R_{559} + R_{587} + R_{615}} \cdot 0{,}058\ \text{V} = 0{,}125\ V_{ref}$$

The transfer functions from V_{DET} to DO and HFL as a function of time are given in Fig. 4.

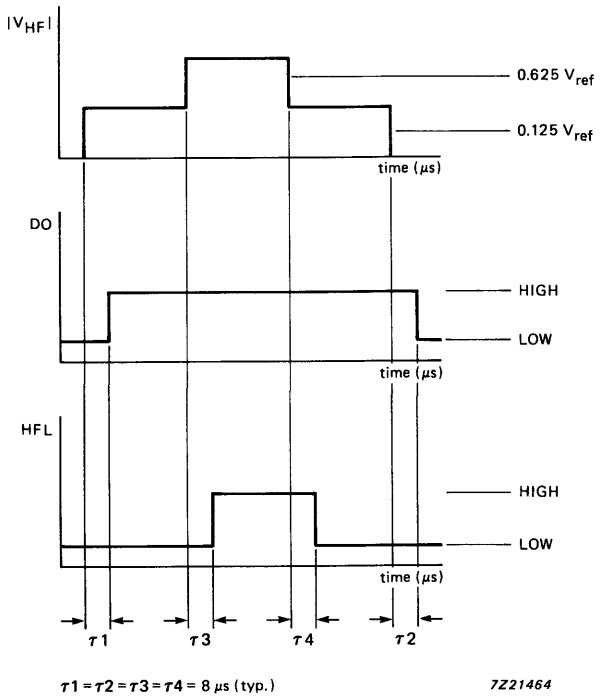


Fig. 4 Timing relation; HF level detector.

DEVELOPMENT DATA

HF AGC

The transfer function from V_{HF} to I_{GCHF} is shown in Fig. 5.

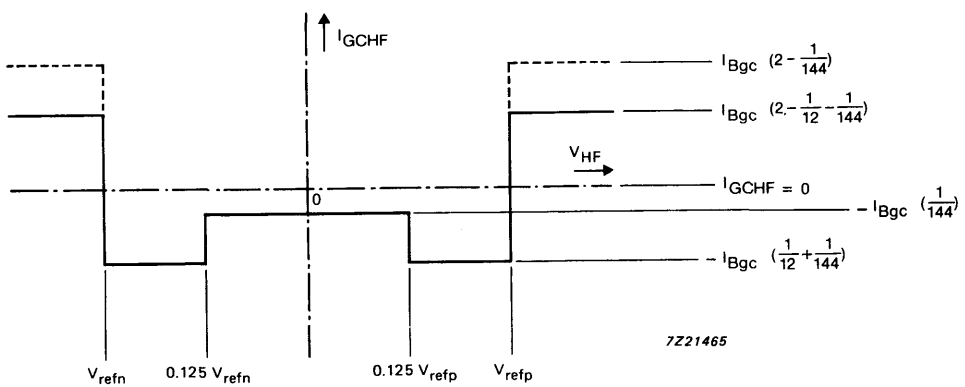


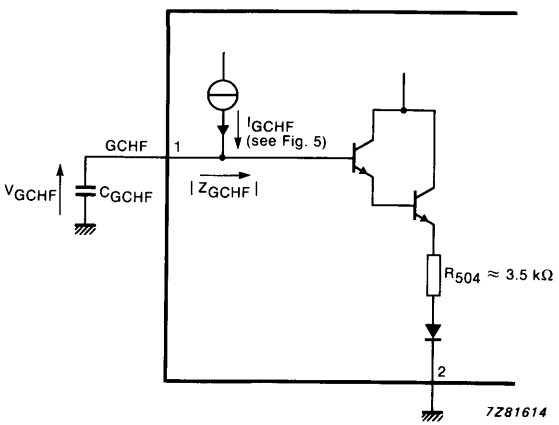
Fig. 5 I_{GCHF} as a function of V_{DET}.

HF AGC (continued)

When the HF AGC loop is closed i.e. pin GCHF connected to GND via a capacitor and pin HF out connected to pin DET via a capacitor, a fully integrated first order loop is obtained.
In this situation the amplitude of the HF output signal is temperature compensated.
In this condition the HF amplitude is regulated to:

$$|V_{HF(max)}| = \frac{9\,k + R_O}{R_{559}} \cdot 0{,}058\ V = V_{ref}$$

Input impedance of HF gain control input



$|Z_{GCHF}| \approx 25\ M\Omega$.

Fig. 6 GCHF equivalent input circuit.

DEVELOPMENT DATA

Transfer function from (D1 + D2) input to Re1 output

The current gain from the (D1 + D2) input to the Re1 output is equal to the current gain from the (D3 + D4) input to the Re2 output.

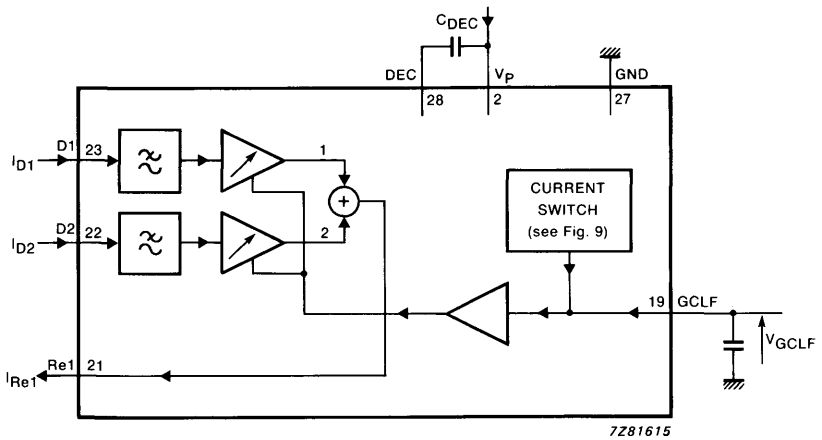


Fig. 7 Block diagram; (D1 + D2) input to Re1 output.

The transfer function is given by:

$$\frac{I_{Re1}}{I_{D1}+I_{D2}} = \frac{I_{Re2}}{I_{D3}+I_{D4}} = G3 \cdot G4$$

Where:

$$G3 = k_1 \cdot \frac{V_{GCLF} - 2V_j}{3 \cdot R_{171} \cdot \frac{V_{gap}}{R_{922}}} \text{ with } 0 < \frac{V_{GCLF} - 2V_j}{3 \cdot R_{171} \cdot \frac{V_{gap}}{R_{922}}} \leqslant 1$$

$$G4 = \frac{1}{1 + (S/\omega_1)}$$

k_1 = fixed, typical 64 times.
V_{GCLF} = gain control voltage for LF amplifier, $1\,V \leqslant V_{GCLF} \leqslant 2{,}8\,V$; active range.
R_{171} = integrated resistor 4 kΩ (typ.).
ω_1 = 157 10^3 radians per second (fixed).

When the LF AGC loop is closed i.e. pin GCLF connected to GND via a capacitor, a fully integrated first order loop is obtained.

Low pass filter (LPF; pin 14)

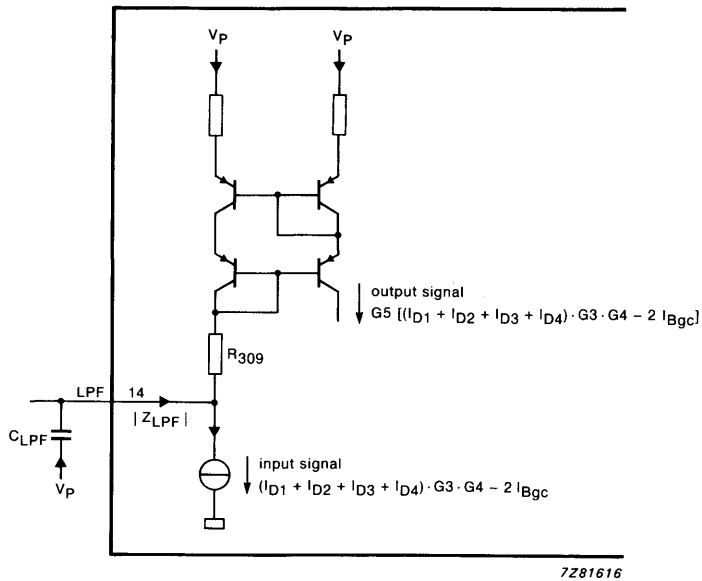


Fig. 8 Low pass filter (LPF); equivalent circuit.

Where:

$$(I_{D1} + I_{D2} + I_{D3} + I_{D4}) \cdot G3 \cdot G4 - 2I_{Bgc} \geqslant 0$$

$$G5 = \frac{1}{1 + S/\omega_2}$$

$$\omega_2 = \frac{1}{Z_{LPF} \cdot C_{LPF}}$$

$$Z_{LPF} \approx 3\,k\Omega$$

Transfer:

$I_{D1} \cdot\cdot I_{D4}$, V_{HF}, $\overline{DODS}$ ⟶ $\overline{TL}$, $\overline{PLLH}$, LF AGC

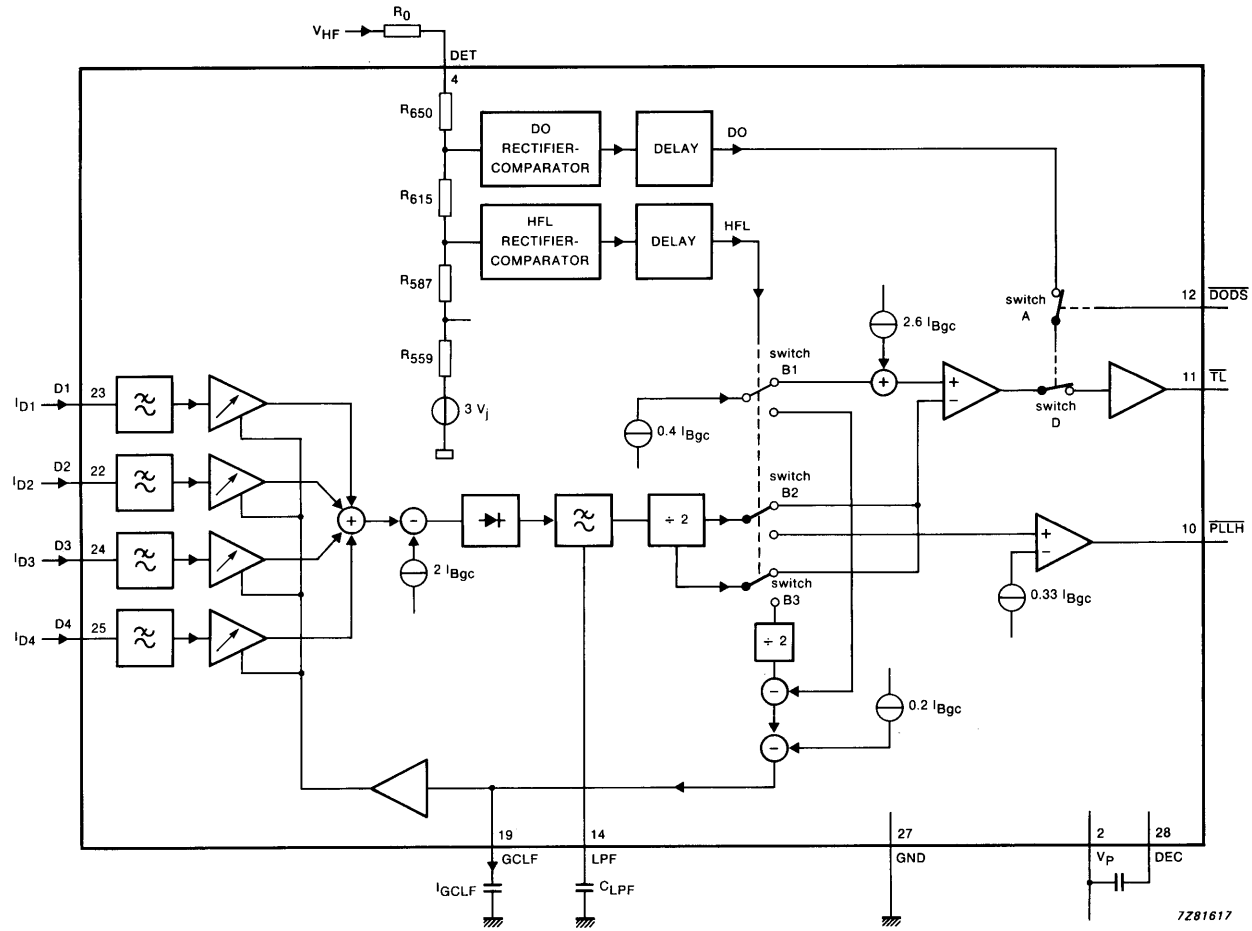


Fig. 9 Transfer function from ($I_{D1} + I_{D2} + I_{D3} + I_{D4}$) to the gain control low frequency input (GCLF) with I_{DET} as parameter.

Table 2 Transfer function from $(I_{D1} + I_{D2} + I_{D3} + I_{D4})$ to GCLF with I_{DET} as parameter

DET input	low frequency input signal	GCLF output	LF AGC loop
$\lvert V_{HF}\rvert < 5/8\ V_{ref}$		$I_{GCLF} = -0{,}2\ I_{Bgc}$	open
$\lvert V_{HF}\rvert > 5/8\ V_{ref}$	$(I_{D1} + I_{D2} + I_{D3} + I_{D4}) \cdot G3 \cdot G4 < 2 \cdot I_{Bgc}$	$I_{GCLF} = -0{,}6\ I_{Bgc}$	open
$\lvert V_{HF}\rvert > 5/8\ V_{ref}$	$(I_{D1} + I_{D2} + I_{D3} + I_{D4}) \cdot G3 \cdot G4 > 2 \cdot I_{Bgc}$	$I_{GCLF} = -I^{(1)}$	closed

Where:

$$(1)\ I = \left(\frac{\{(I_{D1} + I_{D2} + I_{D3} + I_{D4}) \cdot G3 \cdot G4\} - 2I_{Bgc}}{4} \right) \cdot G5 - 0{,}6\ I_{Bgc}$$

$$G3 = k_1 \cdot \frac{V_{GCLF} - 2\ V_j}{3 \cdot R_{171} \cdot \frac{V_{gap}}{R_{922}}} \text{ with } 0 < \frac{V_{GCLF} - 2\ V_j}{3 \cdot R_{171} \cdot \frac{V_{gap}}{R_{922}}} \leqslant 1$$

$$G4 = \frac{1}{1 + (S/\omega_1)}$$

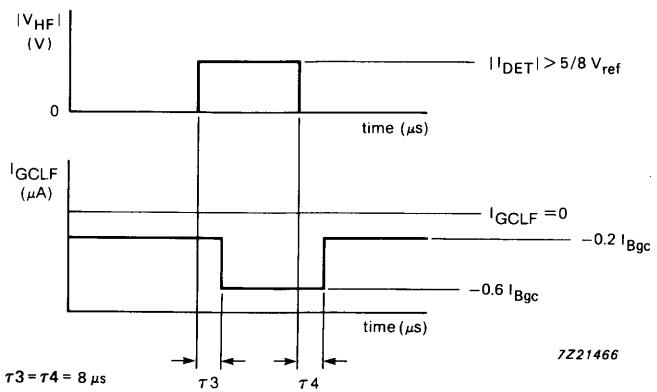
$$G5 = \frac{1}{1 + (S/\omega_2)}$$

k_1 = fixed, typical 64 times

With LF AGC loop closed:

$(I_{D1} + I_{D2} + I_{D3} + I_{D4}) \cdot G3 \cdot G4 \cdot G5$ is regulated to (cfr on track) $4{,}4\ I_{Bgc}$.

The influence of the delay circuits on the transfer function; $(I_{D1} + I_{D2} + I_{D3} + I_{D4})$ to GCLF is shown in Fig. 10.



Test condition: $(I_{D1} + I_{D2} + I_{D3} + I_{D4}) \cdot G3 \cdot G4 < 2 \cdot I_{Bgc}$.

Fig. 10 Delay times between I_{DET} and I_{GCLF}.

Transfer function $\overline{TL}$, $\overline{PLLH}$ outputs with V_{HF}, I_{D1}, I_{D2}, I_{D3} and I_{D4} as variables with V_{GCLF} and $\overline{DODS}$ as parameters (see Fig. 9).

Transfer function $\overline{TL}$

$\overline{DODS}$ = HIGH

$\overline{TL}$ = 0 (approximately GND) if;
$1/8\ V_{ref} < |V_{HF}| < 5/8\ V_{ref}$
and
$(I_{D1} + I_{D2} + I_{D3} + I_{D4}) \cdot G3 \cdot G4 \cdot G5 > 5 \cdot I_{Bgc}$.

$\overline{DODS}$ = LOW

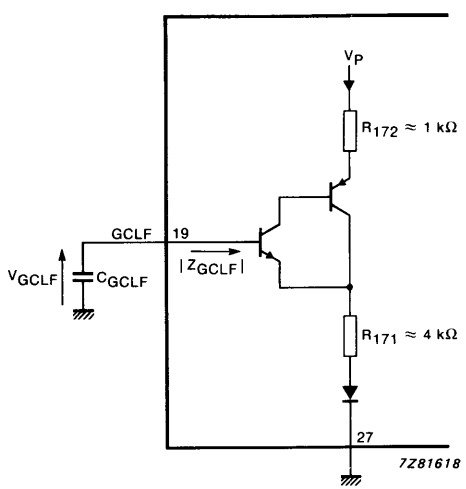
$\overline{TL}$ = 0 if;
$|V_{HF}| < 5/8\ V_{ref}$
and
$(I_{D1} + I_{D2} + I_{D3} + I_{D4}) \cdot G3 \cdot G4 \cdot G5 > 5 \cdot I_{Bgc}$.

Transfer function $\overline{PLLH}$

$\overline{PLLH}$ = 0 if;
$|V_{HF}| < 5/8\ V_{ref}$
or

$$|V_{HF}| < 5/8\ V_{ref} \text{ and } G5\ \frac{(I_{D1} + I_{D2} + I_{D3} + I_{D4}) \cdot G3 \cdot G4 - 2I_{Bgc} < 0{,}33 I_{Bgc}}{2}$$

Input impedance of the LF gain control input



$|Z_{GCLF}| \approx 25\ M\Omega$.

Fig. 11 GCLF equivalent input circuit.

DEVELOPMENT DATA

Transfer function from diode inputs D1, D2, D3, D4 and voltage input V_{Sc} to outputs FE and FElag

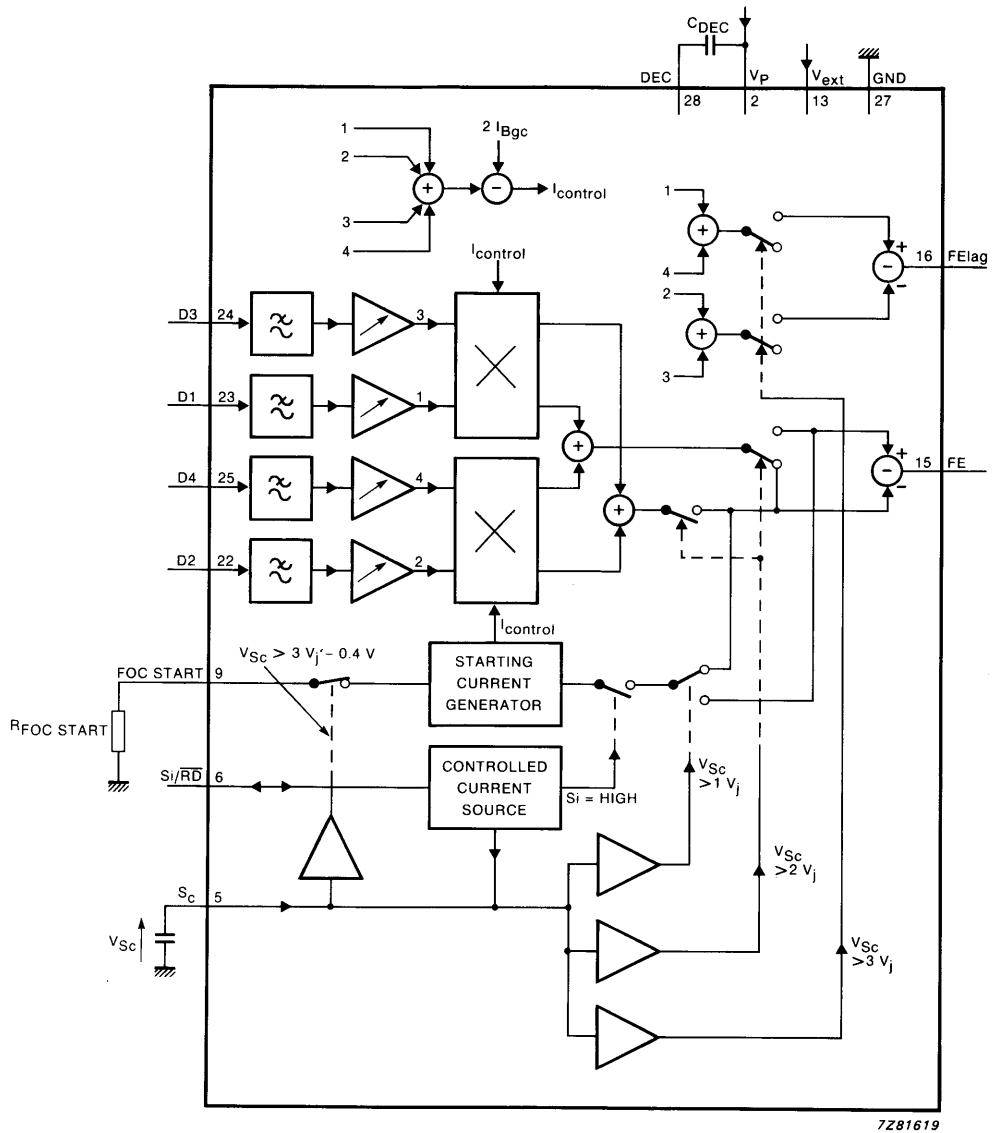


Fig. 12 Block diagram; photo diode inputs to FE and FElag outputs.

The transfer function from I_{D1}, I_{D2}, I_{D3}, I_{D4} to FElag output with V_{Sc} as parameter is given by the following formula (see also Fig. 14).

$$I_{FElag} = G3 \cdot G4 \cdot \frac{1 + \tan h \left(\frac{V_{Sc} - 3\,V_j}{2V_T} \right)}{2_2} \cdot [(I_{D1} + I_{D4}) - (I_{D2} + I_{D3})]$$

Note

Since $\tan h \frac{V_{Sc} - 3\,V_j}{2V_T} \approx -1$ for $V_{Sc} - 3\,V_j \leqslant -150$ mV

and $\tan h \frac{V_{Sc} - 3\,V_j}{2V_T} \approx +1$ for $V_{Sc} - 3\,V_j \geqslant +150$ mV

this means

FElag = 0 for $V_{Sc} - 3\,V_j \leqslant -150$ mV and

FElag = $G3 \cdot G4 \cdot \{ (I_{D1} + I_{D4}) - (I_{D2} + I_{D3}) \}$ for $V_{Sc} - 3\,V_j \geqslant 150$ mV

In practice we see a smooth take over from FElag = 0 to FElag (nominal value) with respect to the voltage V_{Sc}.

Remark:

Si/$\overline{RD}$ not forced LOW.

DEVELOPMENT DATA

The transfer function from I_{D1}, I_{D2}, I_{D3}, I_{D4} to FE output with V_{Sc} as parameter is given by the following formula (see also Fig. 14).

$$I_{FE} = I_{start} \cdot \left[\tanh \left(\frac{V_{Sc} - 1\,V_j + \frac{I_{start}\,(R_{439} - R_{440})}{2}}{2\,V_T + \frac{I_{start}\,(R_{439} + R_{440})}{2}} \right) + \frac{1}{2} + \frac{1}{2} \tanh \left(\frac{V_{Sc} - 3\,V_j - I_{int} \cdot R_{448}}{2\,V_T} \right) \right] +$$

$$I_{control} \left[\frac{(I_{D1} - \frac{I_{D2}}{2}) \tanh (\frac{V_{Sc} - 2\,V_j}{2\,V_T}) - \frac{I_{D2}}{2}}{I_{D1} + I_{D2}} + \right.$$

$$\text{---------- normalized current ----------}$$

$$\left. \frac{(I_{D4} - \frac{I_{D3}}{2}) \tanh \left(\frac{V_{Sc} - 2\,V_j}{2\,V_T} \right) - \frac{I_{D3}}{2}}{I_{D3} + I_{D4}} \right] +$$

$$\text{------- normalized current -------}$$

$$G3 \cdot G4 \cdot \frac{1}{2} \cdot \left[\tanh \left(\frac{V_{Sc} - 3\,V_j}{2\,V_T} \right) - 1 \right] \cdot (I_{D2} + I_{D3})$$

$$\text{-------- not normalized current --------}$$

which means if:

$$0 < V_{Sc} < 1\,V_j - 250\,mV \rightarrow I_{FE} = -I_{start} - I_{control} \left(\frac{I_{D1}}{I_{D1} + I_{D2}} + \frac{I_{D4}}{I_{D3} + I_{D3}} \right) - G3 \cdot G4 \cdot (I_{D2} + I_{D3})$$

$$1\,V_j + 250\,mV < V_{Sc} < 2\,V_j - 100\,mV \rightarrow I_{FE} = I_{start} - I_{control} \left(\frac{I_{D1}}{I_{D1} + I_{D2}} + \frac{I_{D4}}{I_{D3} + I_{D4}} \right) - G3 \cdot G4 \cdot (I_{D2} + I_{D3})$$

$$2\,V_j + 100\,mV < V_{Sc} < 3\,V_j - 100\,mV \rightarrow I_{FE} = I_{start} - I_{control} \left(\frac{I_{D1} - I_{D2}}{I_{D1} + I_{D2}} + \frac{I_{D4} - I_{D3}}{I_{D3} + I_{D4}} \right) - G3 \cdot G4 \cdot (I_{D2} + I_{D3})$$

$$V_{Sc} > 3\ V_j - 100\ mV \rightarrow I_{FE} = I_{control}\left(\frac{I_{D1} - I_{D2}}{I_{D1} + I_{D2}} + \frac{I_{D4} - I_{D3}}{I_{D3} + I_{D4}}\right)$$

Where:

I_{start} (focus start current) is related to R_{FS} (resistor determining the focus start current). The relationship is shown by the following formula:

$$R_{FS} = \frac{V_T}{I_{start}} \text{Ln} \frac{\frac{V_{gap}}{R_{922}}}{I_{start}} + \frac{R_{444} \cdot \frac{V_{gap}}{R_{922}}}{I_{start}} \approx \frac{0{,}56\ V}{I_{start}}$$

R_{439} = integrated resistor 700 Ω (typ.).
R_{440} = integrated resistor 300 Ω (typ.).
R_{444} = integrated resistor 5,5 kΩ (typ.).
R_{448} = integrated resistor 4,0 kΩ (typ.).
R_{922} = integrated resistor 12 kΩ (typ.).

$\Sigma = \frac{V_{gap}}{R_{922}} \cdot R_{448} = I_{int} \cdot R_{448} \approx 0{,}4$ V.

$I_{control} = (I_{D1} + I_{D2} + I_{D3} + I_{D4}) \cdot G3 \cdot G4$ for
$(I_{D1} + I_{D2} + I_{D3} + I_{D4}) \cdot G3 \cdot G4 \leqslant 2 \cdot I_{Bgc}$
otherwise $I_{control} = 2 \cdot I_{Bgc}$ (see also Fig. 13).

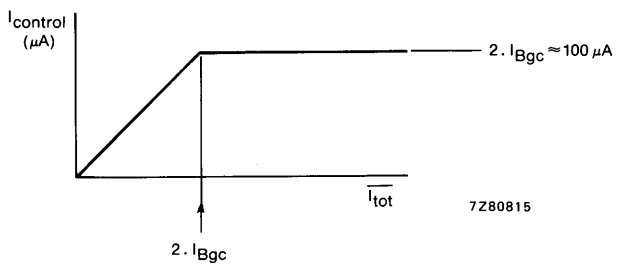


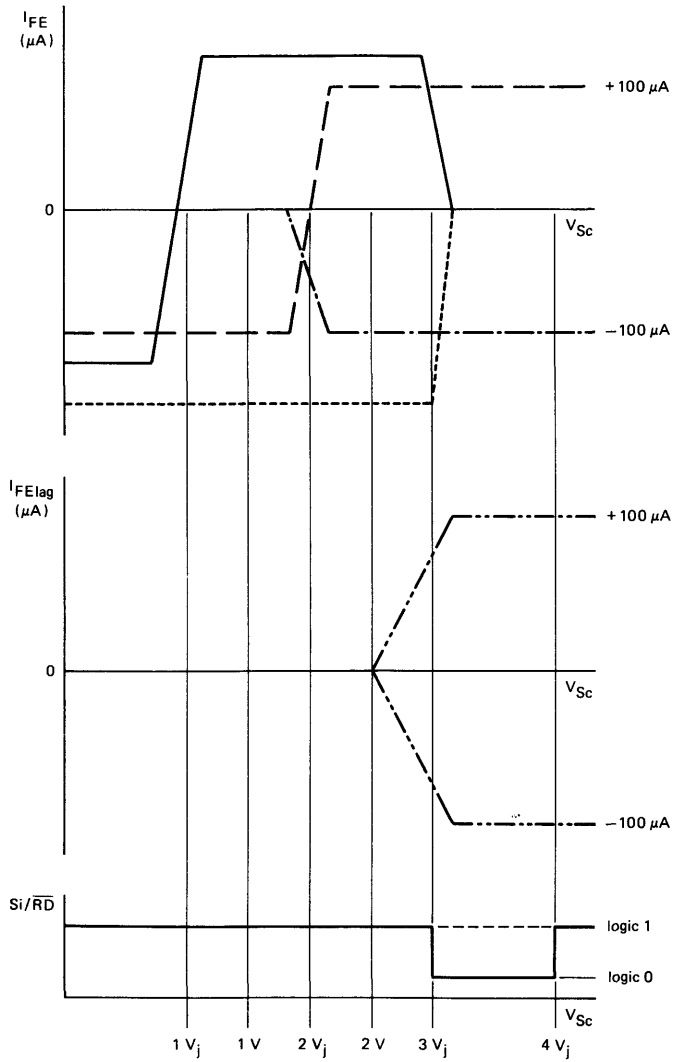
Fig. 13 $I_{control}$ as a function of $\overline{I_{tot}}$.

$\overline{I_{tot}} = (I_{D1} + I_{D2} + I_{D3} + I_{D4}) \cdot G3 \cdot G4.$

Remark:

Si/$\overline{RD}$ = not forced LOW

DEVELOPMENT DATA



Where:

LF amplifier gain	= 64
I_D	= 1 μA
I_{start}	= 110 μA
————	= I_{start}
— — —	= (I_{D1} + I_{D4}) normalized current
— · — · —	= (I_{D2} + I_{D3}) normalized current
— ·· — ·· —	= (I_{D1} + I_{D4}) · G3 · G4 not normalized current
– – – – – –	= (I_{D2} + I_{D3}) · G3 · G4 not normalized current

Fig. 14 I_{FE}, I_{FElag} and Si/$\overline{RD}$ as a function of V_{Sc} (asymtotes shown).

DEVELOPMENT DATA

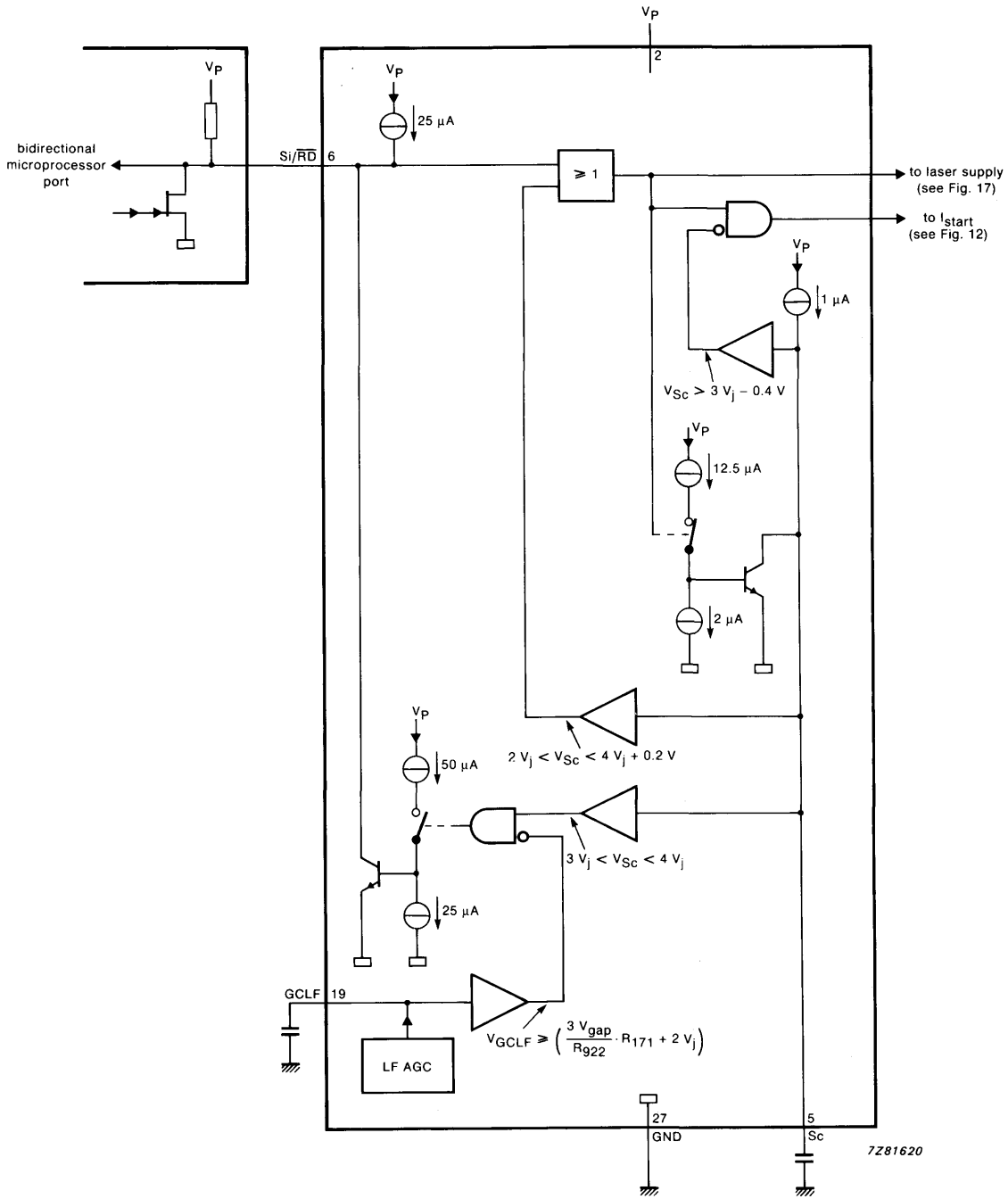


Fig. 15 Transfer function from Si/$\overline{RD}$ to V_{Sc} and V_{GCLF}.

The condition $V_{GCLF} \leqslant \frac{3\,V_{gap}}{R_{922}} \cdot R_{171} + 2\,V_j$ is fulfilled (from a system point of view) if:

$|V_{DET}| \geqslant 0{,}625\,V_{ref}$ and $(I_{D1} + I_{D2} + I_{D3} + I_{D4}) \cdot k_1 - 2I_{Bgc} \geqslant 2{,}4I_{Bgc}$

This means that:

- Si/$\overline{RD}$ will only go LOW (ready = true) if the LF AGC is in its active range
- HF must be present; motor must be running

Between $V_{Sc} = 2\,V_j$ and $V_{Sc} = 4\,V_j + 200$ mV the Si/$\overline{RD}$ line is not monitored by the IC. This means that stopping the start procedure is impossible within this range.

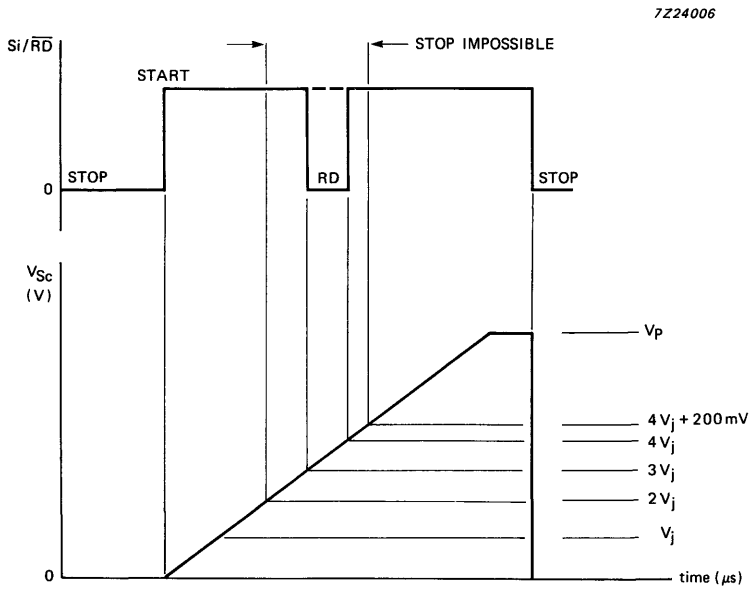


Fig. 16 Si/$\overline{RD}$ signal as a function of V_{Sc} and time.

Transfer function laser supply

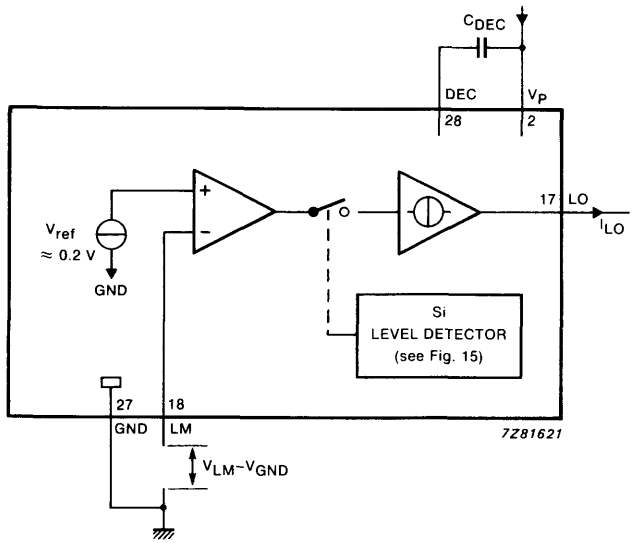


Fig. 17 Block diagram; laser supply.

Laser supply transconductance for DC

$$G_{LDC} = \frac{\Delta I_{LO}}{\Delta V_{LM}} (0 < -I_{LO} < 2\ mA) \approx 0{,}5\ A/V.$$

Laser supply transconductance for AC

$$G_{LAC} = G_{LDC} \cdot \frac{1}{1 + S\tau 11}$$

Where:

$\tau 11$ = fixed with external compensation capacitor (C_{comp})

$$\tau 11 = (Z_{LO} \,//\, Z_{pi}) \cdot C_{comp}.$$

Where:

Z_{LO} = laser amplifier output impedance ≈ 95 kΩ
Z_{pi} = power stage input impedance

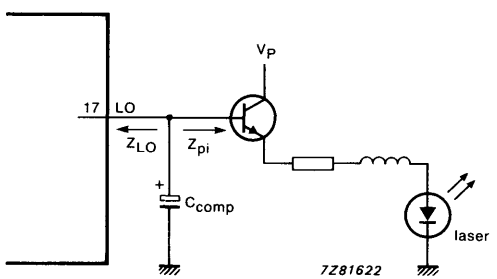


Fig. 18 Laser amplifier output circuitry.

RADIAL ERROR SIGNAL PROCESSOR FOR COMPACT DISC PLAYERS

GENERAL DESCRIPTION

The TDA8809T is a bipolar integrated circuit which provides control signals for the radial motor. These control signals are generated from radial error signals received from a photo-diode signal processor (TDA8808), and velocity control signals from the control processor.

Features

- Tracking error processor with automatic asymmetry control
- AGC circuitry with automatic start-up and wobble generator
- Tracking control for fast forward/reverse scan, search, repeat and pause functions
- Radial polarity - 4 - tracks counting
- Possibility for car, home and portable applications

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range						
pin 12		$V_{ext(+)}$	V_P	10	12	V
pin 13		$V_{ext(-)}$	−5,5	−5,0	0	V
pin 12 to pin 13		$V_{ext(+)} - V_{ext(-)}$	4,5	–	12	V
Supply current		I_P	–	5,3	–	mA
Operating ambient temperature range		T_{amb}	−30	–	+85	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

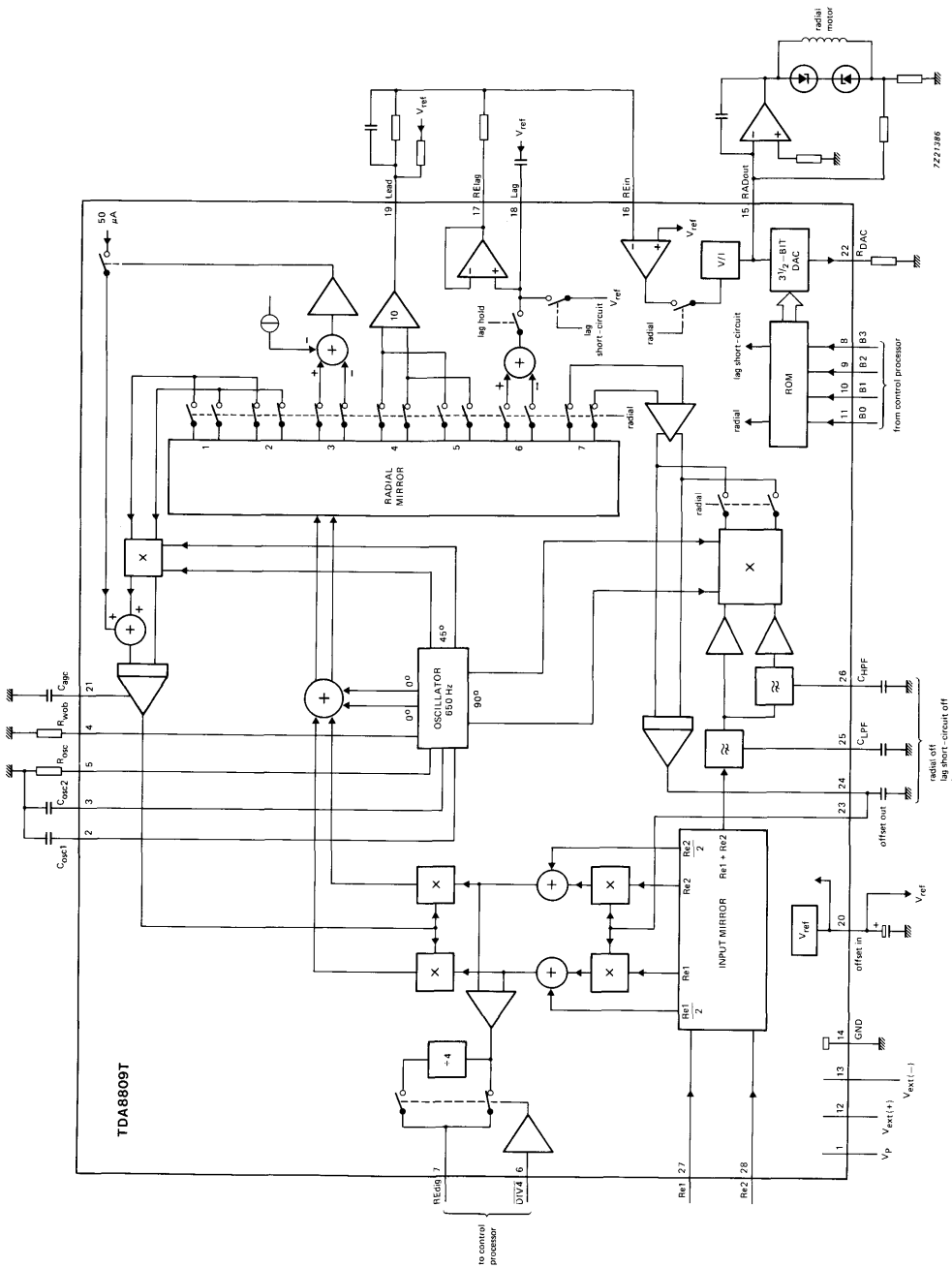


Fig. 1 Block diagram.

PINNING

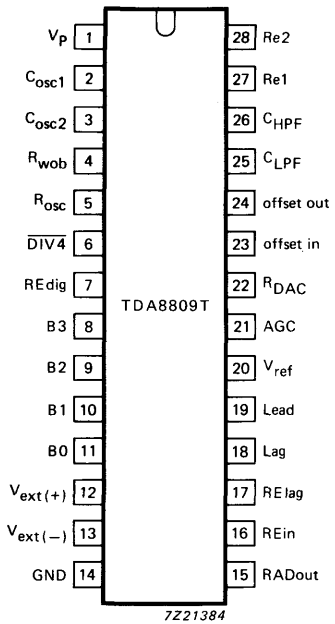


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

Pin functions

pin	mnemonic	description
1	V_P	Positive supply voltage
2	C_{osc1}	Frequency setting capacitors for oscillator
3	C_{osc2}	
4	R_{wob}	Wobble generator input
5	R_{osc}	Biassing resistor for oscillator frequency and internal amplitude
6	$\overline{DIV4}$	Divide-by-4 input
7	REdig	Digital output of sign (Re2 - Re1)
8	B3	Input control bits for off-, catch-, play-status and DAC output current
9	B2	
10	B1	
11	B0	
12	$V_{ext(+)}$	Positive external voltage input
13	$V_{ext(-)}$	Negative external voltage input (also substrate connection)
14	GND	Negative supply connection
15	RADout	Current output of amplified (Re2 - Re1) input currents
16	REin	Radial error input
17	RElag	Voltage output of integrated (Re2 - Re1) input currents
18	Lag	Connection of integrator capacitor for (Re1 - Re2) input currents
19	Lead	Lead output
20	V_{ref}	Internal reference voltage output
21	AGC	Gain control input for radial error signal
22	R_{DAC}	Biassing resistor for current output for track jumping (3½ bits)
23	offset in	Offset control input for radial offset
24	offset out	Offset control output for radial offset
25	C_{LPF}	Low-pass filter for Re1 and Re2, used for radial offset control
26	C_{HPF}	High-pass filter for Re1 and Re2, used for radial offset control
27	Re1	Input for amplified currents from photo-diodes D1 and D2
28	Re2	Input for amplified currents from photo diodes D3 and D4

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage ranges (see Fig. 3)				
pin 1 to pin 14	V_P	−0,3	13	V
pin 12 to pin 13	V_{ext}	−0,3	13	V
pin 14 to pin 13	$V_{ext(-)}$	−0,3	13	V
Output voltage ranges				
except RADout	V_O	0	V_P	V
RADout	V_O	$V_{ext(-)}$	$V_{ext(+)}$	V
R_{DAC} current range	I_{RDAC}	50	250	μA
Total power dissipation	P_{tot}	see Fig. 4		
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	−30	+85	°C
Operating junction temperature	T_j	−	150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 140 K/W

DEVELOPMENT DATA

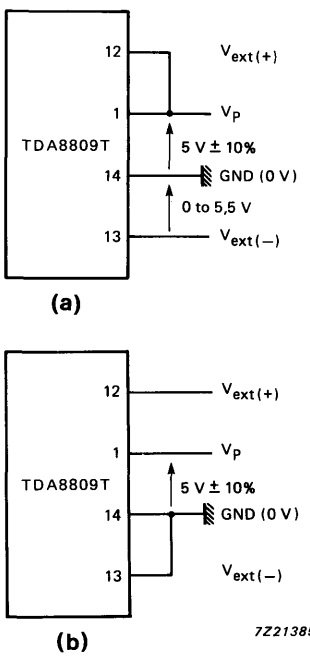


Fig. 3 Supply voltages;
(a) Home application (b) Car application.

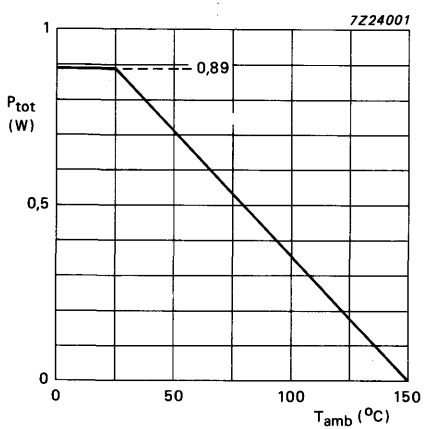


Fig. 4 Power derating curve.

CHARACTERISTICS

V_P = + 5 V; V_{GND} = 0 V; $V_{ext(+)}$ = + 5 V; $V_{ext(-)}$ = −5 V; I_{RDAC} (pin 22) = −75 μA; I_{Rwob} (pin 4) = −8 μA; I_{Rosc} (pin 5) = −50 μA; V_{RADout} = 0 V; $V_{offset\ in}$ = V_{lead} = V_{lag} = V_{Cosc1} = V_{Cosc2} = V_{ref}; $V_{offset\ in}$ is connected to $V_{offset\ out}$; T_{amb} = 25 °C; all voltages measured with respect to V_{GND}; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range (see Fig. 3)						
pin 12		$V_{ext(+)}$	V_P	10	12	V
pin 13		$V_{ext(-)}$	−5,5	−5,0	0	V
pin 12 to pin 13		$V_{ext(+)} - V_{ext(-)}$	4,5	–	12	V
Supply current		I_P	4,0	5,3	6,6	mA
Reference output (V_{ref})						
Output voltage	$\lvert I_{Vref} \rvert \leqslant \pm 1$ mA	V_{ref}	2,25	2,45	2,65	V
Output impedance		$\lvert Z_O \rvert$	–	25	–	Ω
Reference input (R_{osc})						
Input voltage level	I_{Rosc} = −50 μA	V_{Rosc}	1,1	1,24	1,3	V
Input current		I_{Rosc}	–	−50	–	μA
Reference input (R_{DAC})						
Input voltage level	I_{RDAC} = −75 μA	V_{RDAC}	1,1	1,23	1,3	V
Input current		I_{RDAC}	–	−75	–	μA
Reference input (R_{wob})						
Input voltage level	I_{Rwob} = −8 μA	V_{Rwob}	150	165	180	mV
Input current		I_{Rwob}	–	−8	–	μA
REdig output (REdig)						
Output source current	note 1 (A)	I_{REdig}	–	−160	−50	μA
Output sink current	note 1 (B)	I_{REdig}	0,4	3,5	–	mA
Output voltage HIGH	I_{REdig} = −50 μA; note 1 (A)	V_{REdig}	2,4	–	–	V
Output voltage LOW	I_{REdig} = 400 μA; note 1 (B)	V_{REdig}	0	0,13	0,4	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Digital inputs						
B0, B1, B2 and B3						
Input voltage HIGH	note 2	V_{IH}	2,0	–	V_P	V
Input voltage LOW	note 2	V_{IL}	0	–	0,8	V
Input sink current HIGH		I_{IH}	0	0,03	1,0	μA
Input source current LOW		I_{IL}	–3,0	–0,1	0	μA
Divide-by-4 input ($\overline{DIV4}$)						
Input voltage HIGH	divide-by-1	V_{IH}	2,0	–	V_P	V
Input voltage LOW	divide-by-4	V_{IL}	0	–	0,8	V
Input sink current HIGH		I_{IH}	0	5,0	*	μA
Input source current LOW		I_{IL}	–10	–3	0	μA
Input frequency at Re1 and Re2		f_i	–	10	50	kHz
Radial error inputs (Re1; Re2)						
Input voltage level	$I_{Re1} = I_{Re2} = -110\,\mu A$	V_{Re1}, V_{Re2}	$V_P-1,81$	$V_P-1,71$	$V_P-1,61$	V
Input current		I_{Re1}, I_{Re2}	–	–110	–	μA
Input impedance		$\lvert Z_{Re1}\rvert, \lvert Z_{Re2}\rvert$	–	2,5	–	kΩ
Gain control input (AGC)	rad on; lag hold off					
Offset current	$V_{AGC} = 3,8$ V; $I_{Re1} = I_{Re2} = 0$	I_{AGC}	–0,2	0	0,2	μA
Lag current for	$I_{Re1} = -85\,\mu A$; $I_{Re2} = -115\,\mu A$					
minimum radial gain	$V_{AGC} = 0,6$ V	I_{lag}	–2,5	–0,45	+ 1,5	μA
maximum radial gain	$V_{AGC} = 3,8$ V	I_{lag}	–42	–30	–18	μA
Input impedance		$\lvert Z_{AGC}\rvert$	–	*	–	MΩ
Gain	$V_{AGC} = 3,8$ V; $V_{Cosc2} = V_{ref} + 1,4$ V; $V_{Cosc1} = V_{ref}$; $I_{Re1} = -100\,\mu A$; $I_{Re2} = -100\,\mu A$	I_{AGC0}	–	–2	–	μA
	$I_{Re1} - I_{Re2} = 4\,\mu A$ – I_{AGC0} then $I_{Re1} - I_{Re2} = -4\,\mu A$ – I_{AGC0}	$\frac{\Delta I_{AGC}}{\Delta(I_{Re1}-I_{Re2})}$	0,7	0,9	1,1	

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Gain control (continued)						
Radial error trackcrossing	rad off; V_{AGC} = 3,8 V $I_{Re2}-I_{Re1}$ = −12 μA; $I_{Re2}+I_{Re1}$ = −200 μA	I_{AGC}	−3	0	3	μA
	$I_{Re2}-I_{Re1}$ = −48 μA; $I_{Re2}+I_{Re1}$ = −200 μA	I_{AGC}	39	49	59	μA
Offset control (offset out)						
Offset current	rad on; I_{CHPF} = 0; $I_{Re1}=I_{Re2}$ = −110 μA	$I_{offset\ out}$	−0,1	0	0,1	μA
Offset lag current for	rad on; lag hold off; V_{AGC} = 3,8 V; $I_{Re1}=I_{Re2}$ = −100 μA					
minimum amplification Re1 maximum amplification Re2	$V_{offset\ in}$ = V_{ref} − 1,2 V	I_{lag}	−115	−100	−85	μA
minimum amplification Re2 maximum amplification Re1	$V_{offset\ in}$ = V_{ref} + 1,2 V	I_{lag}	+ 85	+100	+115	μA
Offset lag current	note 3	I_{lag}	−7	0	+ 7	μA
Transconductance factor						
	rad off; V_{AGC} = 3,8 V; $I_{Re1}=I_{Re2}$ = −100 μA; $V_{range\ offset\ in}$ = 0,6 V (int.); $I_{tot}=I_{Re1}+I_{Re2}$	$\frac{\Delta I_{offset\ out}}{\Delta V_{offset\ in}.I_{tot}}.V_{range\ offset\ in}$	0,17	0,21	0,25	
	rad off; $V_{AGC}=V_{GND}$ $I_{Re1}=I_{Re2}$ = −100 μA; $V_{range\ offset\ in}$ = 0,6 V (int.); $I_{tot}=I_{Re1}+I_{Re2}$	$\frac{\Delta I_{offset\ out}}{\Delta V_{offset\ in}.I_{tot}}.V_{range\ offset\ in}$	−0,1	0	0,1	
Input impedance		$\lvert Z_{offset\ in}\rvert$	−	*	−	MΩ
High-pass filter (C_{HPF})						
Voltage level at I_{CHPF} = 0	$I_{Re1}=I_{Re2}$ = 0; I_{CLPF} = 0	V_{CHPF}	V_P −0,82	V_P −0,72	V_P −0,62	V
Transresistance from Re1, Re2 to C_{HPF}	$I_{Re1}+I_{Re2}$ = −200 μA	$\frac{\Delta V_{CHPF}}{\Delta(I_{Re1}-I_{Re2})}$	−200	*	200	Ω
		$\frac{\Delta V_{CHPF}}{\Delta(I_{Re1}+I_{Re2})}$	6,2	8,8	11,5	kΩ
Input impedance		$\lvert Z_{CHPF}\rvert$	−	8	−	kΩ

* Value to be fixed.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Low-pass filter (C_{LPF})						
Voltage level at $I_{CLPF} = 0$	$I_{Re1} = I_{Re2} = 0$	V_{CLPF}	4,7	–	V_P	V
Input impedance		$\lvert Z_{CLPF} \rvert$	–	8	–	kΩ
RElag output						
Output voltage range	$I_{RElag} = -200\ \mu A$; $V_{lag} = 4{,}25$ V	V_{RElag}	$V_P-1{,}1$	–	–	V
	$I_{RElag} = 200\ \mu A$; $V_{lag} = 0{,}9$ V	V_{RElag}	–	–	1,1	V
Maximum source current output	$V_{lag} = 4{,}1$ V	I_{RElag}	–6,0	–3,5	–1,0	mA
Maximum sink current output	$V_{lag} = 0{,}9$ V	I_{RElag}	2,5	4,1	5,5	mA
Output impedance	f = < 10 kHz	$\lvert Z_{RElag} \rvert$	–	–	50	Ω
Offset ($V_{RElag}-V_{ref}$)	lag short-circuit on; lag hold on	$V_{RElag\ offset}$	–10	–	10	mV
Transfer lag ⟶ RElag	f = < 10 kHz; lag short-circuit off; lag hold on	$\frac{V_{RElag}}{V_{lag}}$	–5%	1	5%	
Slew rate						
RElag output amplifier	lag short-circuit off; lag hold on	SR	–	0,4	–	V/μs
Lag push-pull current output, voltage input (pin 18)	note 4					
Output voltage	$I_{lag} = -20\ \mu A$; $V_{offset\ in} = V_{ref}-1{,}2$ V	V_{lag}	$V_P-1{,}5$	–	–	V
	$I_{lag} = 20\ \mu A$; $V_{offset} = V_{ref} + 1{,}2$ V	V_{lag}	–	–	1,5	V
Output impedance		$\lvert Z_{lag} \rvert$	–	*	–	MΩ
Switch lag short-circuit						
Impedance $\frac{\Delta V_{lag}}{\Delta I_{lag}}$	lag short-circuit on; lag hold on; $I_{lag} = \pm 100\ \mu A$	$\lvert Z_{lag\ sc} \rvert$	–	0,4	1	kΩ
Radial error input (REin)						
Input impedance	rad on	$\lvert Z_{REin} \rvert$	–	0	–	kΩ

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
RADout push-pull current output						
Output voltage	rad on I_{REin} = 180 μA; I_{RADout} = −50 μA	V_{RADout}	$V_{ext(+)}$−1,5	−	−	V
	I_{REin} = −180 μA; I_{RADout} = 50 μA	V_{RADout}	−	−	$V_{ext(-)}$+1,5	V
Current gain	rad on; I_{REin} = ± 100 μA	$\frac{I_{RADout}}{I_{REin}}$	−10%	1	10%	
Slew rate		SR	−	0,4	−	V/μs
Output impedance		$\lvert Z_{RADout} \rvert$	−	*	−	MΩ
Ratio of output current to reference current	I_{REin} = 0; I_{RDAC} = −75 μA; see also Table 1	$\frac{I_{RADout}}{I_{RDAC}}$	−5%	−0,5	+ 15%	
			−8%	−2	+ 12%	
			−0,02	0	0,02	
			−0,02	0	0,02	
			−14%	0,5	+ 6%	
			−12%	2	+ 8%	
			−0,1	0	0,1	
			−0,1	0	0,1	
			−5%	−0,5	+ 15%	
			−5%	−0,375	+ 15%	
			−5%	−0,25	+ 15%	
			−4%	−0,125	+ 16%	
			−14%	+ 0,5	+ 6%	
			−13%	+ 0,375	+ 7%	
			−13%	+ 0,25	+ 7%	
			−13%	+ 0,125	+ 7%	
Lead output	V_{AGC} = 3,8 V					
Output voltage	I_{Re1} = −90 μA; I_{Re2} = −100 μA; I_{lead} = −20 μA	V_{lead}	V_P−1,5	−	−	V
	I_{Re1} = −100 μA; I_{Re2} = −90 μA; I_{lead} = 20 μA	V_{lead}	−	−	1,5	V
Offset current	$I_{Re1} = I_{Re2}$ = −100 μA	$I_{lead\ off}$	−100	0	100	μA

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Lead output (continued)						
Current gain	$I_{Re1} = -120\ \mu A$; $I_{Re2} = -100\ \mu A$	$\frac{\Delta I_{lead}}{\Delta(I_{Re1}-I_{Re2})}$	−11,2	−9,9	−8,8	
Output impedance		$\lvert Z_{lead}\rvert$	–	*	–	MΩ
Oscillator						
(C_{osc1} and C_{osc2} connected to 12 nF capacitors)						
Amplitude oscillation (peak-to-peak value)						
C_{osc1}		$V_{osc1(p-p)}$	1,05	1,25	1,45	V
C_{osc2}		$V_{osc2(p-p)}$	1,05	1,25	1,45	V
Operating frequency	$I_{Re1} = I_{Re2} = -110\ \mu A$	f_{osc}	690	740	790	Hz
Output voltages (peak-to-peak value)						
0° injection						
lead (pin 19)	$R_{lead} = 10\ k\Omega$	$V_{lead(p-p)}$	0,85	1,05	1,25	V
C_{lag} (pin 18)	$R_{lag} = 10\ k\Omega$; rad on; lag hold off	$V_{lag(p-p)}$	85	105	125	mV
	rad on; lag hold on	$V_{lag(p-p)}$	–	0	20	mV
90° injection						
offset out	$I_{CHPF} = -100\ \mu A$; $R_{offset\ out} = 10\ k\Omega$; rad on	$V_{offset\ out}$ (p-p)	90	110	130	mV
45° injection						
AGC	$R_{agc} = 10\ k\Omega$; $V_{offset\ in} = V_{ref} + 1\ V$; rad on	$V_{AGC(p-p)}$	200	250	300	mV

Notes to the characteristics

1. REdig output conditions:
   (A) $I_{Re1} > I_{Re2} + 5\ \mu A$; (B) $I_{Re2} > I_{Re1} + 5\ \mu A$.
2. Input voltage HIGH indicates logic 1; Input voltage LOW indicates logic 0; see also Table 1.
3. $\overline{DIV4}$ = HIGH; $V_{offset\ in}$ adjusted for $V_{REdig} = 1,4$ V; rad on; lag hold off; $V_{AGC} = 3,8$ V; $I_{Re1} = I_{Re2} = -100\ \mu A$.
4. Output voltage conditions are:
   rad on; lag short-circuit off; lag hold off; $V_{AGC} = 3,8$ V; $I_{Re1} = I_{Re2} = -100\ \mu A$; $V_{offset} = V_{ref} - 1,2$ V.

DEVELOPMENT DATA

Table 1 Truth table for DAC output current

functions	DAC output	logical inputs				internal switches		
	I_{REout}/I_{DAC}	B3	B2	B1	B0	lag s/c	rad	lag hold
PUSH	−1/2	0	0	0	0	off	off	on
(kick)	−2	0	0	0	1	off	off	off
OFF	0	0	0	1	0	off	off	on
OFF	0	0	0	1	1	on	off	off
PULL	1/2	0	1	0	0	off	off	on
(kick)	2	0	1	0	1	off	off	off
CATCH	0	0	1	1	0	off	on	on
PLAY	0	0	1	1	1	off	on	off
PUSH	−1/2	1	0	0	0	on	off	on
PUSH	−3/8	1	0	0	1	on	off	off
PUSH	−1/4	1	0	1	0	on	off	on
PUSH	−1/8	1	0	1	1	on	off	off
PULL	1/2	1	1	0	0	on	off	on
PULL	3/8	1	1	0	1	on	off	off
PULL	1/4	1	1	1	0	on	off	on
PULL	1/8	1	1	1	1	on	off	off

Where:

0 = input voltage LOW; 1 = input voltage HIGH.

TRANSFER FUNCTIONS OF THE TDA8809

GENERAL

A description of several transfer functions is given on the following pages. These transfer functions will provide application engineers with a full understanding of the operation of the integrated circuit. A number of general parameters are used to aid the explanation. Their given values are typical. Tolerance values are detailed in the TDA8809 data sheet.

General parameters

parameter	description
V_j	junction voltage, 0,7 V at T_{amb} = 25 °C; temperature coefficient approximately −2 mV/°C
V_T	$V_T = \frac{k \cdot T}{q}$ = 25,86 mV at 300 K where: k = Boltzman constant T = absolute temperature q = charge of one electron
I_{int}	internal reference current (100 μA, typ.), which has a negative temperature coefficient $I_{int} = \frac{V_{gap}}{R_{12}}$
I_{osc}	internal reference current (50 μA, typ.), externally fixed by resistor R_{osc} This current is temperature independent
I_1	internal reference current (50 μA, typ.) This current is temperature independent
V_{ref}	internal reference voltage source This voltage is equal to 2 x V_{gap} (2,4 V, typ.)
V_{gap}	internal reference voltage source (1,2 V, typ.) This voltage is temperature independent

Reference currents (I_{int}, I_{osc})
Reference voltages (V_{gap}, V_{ref})

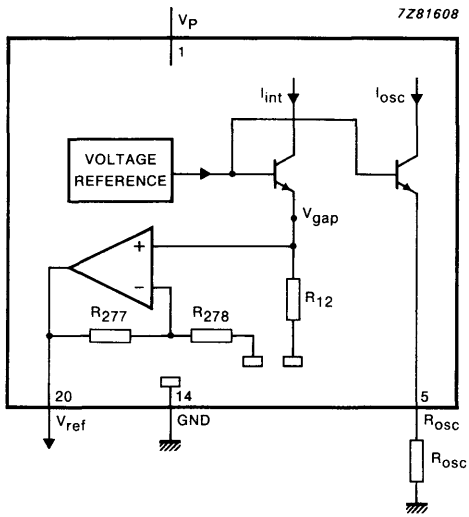


Fig. 1 Block diagram; reference currents I_{int}, I_{osc}; reference voltages V_{gap}, V_{ref}.

Where:

Voltage reference level = V = 1,2 V

$$I_{int} = \frac{V_{gap}}{R_{12}} \approx \frac{1{,}2\ V}{R_{12}} \qquad \text{at } R_{12} \approx 12\ k\Omega\ (I_{int} \approx 100\ \mu A)$$

$$I_{osc} = \frac{1{,}2\ V}{R_{osc}} \qquad \text{at } R_{osc} \approx 24\ k\Omega\ (I_{osc} \approx 50\ \mu A)$$

$$V_{ref} = (1 + \frac{R_{277}}{R_{278}}) \times V_{gap} \qquad \text{at } R_{277} \approx R_{278}\ (V_{ref} = 2 \cdot V_{gap})$$

Note

The value of R_{osc} determines the transconductance of the oscillator.

Transfer function of $(I_{Re1} + I_{Re2})$ to V_{LPF} and I_{HPF}

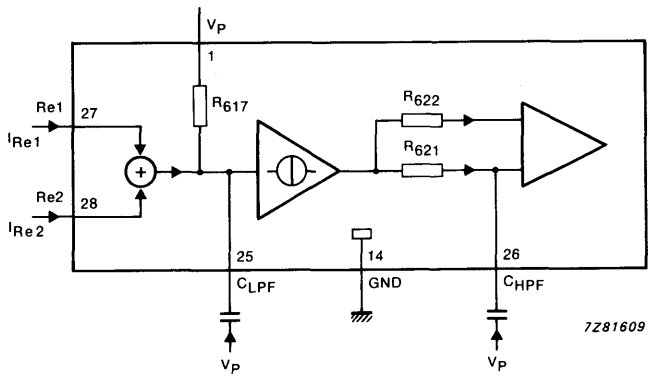


Fig. 2 Block diagram; $(I_{Re1} + I_{Re2})$ to V_{LPF} and I_{HPF}.

$$V_{LPF} = V_{DD} + (I_{Re1} + I_{Re2})\, R_{617} \frac{1}{1 + j\frac{\omega}{\omega_L}}$$

$$I_{HPF} = -\frac{V_{LPF}}{R_{621}} \frac{j\frac{\omega}{\omega_H}}{1 + j\frac{\omega}{\omega_H}} \Rightarrow I_{HPF} = -(I_{Re1} + I_{Re2}) \frac{1}{1 + j\frac{\omega}{\omega_L}} \cdot \frac{j\frac{\omega}{\omega_H}}{1 + j\frac{\omega}{\omega_H}} \cdot \frac{R_{617}}{R_{621}}$$

While $R_{617} \approx R_{621} \Rightarrow$

$$I_{HPF} = -(I_{Re1} + I_{Re2}) \frac{1}{1 + j\frac{\omega}{\omega_L}} \cdot \frac{j\frac{\omega}{\omega_H}}{1 + j\frac{\omega}{\omega_H}}$$

Where:

$$\omega_L = \frac{1}{C_{LPF} \cdot R_{617}}$$

$$\omega_H = \frac{1}{C_{HPF} \cdot R_{621}}$$

R_{621} = integrated resistor 8 kΩ (typ.)

R_{617} = integrated resistor 8 kΩ (typ.)

DEVELOPMENT DATA

Transfer function of I_{Re1}, I_{Re2} to REdig with V_{offset} and digital inputs as parameters

See also block diagram Fig.4.

Table 1 State of the REdig output set by conditions of I_{Re1} and R_{Re2}

condition	REdig output
$I_{Re1} \cdot (1 + \frac{\alpha}{2}) > I_{Re2} \cdot (1 - \frac{\alpha}{2})$	LOW
$I_{Re1} \cdot (1 + \frac{\alpha}{2}) < I_{Re2} \cdot (1 - \frac{\alpha}{2})$	HIGH

with:

$$\alpha = \frac{V_{offset} - V_{ref}}{R_B \cdot I_{int}/2}; \; R_B \cdot I_{int}/2 = (R_{619} + R_{620}) \frac{V_{gap}}{2 \cdot R_{12}} = 0{,}6 \text{ V}$$

$$-1 \leqslant \alpha \leqslant 1$$

DEVELOPMENT DATA

Transfer function of B0, B1, B2, B3 and REin inputs to RADout output

Table 2 Truth table for RADout output current

functions	RADout output	logical inputs				internal switches		
	I_{RADout}	B3	B2	B1	B0	lag s/c	rad	lag hold
KICK-PUSH	$-I_{DAC}$	0	0	0	0	off	off	on*
	$-4 \cdot I_{DAC}$	0	0	0	1	off	off	off*
HOLD-OFF	0	0	0	1	0	off	off	on*
	0	0	0	1	1	on	off	off*
KICK-PULL	I_{DAC}	0	1	0	0	off	off	on*
	$4 \cdot I_{DAC}$	0	1	0	1	off	off	off*
CATCH	$-I_{REin}$	0	1	1	0	off	on	on
PLAY	$-I_{REin}$	0	1	1	1	off	on	off
PUSH	$-I_{DAC}$	1	0	0	0	on	off	on*
PUSH	$-3/4 I_{DAC}$	1	0	0	1	on	off	off*
PUSH	$-1/2 I_{DAC}$	1	0	1	0	on	off	on*
PUSH	$-1/4 I_{DAC}$	1	0	1	1	on	off	off*
PULL	I_{DAC}	1	1	0	0	on	off	on*
PULL	$3/4 I_{DAC}$	1	1	0	1	on	off	off*
PULL	$1/2 I_{DAC}$	1	1	1	0	on	off	on*
PULL	$1/4 I_{DAC}$	1	1	1	1	on	off	off*

Where:

0 = input voltage LOW; 1 = input voltage HIGH.

* = not functional.

$$I_{DAC} = \frac{1}{2} \frac{V_{gap}}{R_{DAC}} = \frac{0{,}6\ V}{R_{DAC}} \text{ typ.}$$

$Z_{REin} \rightarrow 0$; voltage V_{ref}

$Z_{RADout} \rightarrow \infty$; voltage between V_{ext+} and V_{ext-} (minus saturation drop).

Transfer function of C_{osc1}, C_{osc2} and R_{osc} to the generated wobble frequency

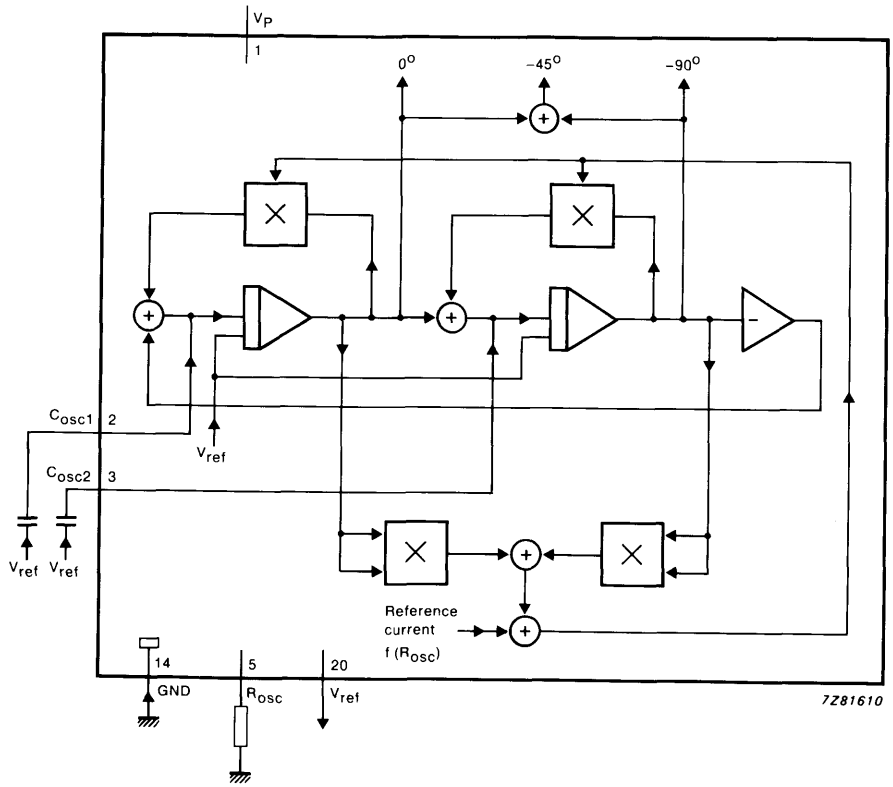


Fig. 3 Block diagram; C_{osc1}, C_{osc2} and R_{osc} to the generated wobble frequency.

$0^o = A \cdot \sin \omega_o t$

$-45^o = A \cdot \sqrt{2} \cdot \sin (-45^o + \omega_o t)$

$-90^o = -A \cos \omega_o t$

Where:

$$\omega_o = \frac{\alpha}{R_{osc}\sqrt{C_{osc1} \cdot C_{osc2}}};$$

$$\alpha = \underbrace{\frac{R_{206} + R_{207}}{R_{206} + R_{207} + re\ (50\ \mu A)}}_{0{,}94} \cdot \sqrt{\underbrace{\frac{R_{12}}{R_{206} + R_{207}} \frac{R_{12}}{R_{306} + R_{307}}}_{3/2}}$$

$$A = \frac{\sqrt{1/2}}{\alpha}\ V_{gap} = 0{,}6\ V$$

$R_{12} = 3 \times 4\ k\Omega$; typ. $R_{206} = R_{207} = R_{306} = R_{307} = 4\ k\Omega$ typ.; $re\ (50\ \mu A) = 500\ \Omega$

Calculation of R_{wob}:

$$\hat{I}_{IN} = \frac{\hat{V}_{osc1} - V_{ref}}{A} \sqrt{\frac{1}{2}} - I_{wob} \Rightarrow I_{wob} = \frac{\hat{I}_{IN}}{\sqrt{\frac{1}{2}}} \frac{A}{\hat{V}_{osc1} - V_{ref}} \Rightarrow I_{wob} = \sqrt{2} \cdot \hat{I}_{IN}$$

$$R_{wob} = \frac{R_{120} - \frac{V_T}{I_{osc}} \text{Ln} \frac{I_{wob}}{I_{osc}}}{\frac{I_{wob}}{I_{osc}}} \Rightarrow$$

$$R_{wob} = \frac{2\,k\Omega - 500\,\Omega \cdot \text{Ln} \frac{I_{wob}}{50\,\mu A}}{\frac{I_{wob}}{50\,\mu A}} \text{ typ. with } I_{wob} = \sqrt{2} \cdot \hat{I}_{IN}$$

DEVELOPMENT DATA

Transfer functions of inputs Re1 and Re2 to output V_{offset} with V_{agc} and R_{osc} as parameters

Table 3 Transfer function of inputs Re1 and Re2 to output V_{offset} with V_{agc} and R_{osc} as parameters

radial switch*	I_{offset}
OFF	$\frac{1}{2}\left[k\left(I_{Re1}\left(1+\frac{\alpha}{2}\right)-I_{Re2}\left(1-\frac{\alpha}{2}\right)\right)+\sqrt{\frac{1}{2}}\cdot I_{wob}\frac{V_{osc1}-V_{ref}}{A}\right]$
ON	$\frac{\cdot 17\,(V_{osc2}-V_{ref})}{R_{207}+R_{208}+re\,(50\,\mu A)}\cdot \tanh\left(\frac{I_{HPF}\cdot R_{621}}{2\cdot V_T}\right)$

Notes to Table 3

- $\alpha=\frac{V_{offset}-V_{ref}}{R_B\cdot\frac{I_{int}}{2}}$; $-1\leqslant\alpha\leqslant 1$
- $k=\frac{V_{agc}-2V_j}{I_{int}\cdot R_{707}}$; $0\leqslant k\leqslant 1$
- $I_{int}\cdot R_{707}=\frac{V_{gap}}{R_{12}}R_{707}=2$ V
- $R_B\cdot\frac{I_{int}}{2}=(R_{619}+R_{620})\frac{V_{gap}}{R_{12}}=0{,}6$ V
- $R_{207}+R_{208}+re\,(50\,\mu A)=8{,}5$ kΩ typ.
- $R_{621}=8$ kΩ typ.
- I_{wob} is a function of R_{wob} (see calculation of R_{wob})
- $A=0{,}6$ V
- I_{HPF} (see transfer function of $(I_{Re1}+I_{Re2})$ to V_{LPF} and I_{HPF}
- $V_{offset}=2{,}4$ V

* See Table 2.

Transfer function of inputs Re1 and Re2 to output AGC with V_{offset} and R_{osc} as parameters

The transfer is given by:

$$I_{agc} = \underbrace{-0{,}27 \frac{V_{osc1} + V_{osc2}}{R_{207} + R_{208} + re\ (50\ \mu A)}}_{-45^o} \cdot \tanh\left(\frac{I_{IN} \cdot R_{708}}{2V_T}\right) + Ix^*$$

Where:

$$I_{IN} = \underbrace{\sqrt{\frac{1}{2}} \cdot I_{wob} \cdot \frac{V_{osc1} - V_{ref}}{A}}_{0^o} - k\left(I_{Re1}\left(1 + \frac{\alpha}{2}\right) - I_{Re2}\left(1 - \frac{\alpha}{2}\right)\right)$$

$$\alpha = \frac{V_{offset} - V_{ref}}{R_B \cdot \frac{I_{int}}{2}};\ -1 \leqslant \alpha \leqslant 1$$

$$k = \frac{V_{agc} - 2V_j}{I_{int} \cdot R_{707}};\ 0 \leqslant k \leqslant 1$$

R_{708} = 4 kΩ typ.

$$I_{int} \cdot R_{707} = \frac{V_{gap}}{R_{12}} R_{707} = 2\ V$$

$$R_B \cdot \frac{I_{int}}{2} = (R_{619} + R_{620}) \frac{V_{gap}}{R_{12}} = 0{,}6\ V$$

$R_{206} + R_{207} + re\ (50\ \mu A)$ = 8,5 kΩ typ.

I_{wob} is a function of R_{wob} (see calculation of R_{wob})

A = 0,6 V typ. (see transfer function of C_{osc1}, C_{osc2} and R_{osc} to the generated wobble frequency)

DEVELOPMENT DATA

* See Table 4.

Table 4 Current output Ix

input conditions		output
radial switch	I_{IN} (μA)	Ix (μA)
OFF	$I_{IN} > 0{,}72 \frac{V_{gap}}{R_{osc}}$	50
OFF	$I_{IN} < 0{,}72 \frac{V_{gap}}{R_{osc}}$	0
ON	don't care	0

Transfer function of inputs Re1 and Re2 to output Lead

$I_{lead} = 10 \cdot I_{IN}$

Transfer function of inputs Re1 and Re2 to output Lag with the logical inputs B0, B1, B2 and B3 as parameters

Table 5 Transfer function of inputs Re1 and Re2 to output Lag with the logical inputs B0, B1, B2 and B3 as parameters.

condition of internal switches			Lag output
lag s/c	lag hold	radial	
ON			$V_{lag} = V_{ref}$
OFF	ON		$I_{lag} = 0$ (high ohmic)
OFF	OFF	ON	$I_{lag} = I_{IN}$*
OFF		OFF	$I_{lag} = 0$ (high ohmic)

Transfer function of input Lag to output RE_{lag}

The transfer function is: 1

$Z_{lag} \rightarrow \infty$
$Z_{RElag} \rightarrow 0$

* See transfer function of inputs Re1 and Re2 to output AGC with V_{offset} and R_{osc} as parameters.

DEVELOPMENT DATA

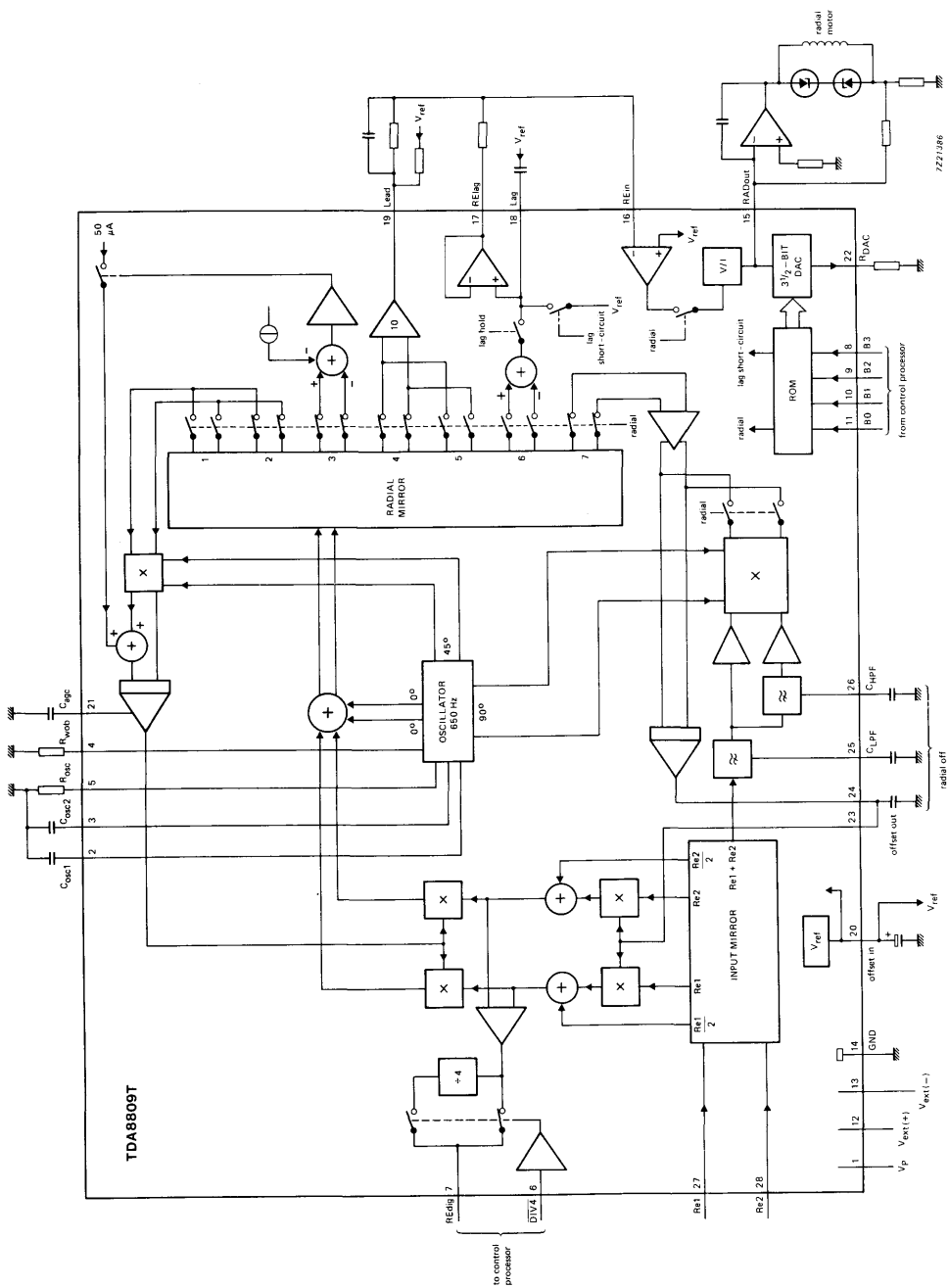


Fig. 4 Block diagram; TDA8809T.

I.F. LIMITING AMPLIFIER, FM DETECTOR AND AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDB1080 is a bipolar integrated circuit comprising a limiting amplifier, a balanced FM detector and a class-B audio amplifier. It is intended for frequencies up to 500 kHz with either narrow-band or wide-band FM. The circuit is especially suited for use in portophone sets, where a low supply voltage, a low supply current and a high sensitivity are of paramount importance.

QUICK REFERENCE DATA

Supply voltage range				
I.F. part	V_{CC1}		2,3 to 3,5	V
A.F. part	V_{CC2}		2,3 to 10	V
Supply current at $V_{CC1} = V_{CC2} = 2{,}5$ V, no signal	$I_{CC1} + I_{CC2}$	typ.	3	mA
Input voltage at onset of limiting	$V_{I1lim(rms)}$	typ.	30	μV
AM rejection at $V_i = 1$ mV	k_{AMR}	typ.	50	dB
Open-loop voltage amplification of audio amplifier	A_{vd}	typ.	200	
Output power of audio amplifier at $V_{CC2} = 9$ V	P_o	typ.	65	mW
Operating ambient temperature range	T_{amb}		−20 to + 70	°C

PACKAGE OUTLINES

TDB1080: 16-lead DIL; plastic (SOT38WBE).
TDB1080T: 16-lead mini-pack; plastic (SO16; SOT109A).

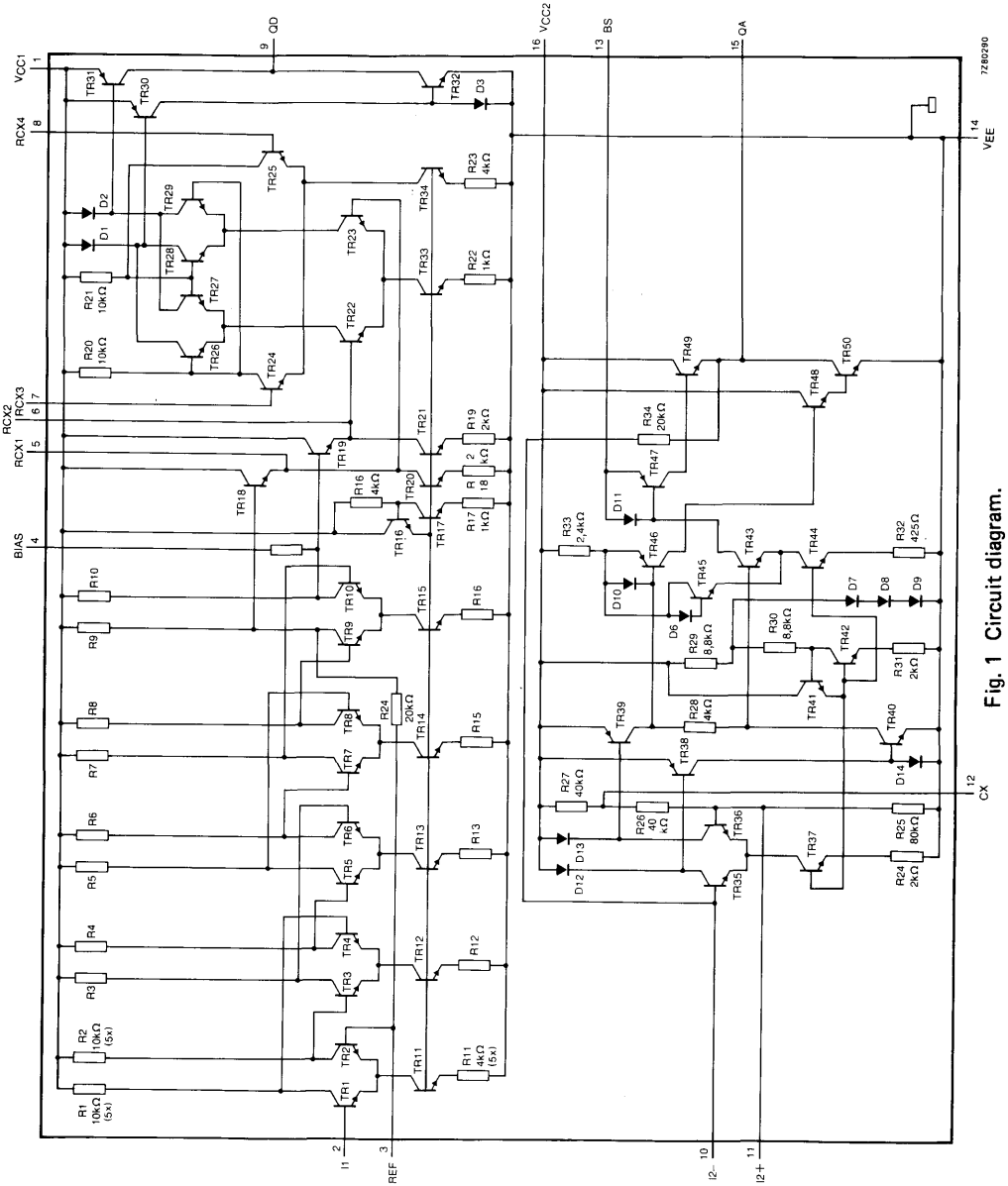


Fig. 1 Circuit diagram.

PINNING

1	V_{CC1}	positive supply, limiting amplifier
2	I1	limiting amplifier input
3	REF	reference input, limiting amplifier
4	BIAS	input biasing output
5	RCX1	external RC network
6	RCX2	external RC network
7	RCX3	external RC network
8	RCX4	external RC network
9	QD	FM detector output
10	I2–	out-of-phase input, audio amplifier
11	I2+	in-phase input, audio amplifier
12	CX	external capacitor
13	BS	bootstrap
14	V_{EE}	ground
15	QA	audio amplifier output
16	V_{CC2}	positive supply, audio amplifier

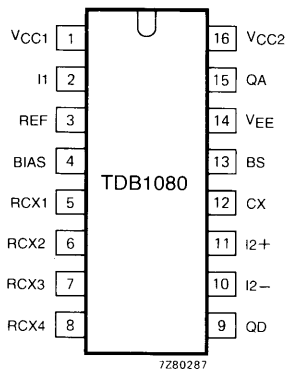


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The TDB1080 consists of two parts that may be used independently, viz. a limiting i.f. amplifier with balanced FM detector, and a class-B audio amplifier.

Supply

The two parts of the circuit have a common-ground pin V_{EE} but separate supply pins V_{CC1} and V_{CC2}. The limiting amplifier and detector may be used with a supply voltage up to 3,5 V, the audio amplifier up to 10 V. The circuit is built to a large extent on the basis of long-tailed pairs with current sources in their tails. Thanks to the stabilizer diodes (D7, D8 and D9) the supply current of the audio amplifier varies little with the supply voltage. This permits the circuit to be used over a wide supply voltage range without an excessive battery drain as a result.

Limiting amplifier inputs I1 and REF and biasing output BIAS (pins 2, 3 and 4)

The limiting amplifier has differential inputs I1 and REF. I1 is intended to be used as an input; it should be biased externally by connecting it to the input biasing output BIAS via a resistor or an inductor. The reference input REF is biased internally; it should be decoupled by connecting a capacitor from REF to ground.

The onset of limiting is specified as the input voltage giving 3 dB gain reduction.

External RC network pins RCX1 to RCX4 (pins 4 to 8)

The TDB1080 contains a quadrature detector which requires an RC phase shifting network. This has to be connected to RCX1, RCX2, RCX3 and RCX4 as shown in Fig. 4. The component values have to be chosen in accordance with the i.f. centre frequency.

Audio amplifier inputs I2+ and I2– (pins 11 and 10)

The audio amplifier has differential inputs I2+ and I2– which are biased internally.

FUNCTIONAL DESCRIPTION (continued)

External capacitor pin CX (pin 12)

The internal biasing network for input I2 + should be decoupled by connecting an external capacitor between CX and ground.

Audio amplifier output QA and bootstrap pin BS (pins 15 and 13)

The audio amplifier has a class-B output stage. The maximum output voltage swing is obtained by connecting a capacitor between the bootstrap pin BS and the output QA and the load from BS to V_{CC2} (see Fig. 4).

The maximum output power varies from typ. 15 mW at V_{CC2} = 2,5 V to typ. 65 mW at V_{CC2} = 9 V.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages, d.c.	V_{CC1}	max.	5 V
	V_{CC2}	max.	10 V
Supply current	$I_{CC1} + I_{CC2}$	max.	50 mA
Total power dissipation	P_{tot}	see Fig. 3	
Storage temperature range	T_{stg}	−55 to + 125	°C
Operating ambient temperature range	T_{amb}	−20 to + 70	°C

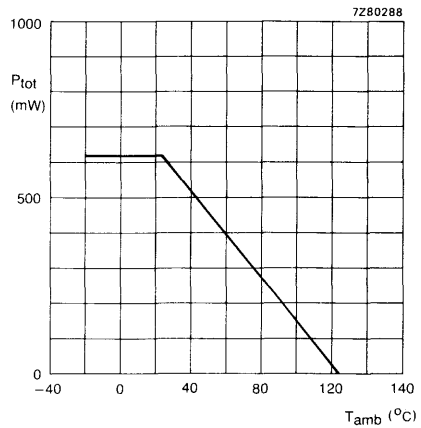


Fig. 3 Power derating curve.

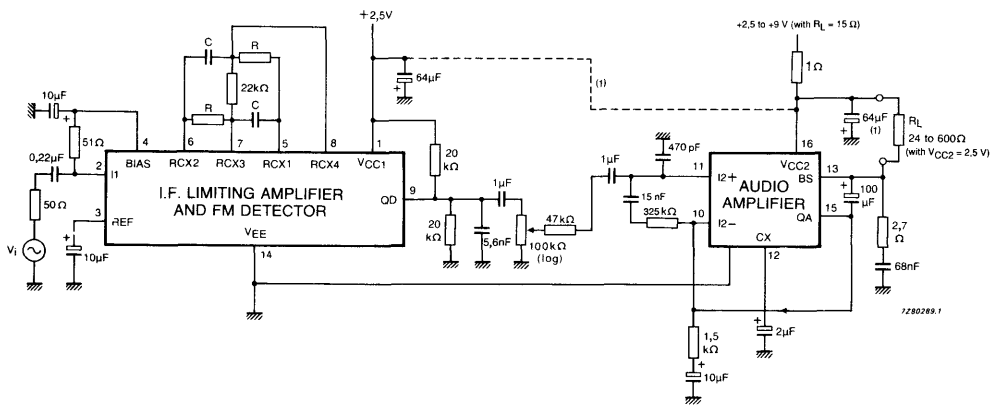
CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2{,}5$ V; $f_i = 95$ kHz; $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $T_{amb} = 25\ ^{o}C$ unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies V_{CC1} and V_{CC2} (pins 1 and 16)					
Supply voltages	V_{CC1}	2,3	2,5	3,5	V
	V_{CC2}	2,3	2,5	10	V
Supply currents					
at $V_{CC1} = 2{,}5$ V	I_{CC1}	–	1,5	2	mA
at $V_{CC2} = 2{,}5$ V, no signal	I_{CC2}	–	1,5	2	mA
at $V_{CC2} = 9$ V, no signal	I_{CC2}	–	3,5	–	mA
Limiting amplifier input I1 (pin 2)					
Input impedance	$\lvert z_{id} \rvert$	15	–	–	kΩ
Input voltage for onset of limiting (3 dB gain reduction)	$V_{I1lim(rms)}$	–	30	–	μV
Source impedance (between I1 and REF)	$\lvert Z_S \rvert$	–	–	5	kΩ
A.M. suppression					
at $\Delta f_i = 70$ Hz; $f_m = 1$ kHz; m = 0,3; $R_S = 50\ \Omega$					
at $V_{I1(rms)} = 300\ \mu$V	k_{AMR}	–	40	–	dB
at $V_{I1(rms)} = 1$ mV	k_{AMR}	–	50	–	dB
at $V_{I1(rms)} = 10$ mV	k_{AMR}	–	50	–	dB
$R_S = 5$ kΩ					
at $V_{I1(rms)} = 300\ \mu$V	k_{AMR}	–	30	–	dB
at $V_{I1(rms)} = 1$ mV	k_{AMR}	–	40	–	dB
at $V_{I1(rms)} = 10$ mV	k_{AMR}	–	50	–	dB
FM Detector output QD (pin 9)					
Output voltage at $d_{tot} = 0{,}5\%$;					
at $f_i = 95$ kHz; $\Delta f = \pm 50$ kHz	$V_{QD(rms)}$	100	–	–	mV
at $f_i = 250$ kHz; $\Delta f = \pm 50$ kHz	$V_{QD(rms)}$	100	–	–	mV
Signal-to-noise ratio					
at $f_i = 95$ kHz; $\Delta f = \pm 50$ kHz	S/N	70	–	–	dB
at $f_i = 250$ kHz; $\Delta f = \pm 50$ kHz	S/N	70	–	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Audio amplifier					
Open-loop voltage amplification	A_{vd}	–	200	–	
variation with frequency, f = 50 Hz to 15 kHz	ΔA_{vd}	−1,5	–	+ 1,5	dB
Load resistance	R_L	24	–	600	Ω
Output voltage at R_L = 24 Ω; d_{tot} = 1%	$V_{QA(rms)}$	–	600	–	mV
Total distortion at R_L = 24 Ω; $V_{QA(rms)}$ = 500 mV	d_{tot}	–	0,5	1	%
Output power at V_{CC2} = 9 V; R_L = 115 Ω; d_{tot} = 5%	P_{QA}	–	65	–	mW
Signal-to-noise ratio at R_L = 115 Ω; V_o = 600 mV; f = 0,5 to 11 kHz; 80 dB/octave cut-off filter	S/N	70	–	–	dB



(1) If V_{CC2} is equal to V_{CC1} pin 16 can be connected to pin 1 and the capacitor to pin 16 can be omitted.

Fig. 4 Test circuit and typical application of the TDB1080. For f_i = 95 kHz R = 100 kΩ and C = 82 pF, for f_i = 250 kHz R = 33 kΩ and C = 47 pF.

EQUALISER FOR AN AUDIO CASSETTE RECORDER

GENERAL DESCRIPTION

The TDD1601 is a CMOS switched capacitor circuit designed for high fidelity cassette recorders. This device compensates for the different types of tape, Ferro (FeO_2), Chrome (CrO_2) and Metal, that may be used and losses at the recording head. The TDD1601 has been optimized for use with the oscillator switch, TDA1600. The TDA1600 contains the oscillator for the erasing heads and playback amplifiers.

Features

- recording correction filters
- oscillator for the switched capacitor circuits
- drive outputs for the recording head and LED bar (recording level indicator)
- monitor paths
- programmable filter characteristics for different types of tape (FeO_2, CrO_2 and Metal)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range	V_{SS} = 0 V; pin 7	V_{DD}	10	15	15	V
Ground voltage range		GND	$\frac{0{,}9\ V_{DD}}{2}$	$\frac{V_{DD}}{2}$	$\frac{1{,}1\ V_{DD}}{2}$	
Supply current		I_{DD}	–	6	10	mA
Output voltage						
record mode		V_O	13	14	15	V
playback mode		V_O	0	1	2	V
Tape select output voltage	5 kΩ					
FeO_2		V_O	14,0	14,5	15,0	V
CrO_2		V_O	7,0	7,5	8,0	V
Metal		V_O	0	0,5	1,0	V

PACKAGE OUTLINE

24-lead DIL; plastic (SOT101B).

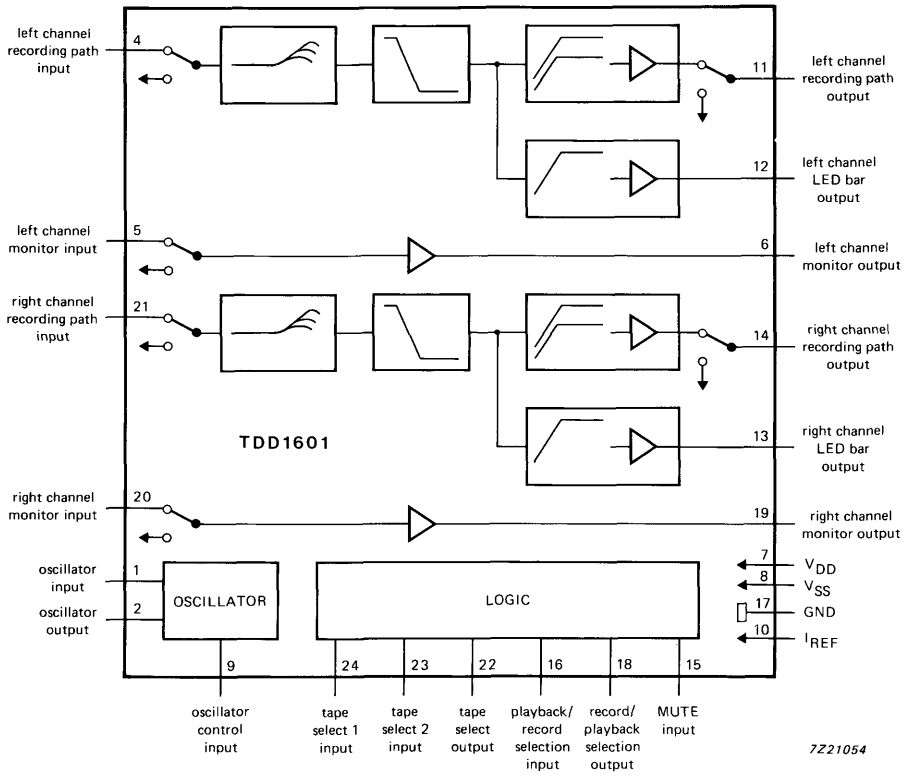


Fig. 1 Block diagram.

PINNING

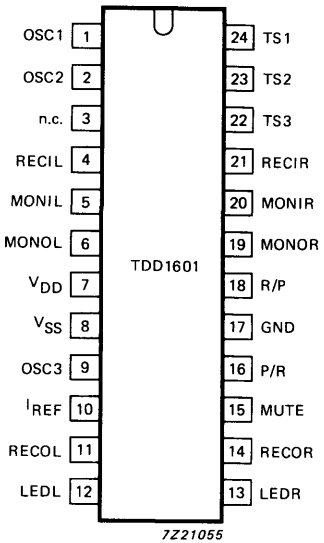


Fig. 2 Pinning diagram.

1	OSC1	oscillator input
2	OSC2	oscillator output
3	n.c.	not connected
4	RECIL	left channel recording path input
5	MONIL	left channel monitor path input
6	MONOL	left channel monitor path output
7	V_{DD}	positive supply voltage
8	V_{SS}	negative supply voltage
9	OSC3	oscillator control input
10	I_{REF}	current reference (grounded)
11	RECOL	left channel recording path output
12	LEDL	left channel LED bar output (recording level indicator)
13	LEDR	right channel LED bar output (recording level indicator)
14	RECOR	right channel recording path output
15	MUTE	mute input
16	P/R	playback/record selection input
17	GND	ground
18	R/P	record/playback selection output
19	MONOR	right channel monitor path output
20	MONIR	right channel monitor path input
21	RECIR	right channel recording path input
22	TS3	tape select output
23	TS2	tape select input 2
24	TS1	tape select input 1

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Oscillator

The TDD1601 requires an external oscillator with a clock frequency of 131 kHz (1,5 x erasing frequency) and a stability of better than 1%. This oscillator will be stabilized by an external ceramic resonator (such as the Murata CSB524P).

The oscillator control input enables the switched capacitor circuits to operate at 262 kHz, this is to allow the alteration of the frequency characteristics. A LOW on the input forces the circuit to operate at 131 kHz. A HIGH on the input forces the circuit to operate at 262 kHz. The gains of the correction filters, at both frequencies, are specified in the section 'CHARACTERISTICS'.

FUNCTIONAL DESCRIPTION (continued)

Recording correction filters

The recording correction path consists of 3 parts; a variable filter, a fixed filter and output buffers with gain correction.

Variable filter

The variable filter is used to compensate for the different types of tapes which may be used (FeO_2, CrO_2 and Metal) and losses at the recording head. Depending upon the type of tape used the FeO_2 filter or CrO_2 filter or Metal filter will be switched in. The output of the filter in use will be switched to the fixed filter. The transfer function of the variable filter contain 2 zeros and 3 poles. The gain of the variable filter is 0 dB at 315 Hz. This device has been developed for use with a single recording head.

Fixed filter

The fixed filter provides a pole at 20 Hz and a zero at 50 Hz (standardized value). The gain of the fixed filter is 0 dB.

Output buffers

The output buffers drives the recording head. The output buffer provides gain correction for the type of tape and the tape recording heads. The gain factors are as follows:

- FeO_2 tape: 5 dB
- CrO_2 tape: 9 dB
- Metal tape: 9 dB

A high-pass filter is also built-in with one pole at 20 Hz. During playback the output of the recording correction filter is switched to GND.

LED bar drive (recording level indicator)

The LED bar drive is a buffer with a gain of 0 dB. The input of the buffer is connected to the output of the fixed filter in the recording path.

Monitor path

The monitor path consists of a switch and an output buffer. The switch is used to connect the input of the buffer to GND. The output buffer has a low output impedance (max. 2 Ω). The input of the buffer requires a coupling capacitor to provide plop-free switching.

Command logic (see Fig. 4)

The command logic controls the switches used in the circuit. The inputs to the command logic are: TS1, TS2, MUTE, P/R and OSC3. The outputs are: TS3 and R/P. The filter characteristics are selected by TS1 and TS2 (see Table 1).

Table 1 Tape selection

Type of tape	TS1	TS2	TS3
FeO_2	GND	GND	V_{DD}
CrO_2	GND	open	GND
Metal	open	open	V_{SS}

TS3 indicates the position of the correction filters. This information is fed to TDA1600.

The P/R input selects the circuits required for record or playback mode. The output of R/P is connected to an external capacitor. When the P/R is LOW, a current of 120 μA flows out of the R/P output and charges the external capacitor. A high voltage on the input of R/P discharges the external capacitor. If the voltage from the capacitor is between V_{DD} and GND the circuit operates in record mode. If the voltage is between GND and V_{SS} the circuit operates in the playback mode.

The MUTE input is used to mute the circuits. A low voltage on the MUTE input connects the input to the variable filter and the output of the monitor path to GND. A high voltage on the MUTE input connects the input of the variable filter to RECIL (or RECIR) and the output of the monitor path to MONIL (or MONIR).

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range	V_{DD} to V_{SS}		−0,5	18	V
Input voltage range	pins 1, 2, 4, 5, 9, 20 and 21	V_{I1}	−0,5	V_{DD}+0,5	V
Input voltage range	pins 15, 16 and 24	V_{I2}	−0,5	V_{DD}+0,5	V
Supply current	pin 7	I_{DD1}	–	12	mA
Supply current	pin 8	I_{DD2}	–	10	mA
Total power dissipation		P_{tot}	–	300	mW
Operating ambient temperature range		T_{amb}	0	+ 70	°C
Storage temperature range		T_{stg}	−55	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} - V_{SS} = 15 V; GND = 7,5 V; T_{amb} = 25 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply	V_{SS} = 0 V					
Supply voltage range	pin 7	V_{DD}	10	15	15	V
Ground voltage range		GND	$\frac{0,9\ V_{DD}}{2}$	$\frac{V_{DD}}{2}$	$\frac{1,1\ V_{DD}}{2}$	V
Supply current		I_{DD}	–	6	10	mA
Power dissipation		P	–	84	–	mW
Recording correction filter						
Input impedance	f = 1 kHz	Z_I	120	180	240	kΩ
Gain for FeO_2 at 131 kHz						
	30 Hz	Gv	8,5	9,0	10	dB
	100 Hz	Gv	–	5,7	–	dB
	300 Hz	Gv	–	5,0	–	dB
	1 kHz	Gv	–	4,3	–	dB
	2 kHz	Gv	4,0	4,2	4,4	dB
	3 kHz	Gv	–	4,6	–	dB
	4 kHz	Gv	–	5,2	–	dB
	8 kHz	Gv	–	8,7	–	dB
	10 kHz	Gv	–	10,9	–	dB
	12 kHz	Gv	–	13,3	–	dB
	14 kHz	Gv	–	16,2	–	dB
	16 kHz	Gv	–	19,2	–	dB
	18 kHz	Gv	21,2	21,9	22,4	dB
Gain for CrO_2 at 131 kHz						
	30 Hz	Gv	12,5	13,0	14	dB
	100 Hz	Gv	–	9,7	–	dB
	300 Hz	Gv	–	9,1	–	dB
	1 kHz	Gv	–	9,2	–	dB
	2 kHz	Gv	9,3	9,5	9,7	dB
	3 kHz	Gv	–	9,9	–	dB
	4 kHz	Gv	–	10,4	–	dB
	8 kHz	Gv	–	13,6	–	dB
	10 kHz	Gv	–	15,5	–	dB
	12 kHz	Gv	–	17,7	–	dB
	14 kHz	Gv	–	20,1	–	dB
	16 kHz	Gv	–	22,8	–	dB
	18 kHz	Gv	25,0	25,5	26,0	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Gain for Metal at 131 kHz						
	30 Hz	Gv	12,5	13,0	15	dB
	100 Hz	Gv	–	9,7	–	dB
	300 Hz	Gv	–	9,0	–	dB
	1 kHz	Gv	–	8,7	–	dB
	2 kHz	Gv	8,3	8,5	8,7	dB
	3 kHz	Gv	–	8,7	–	dB
	4 kHz	Gv	–	8,9	–	dB
	8 kHz	Gv	–	10,9	–	dB
	10 kHz	Gv	–	12,3	–	dB
	12 kHz	Gv	–	13,9	–	dB
	14 kHz	Gv	–	15,8	–	dB
	16 kHz	Gv	–	18,0	–	dB
	18 kHz	Gv	20,1	20,6	21,2	dB
Gain for FeO_2 at 262 kHz						
	60 Hz	Gv	8,5	9,0	10	dB
	200 Hz	Gv	–	5,7	–	dB
	600 Hz	Gv	–	5,0	–	dB
	2 kHz	Gv	–	4,3	–	dB
	4 kHz	Gv	4,0	4,2	4,4	dB
	6 kHz	Gv	–	4,6	–	dB
	8 kHz	Gv	–	5,2	–	dB
	16 kHz	Gv	–	8,7	–	dB
	20 kHz	Gv	–	10,9	–	dB
Gain for CrO_2 at 262 kHz						
	60 Hz	Gv	12,5	13,0	14	dB
	200 Hz	Gv	–	9,7	–	dB
	600 Hz	Gv	–	9,1	–	dB
	2 kHz	Gv	–	9,2	–	dB
	4 kHz	Gv	9,3	9,5	9,7	dB
	6 kHz	Gv	–	9,9	–	dB
	8 kHz	Gv	–	10,4	–	dB
	16 kHz	Gv	–	13,6	–	dB
	20 kHz	Gv	–	15,5	–	dB
Gain for Metal at 262 kHz						
	60 Hz	Gv	12,5	13,0	15	dB
	200 Hz	Gv	–	9,7	–	dB
	600 Hz	Gv	–	9,0	–	dB
	2 kHz	Gv	–	8,7	–	dB
	4 kHz	Gv	8,3	8,5	8,7	dB
	6 kHz	Gv	–	8,7	–	dB
	8 kHz	Gv	–	8,9	–	dB
	16 kHz	Gv	–	10,9	–	dB
	20 kHz	Gv	–	12,3	–	dB

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Total harmonic distortion	1 kHz; V_{IN} = 580 mV; FeO_2, CrO_2 or Metal load on RECOL or RECOR = 10 kΩ	THD	–	–	0,2	%
	V_{IN} = 1,16 V; load on RECOL or RECOR = 6 kΩ	THD	–	–	1	%
Output voltage		V_O	3,25	–	–	V
Output current		I_O	530	–	–	μA
Signal to noise	measured from 20 Hz to 20 kHz	S/N	–55	–	–	dB
Channel separation	1 kHz	∝	50	–	–	dB
	10 kHz	∝	35	–	–	dB
LED bar (recording level indicator)						
Gain	FeO_2, CrO_2 and Metal at 315 kHz record mode; V_{IN} = 0 dB	Gv	–0,4	0	0,6	dB
	playback mode; V_{IN} = 0 dB	Gv	–0,4	0	0,6	dB
Output current		I_O	250	–	–	mA
Total harmonic distortion	1 kHz; V_{IN} = 1,16 V; CrO_2; load = 10 kΩ	THD	–	–	1	%
Monitor path						
Input impedance		Z_I	120	180	240	kΩ
Gain	20 Hz to 20 kHz; load on output = 10 kΩ	Gv	–0,2	–	0,2	dB
Total harmonic distortion	1 kHz; V_{IN} = 0 dB; load on output = 10 kΩ	THD	–	–	0,25	%
Signal to noise	20 Hz to 20 kHz; see Fig. 3, curve A	S/N	–80	–	–	dB
Output source current		I_O	2	–	–	mA
Output sink current		I_O	0,5	–	–	mA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Logic tape select output						
Output voltage	5 kΩ					
FeO_2		V_O	14,0	14,5	15,0	V
CrO_2		V_O	7,0	7,5	8,0	V
Metal		V_O	0	0,5	1,0	V
Record/playback						
Output voltage						
record		V_O	13	14	15	V
playback		V_O	0	1	2	V
Output current	R/P = GND					
record		I_O	−140	−220	−300	μA
playback		I_O	140	220	200	μA
Digital inputs	pins 9, 15 and 16					
Voltage input HIGH		V_{IH}	2,4	–	–	V
Voltage input LOW		V_{IL}	–	–	1,1	V
Input current		I_I	−1	–	1	μA
Digital inputs	pins 23 and 24					
Voltage input HIGH		V_{IH}	3,2	–	–	V
Voltage input LOW		V_{IL}	–	–	1,1	V
Input current	V_I = 5 V	I_I	20	30	120	μA
	V_I = 15 V	I_I	40	60	240	μA
Transition points						
Output voltage	pin 18; transition; record to mute and mute to record	V_O	0,7 V_{DD}	0,75 V_{DD}	0,8 V_{DD}	V
Output voltage	pin 16; transition; playback to mute and mute to playback	V_O	0,2 V_{DD}	0,25 V_{DD}	0,3 V_{DD}	V

D.C. CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Output current	between OSC2 and GND;					
	V_{OSC1} = 8,5 V	I_O	125	–	230	μA
	V_{OSC1} = 6,5 V	I_O	−160	–	−230	μA
Input current	OSC2 open;					
	V_{OSC1} = 8,5 V	I_O	4	–	20	μA
	V_{OSC1} = 6,5 V	I_O	−4	–	−20	μA

DEVELOPMENT DATA

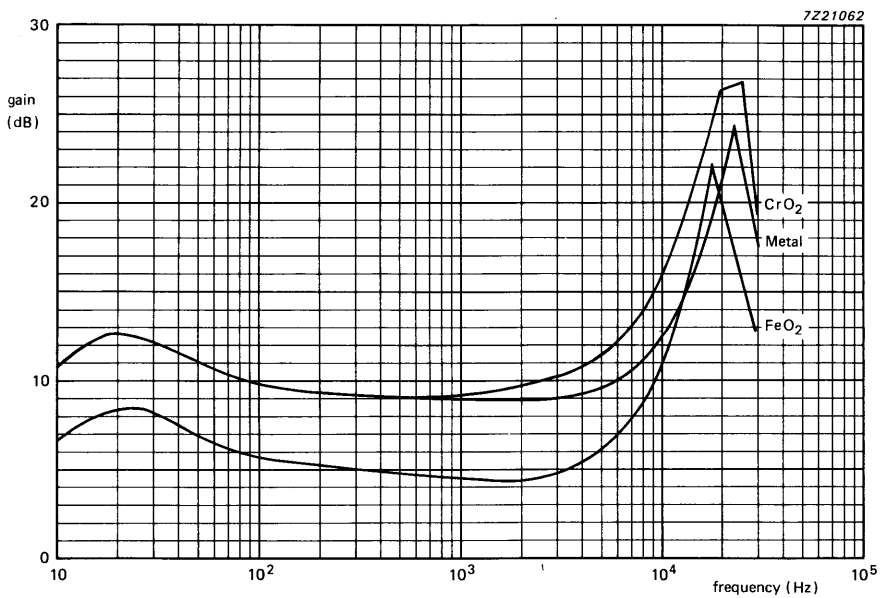


Fig. 3 Filter characteristics of the TDD1601.

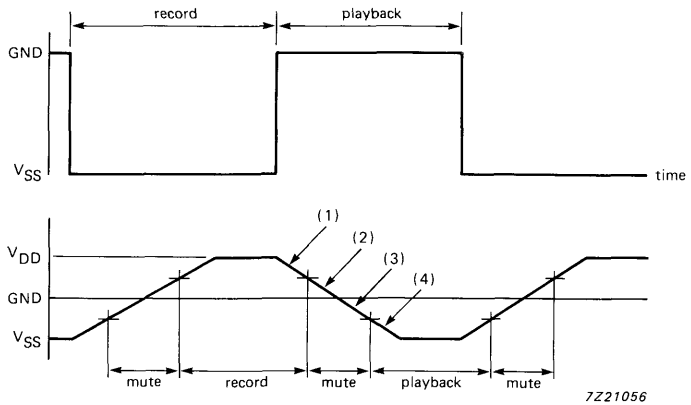
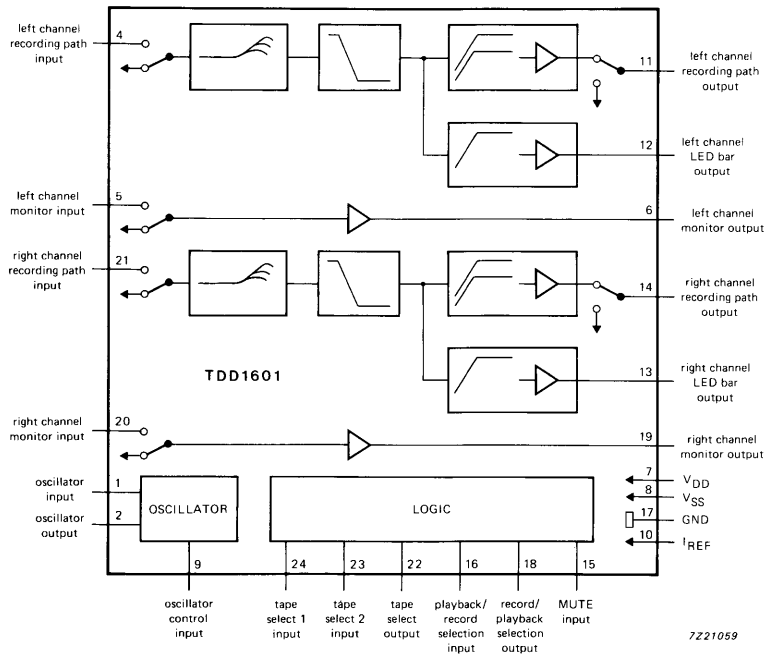
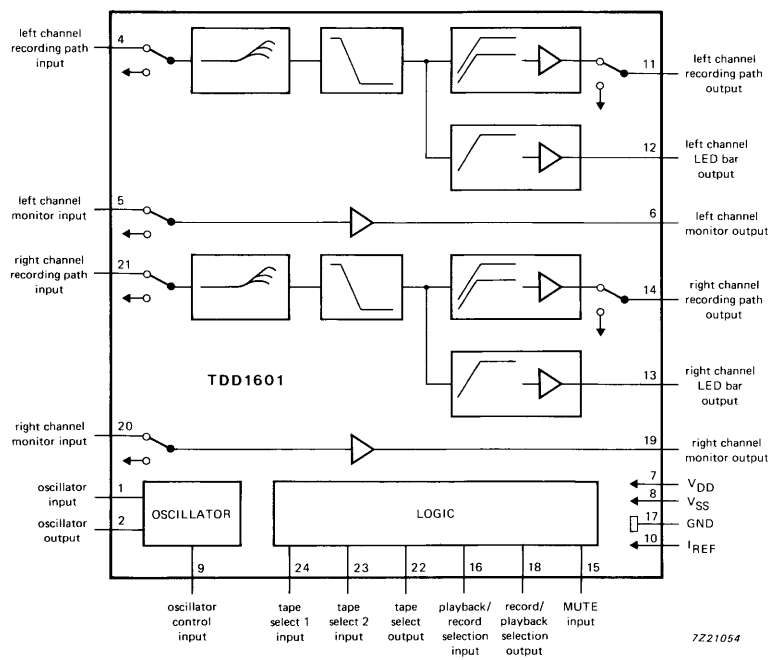


Fig. 4a Timing diagram for P/R.

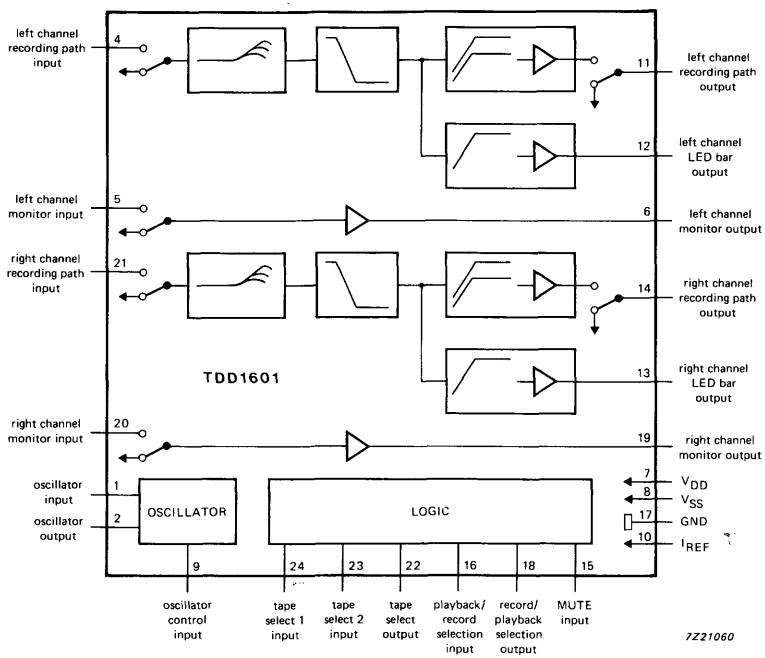


(a) position 1

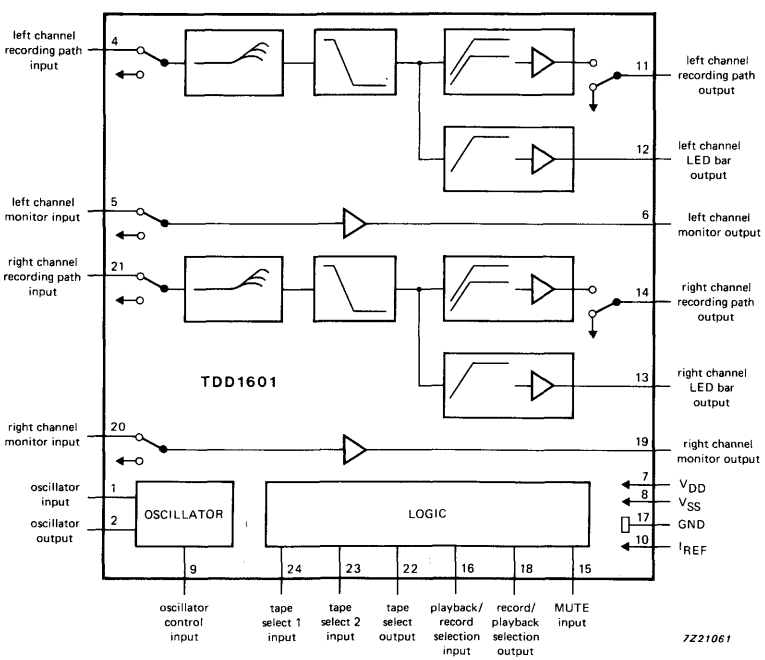


(b) position 2

Fig. 4b Position of the switches in the device (see Fig. 4a).



(c) position 3



(d) position 4

DEVELOPMENT DATA

APPLICATION INFORMATION

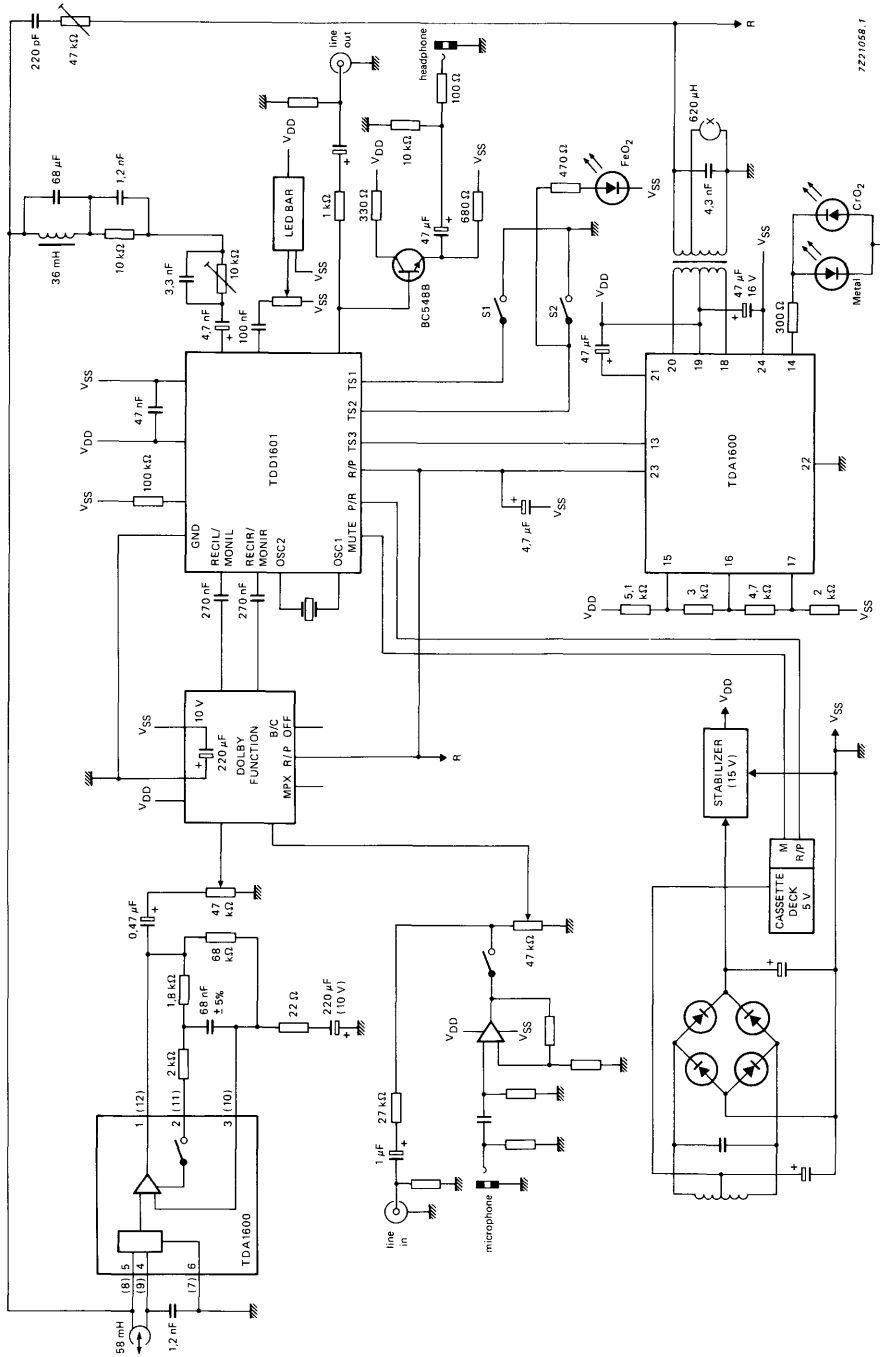


Fig. 5 Application circuit diagram for the TDD1601 and TDA1600 (131 kHz mode).

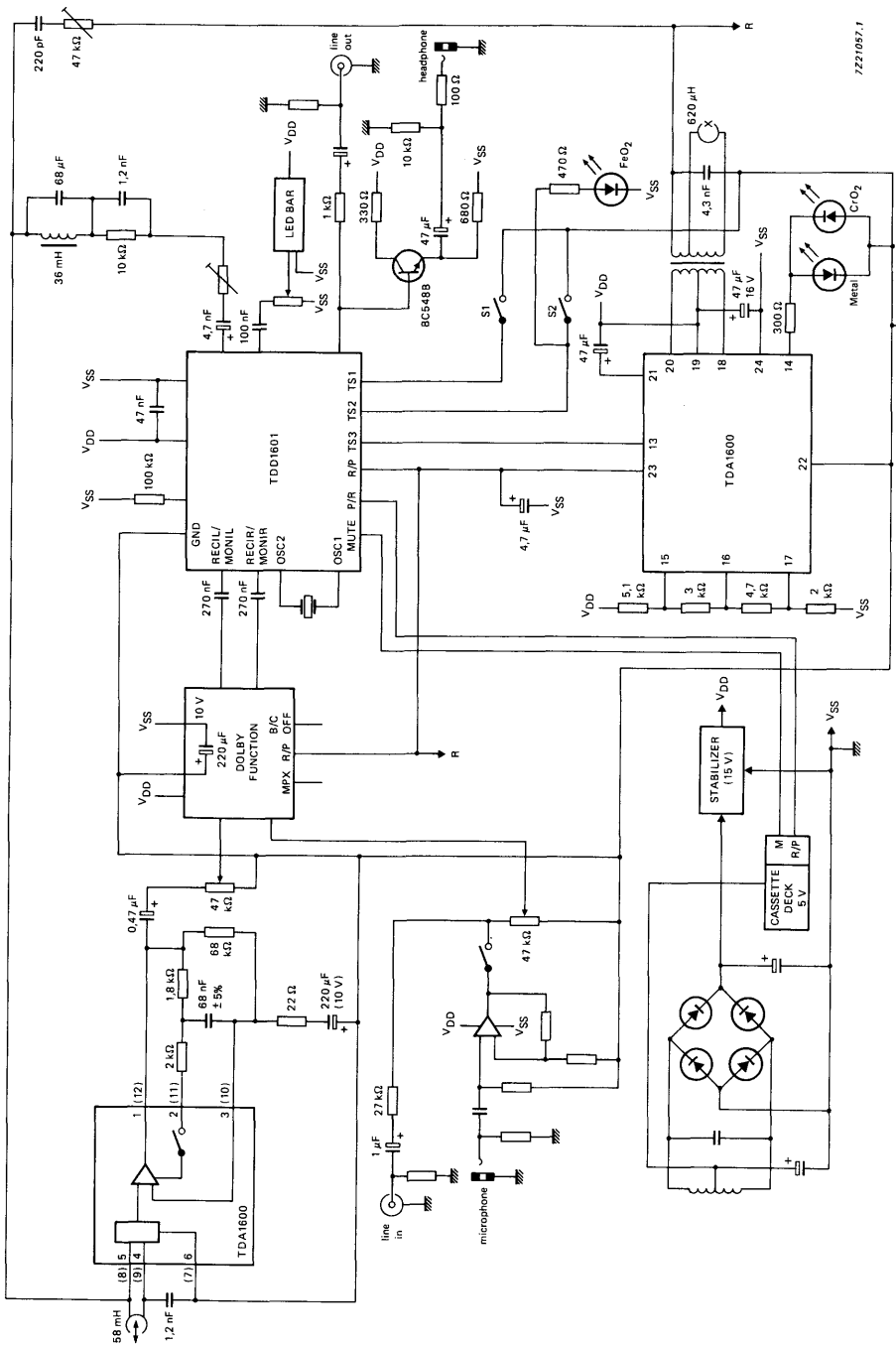


Fig. 6 Application circuit diagram for the TDD1601 and TDA1600 (262 kHz mode).

LOW POWER FREQUENCY SYNTHESIZER (LOPSY)

GENERAL DESCRIPTION

The TDD1742T is a low power, high-performance frequency synthesizer in local oxidation CMOS (LOCMOS) technology. The device is designed for use in channelized VHF/UHF applications especially portable and mobile radios.

The circuit incorporates many of the features of the HEF4750V (frequency synthesizer) and HEF4751 (universal divider), including a high-gain phase comparator together with an on-chip sample-and-hold capacitor and phase modulator.

A multiplexed or bus-structured programming sequence allows interface to a microcontroller or external memory (ROM/PROM); power is applied to the memory only when it is required for programming via additional on-chip circuitry.

Operation is possible with a minimum supply voltage of 7 V and a maximum input frequency of 8,5 MHz.

Encapsulation in a 28-lead mini-pack enables the construction of small, low power consumption synthesizers with low noise performance and high side-band attenuation.

Features

- On-chip sample-and-hold capacitor
- Low power consumption
- High-gain phase comparator with low levels of noise and spurious outputs
- Auxiliary digital phase comparator for fast locking
- On-chip phase modulator
- Simple interfacing to external memory
- Microcontroller compatible
- Power-on reset circuitry

QUICK REFERENCE DATA

Supply voltage ranges		
pin 14	$V_{DD1} = V_{14-6}$	7 to 10 V
pin 8	$V_{DD2} = V_{8-6}$	4,5 to 5 V
pin 1	$V_{DD3} = V_{1-6}$	7 to 10 V
Supply current (at T_{amb} = 25 °C; $V_{DD1} = V_{DD3}$ = 7,4 V; V_{DD2} = 5 V)		
pin 14 (phase modulator OFF)	$I_{DD1} = I_{14}$	max. 1,5 mA
pin 8	$I_{DD2} = I_8$	max. 100 μA

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

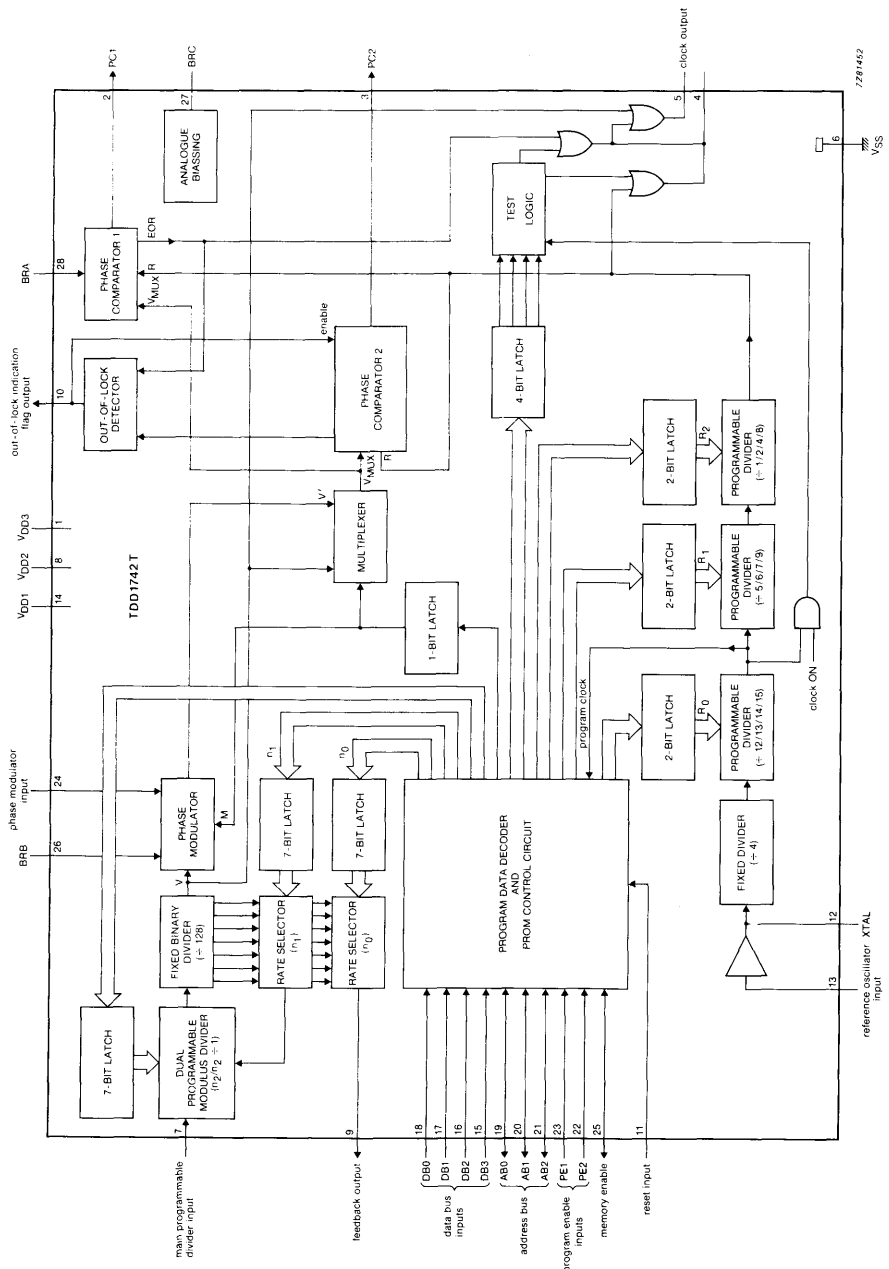


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

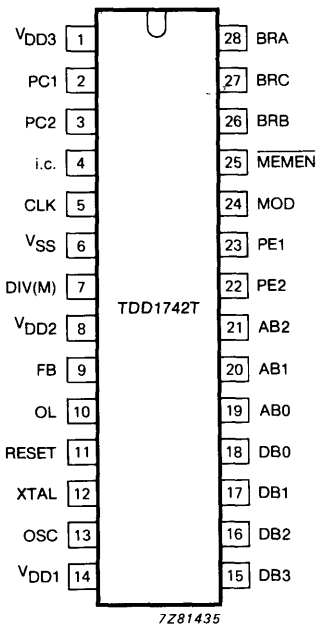


Fig. 2 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	V_{DD3}	**Power Supply 3:** analogue supply voltage (7 to 10 V).
2	PC1	**Phase Comparator 1:** high-gain analogue phase comparator output which is used when the system is in-lock to give low levels of noise and spurious outputs.
3	PC2	**Phase Comparator 2:** low-gain digital phase comparator 3-state output which enables the achievement of fast lock times when the system is initially out-of-lock. Phase comparator 2 is inhibited when the phase is within the locking range of phase comparator 1.
4	i.c.	**internally connected** (must be left floating).
5	CLK	**Clock:** clock output.
6	V_{SS}	**Ground:** circuit earth potential.
7	DIV(M)	**Divider:** input to the main programmable divider (8,5 MHz max.), usually from prescaler.
8	V_{DD2}	**Power Supply 2:** supply voltage for TTL-compatible stages (+ 5 V ± 10%).
9	FB	**Feedback:** feedback output to control the modulus of the external prescaler.
10	OL	**Out-of-lock:** out-of-lock indication flag output. This output is HIGH when phase comparator 2 is in operation (when the system is out-of-lock).
11	RESET	**Power-on-Reset:** Following power up an initial pulse is applied to this input pin to set the internal counters.

Pin functions (continued)

pin no.	mnemonic	description
12	XTAL	**Crystal:** output to external crystal to form the oscillator circuit in combination with the OSC input. Alternatively this pin may be used as a buffer output.
13	OSC	**Oscillator:** input to reference oscillator which together with the XTAL output and an external crystal is used to generate the reference frequency. Alternatively to OSC input may be used as a buffer amplifier for an external reference oscillator.
14	V_{DD1}	**Power Supply 1:** digital supply voltage (7 to 10 V).
15-18	DB3-DB0	**Data Bus:** Data Bus inputs (TTL compatible).
19-21	AB0-AB2	**Address Bus:** TTL compatible bidirectional address bus. Provides address output to an external memory or input from microcontroller. The outputs are 3-state with internal pull-downs.
22	PE2	**Program Enable 2:** TTL compatible inputs to initiate the programming cycle or strobe the internal data latches.
23	PE1	**Program Enable 1:**
24	MOD	**Modulator:** high impedance linear phase modulator input, which applies a voltage controlled delay to the programmable divider output to the phase comparator.
25	$\overline{\text{MEMEN}}$	**Memory Enable:** mode control and memory enable bidirectional pin. If pin 25 is LOW at general reset the TDD1742T is set to the micro-controller mode; if pin 25 is HIGH at general reset the TDD1742T is set to the memory mode and the ROM/PROM is enabled.
26	BRB	**Bias Resistor B:** current mirror which acts as gain control for the phase modulator.
27	BRC	**Bias Resistor C:** current mirror pin which provides analogue biassing.
28	BRA	**Bias Resistor A:** current mirror pin which acts as gain control for phase comparator 1.

FUNCTIONAL DESCRIPTION

Reference oscillator chain

The reference oscillator chain comprises a crystal oscillator and dividers to give the required frequency to drive the phase comparators.
The oscillator stage is a single inverter connected between pin 12 (XTAL) and pin 13 (OSC). Satisfactory operation is achieved with crystals up to 9 MHz. Alternatively, the OSC input may be used as a buffer amplifier for an external reference oscillator.
The reference divider chain comprises a fixed divide by 4-stage followed by three cascaded programmable dividers of ratios ÷ 12/13/14/15, ÷ 5/6/7/9 and ÷ 1/2/4/8. The output of the last stage is applied as one input (R) to the two phase comparators. Thus a number of division ratios between 240 and 4320 are possible which provides all the required VHF and UHF channel spacings with reference crystals in a 1 to 9 MHz range.

Main programmable divider

The main programmable divider is a rate feedback binary divider. As shown in figure 1 it comprises a fixed 7-bit binary divider (÷ 128) and two rate selectors (n_1 and n_0). One rate selector controls a 7-bit fully programmable dual modulus divider (÷ $n_2/n_2 + 1$) and the other controls the external dual modulus prescaler (÷ A/A + 1).

The overall division rate (N) is given by:

$N = (128\ n_2 + n_1)\ A + n_0$

Where:

$0 \leqslant n_0 \leqslant 127$
$0 \leqslant n_1 \leqslant 127$
$1 \leqslant n_2 \leqslant 127.$

The output from the programmable divider is fed to the phase comparators via the phase modulator and the multiplexer. The phase modulator is bypassed if not selected.

Phase comparison

The TDD1742T contains 2 phase comparators which act in close co-operation. Phase comparator 1 is the main comparator. It is designed to have a high-gain analogue output, 4500 volts/cycle at 10 kHz (typ.). This enables a low noise performance to be achieved. However, the output of phase comparator 1 will saturate at high or low levels for very small phase excursions.
Phase comparator 2 is an auxiliary comparator with a wide range, which enables faster lock times to be achieved than otherwise would be possible. This digital phase comparator has a linear $\pm 2\pi$ radians phase range, which corresponds to a gain of $\frac{V_{DD}}{2}$ volts/cycle.

To avoid degrading the noise performance of the system by the relatively low gain of phase comparator 2, once a small phase error has been achieved an internal switch disconnects phase comparator 2, leaving only phase comparator 1 connected. Thus the low noise properties of phase comparator 1 are obtained once phase-lock has been achieved.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 1 (see Fig. 3)

Phase comparator 1 is comprised of a linear ramp generator and a sample and hold circuit.

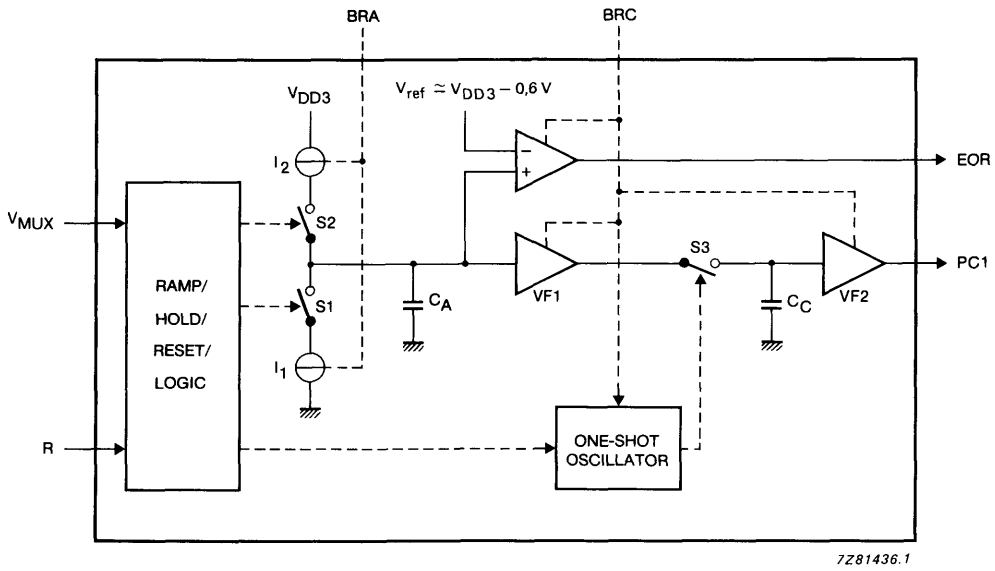


Fig. 3 Simplified block diagram of phase comparator 1.

A negative-going transition at the V_{MUX} input causes the hold capacitor C_A to be discharged via switch S1 and constant current source I_1.
A positive-going transition at the V_{MUX} input causes the hold capacitor C_A to be charged via switch S2 and constant current source I_2, which produces a linear ramp.
A negative-going transition at the R input terminates the linear ramp.
Capacitor C_A holds the voltage that the ramp has attained, and is buffered by the voltage follower VF1. After the output of VF1 is stable (2 μs), the sample switch S3 is closed for approximately 1 μs by the one-shot oscillator. This enables the capacitor C_C to charge to the voltage level of VF1 and in turn buffered by voltage follower VF2 made available at output PC1.
The construction and small duty cycle of the sample switch S3 provides a low hold step, resulting in a minimum side-band level.
If the linear ramp terminates before a negative-going transition at the R input is present, an end of ramp (EOR) signal is produced, generating in turn an out-of-lock (OL) signal. OL enables phase comparator 2 via the out-of-lock detector.

These actions are illustrated in the waveforms of Fig. 4 and Fig. 5.

The gain of phase comparator 1 as measured at PC1 is given by:

$$\text{PC gain} \simeq \frac{446\, I_{BRA}}{F_R}$$

Where:

I_{BRA} is in μA
F_R is the phase comparator reference frequency in kHz

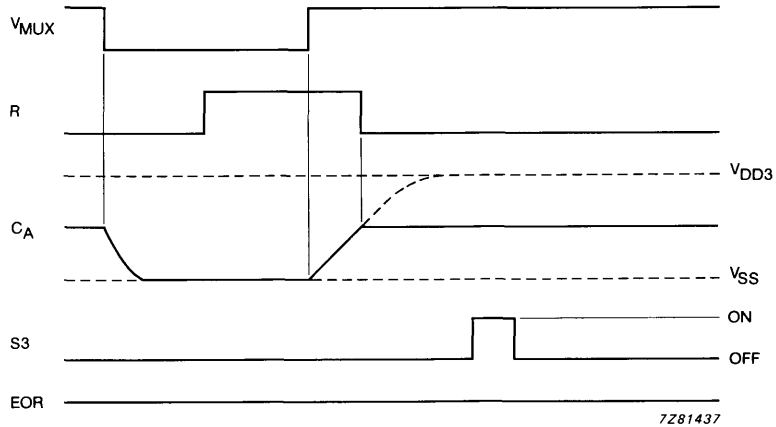


Fig. 4 Waveforms of phase comparator 1; in-lock condition.

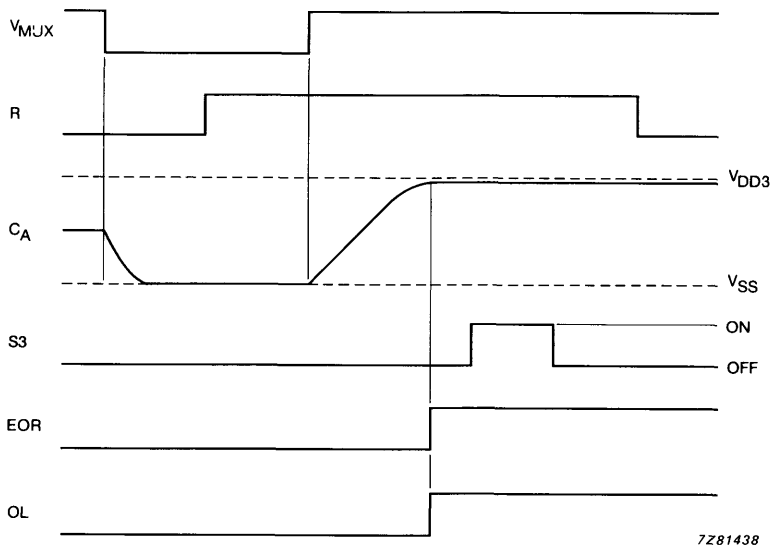


Fig. 5 Waveforms of phase comparator 1; out-of-lock condition.

When V_{MUX} leads R the output signal at pin 2 (PC1) is proportional to the phase difference (in-lock condition) or HIGH (out-of-lock condition).
When R leads V_{MUX} the output signal at pin 2 (PC1) remains LOW.

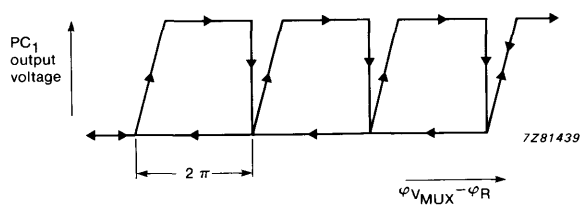


Fig. 6 Phase characteristic of output PC1.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 2 (see Fig. 7)

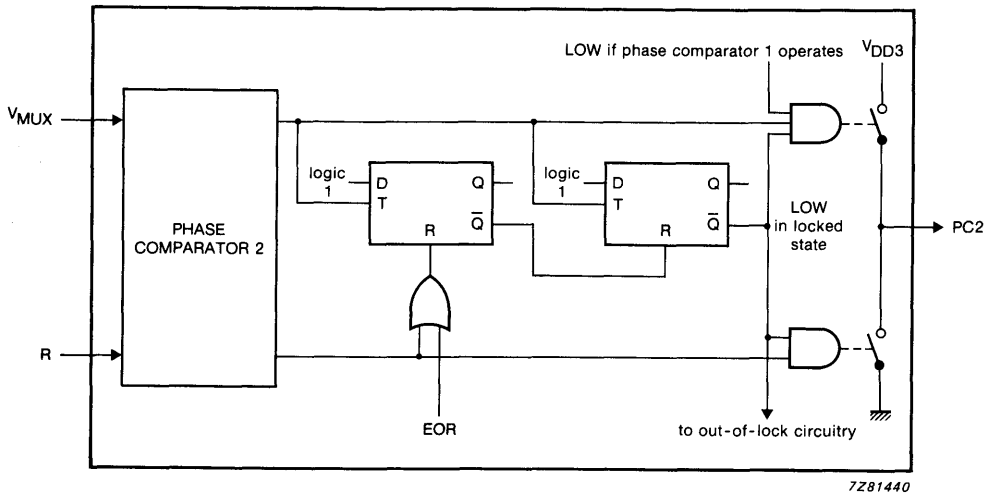


Fig. 7 Simplified block diagram of phase comparator 2.

The digital phase comparator (PC2) has three stable states:

- Reset
- V_{MUX} leads R
- R leads V_{MUX}

Table 1 Phase comparator 2: stable states and corresponding output levels

state	V_{MUX} leads R	R leads V_{MUX}
reset	0	0
V_{MUX} leads R	1	0
R leads V_{MUX}	0	1

Transition from one state to another takes place on command of either an active V_{MUX}-edge or an active R-edge as shown in Fig. 8.

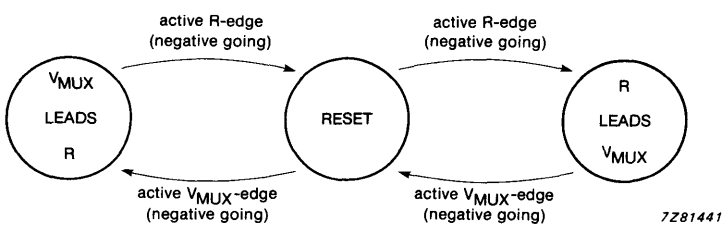


Fig. 8 Transition of state; phase comparator 2.

The output of phase comparator 2 produces positive or negative going pulses with variable width, dependent on the phase relationship of R and V_{MUX}.
The average output voltage is a linear function of the phase difference. Output at pin 3 (PC2) remains in the high impedance OFF-state in the region in which phase comparator 1 operates

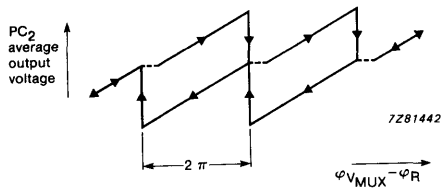


Fig. 9 Phase characteristic of output PC2.

To reach the reset state of phase comparator 2 it is necessary to apply:

- $2V_{MUX}$ + R*
  or
- 2R + V_{MUX}

Thus to achieve the R leads V_{MUX} state 2R must be applied; to achieve the V_{MUX1} leads R state $2V_{MUX}$ must be applied.

DEVELOPMENT DATA

Out-of-lock function

There are several situations when the system goes from the locked to the out-of-lock state (OL output goes HIGH):

- V_{MUX} leads R, however out of the range of phase comparator 1
- R leads V_{MUX}
- R-pulse is missing
- V_{MUX}-pulse is missing

In the first three situations the locked state can be reset by applying two successive cycles within the range of phase comparator 1.
In the fourth situation the locked state can be reset by applying a V_{MUX} pulse followed by two successive cycles within the range of phase comparator 1.

Phase modulator (see Fig. 10)

The linear phase modulator applies a voltage controlled delay to the signal from the programmable divider to the phase comparator input. The gain of the phase modulator is adjustable via an external bias resistor (BRB) which is connected between pin 26 and ground.
The time delay introduced into the V path to the phase modulator is:

$$\frac{909}{I_{BRB}} \text{ ns/volt of input applied to pin 24 (MOD)}$$

When a positive-going transition appears at the V-input, the D type flip-flop produces a HIGH V′ level and causes capacitor C_B to produce a positive-going ramp via switch S1 and constant current source I_1 starting at the V_{SS} potential. When the ramp has reached a value equal to the modulation input voltage (at MOD), the comparator resets the D type flip-flop, which terminates the V pulse. C_B now discharges to V_{SS} via switch S1 and constant current source I_2 and the circuit returns to the start position. Because the trailing edge of the V′ pulse is the active edge for the phase comparators, a linear phase modulation is achieved. The associated waveforms are shown in Fig. 11. The phase modulator can be switched OFF, via the programming logic, to avoid superfluous dissipation. To achieve, this the M signal must be programmed to logic 0. The V pulse will then be connected via switch S2 to V_{MUX}.

* This means apply two successive active V_{MUX} edges followed by one active R edge.

FUNCTIONAL DESCRIPTION (continued)

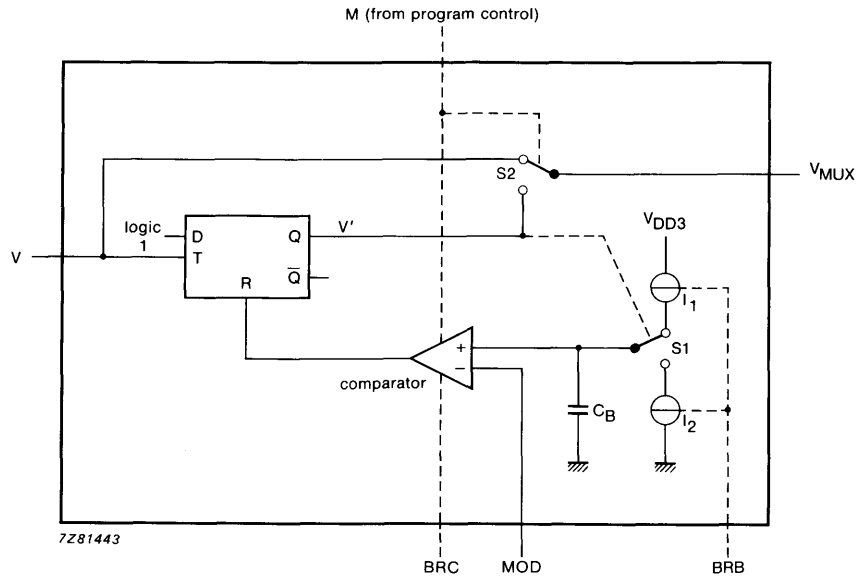


Fig. 10 Simplified block diagram of the phase modulator.

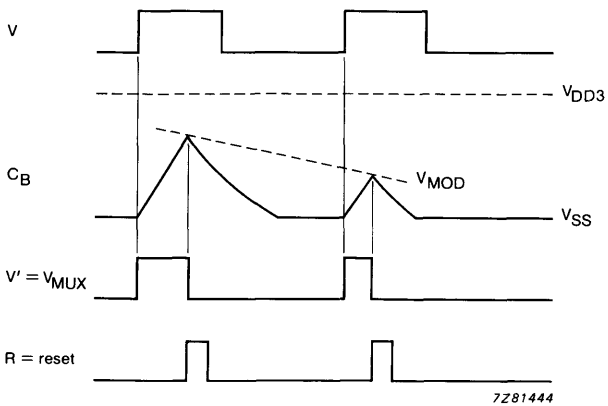


Fig. 11 Phase modulator waveforms; M = 1.

Program control

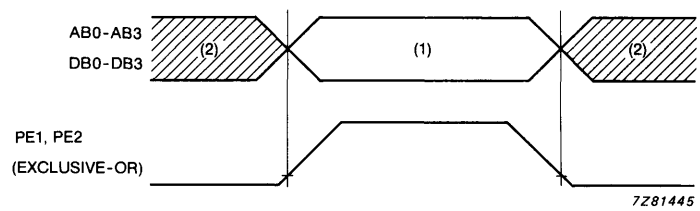
A multiplexed or bus structured sequence allows the TDD1742T to be interfaced to a microcontroller or a PROM.
The device is fully programmable in terms of:

- 6 bits to define the reference divider ratio
- 21 bits to define the main divider ratio
- 1 bit to switch the modulator
- 4 bits to determine the test status

Thus the TDD1742T is programmed with a total of 32 bits which are organized as eight 4-bit words. The address bus is 3 bits wide and the data bus is 4 bits wide. Both buses are TTL compatible. The data words are described in detail in Tables 3 to 7.

Microcontroller mode

If pin 25 ($\overline{\text{MEMEN}}$) is LOW at general reset, the device is set to the micro-controller mode. In this mode a 7-bit word, comprised of 3 address bits (AB0 to AB2) and 4 data bits (DB0 to DB3), may be strobed into the TDD1742T when the program enable pins PE1 and PE2 are set to opposite state (EXCLUSIVE -OR condition; see Fig. 12 and Table 2). One frame of 8 words is necessary to completely program the TDD1742T. Incoming data is not clocked into the internal counter latches until after the receipt of data corresponding to address 111. Upon subsequent reprogramming it is not necessary to change all eight words but a reprogramming sequence must always finish with the data corresponding to address 111.



(1) Address and data valid.
(2) Address and data not valid.

Fig. 12 Waveforms for program enable function; microcontroller mode.

Table 2 Truth table for program enable function; microcontroller mode

PE1	PE2	load
0	0	NO
1	0	YES
0	1	YES
1	1	NO

Program control (continued)

Memory mode (PROM)

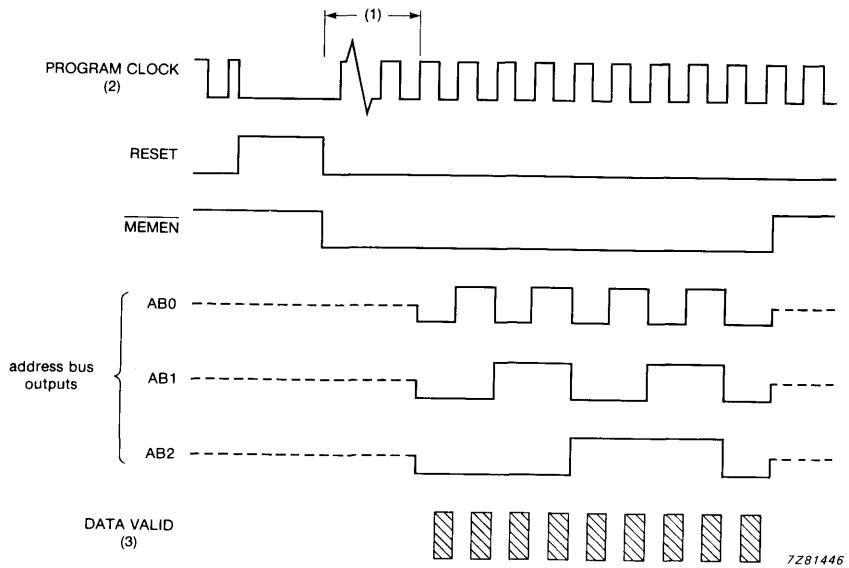
If pin 25 ($\overline{\text{MEMEN}}$) is HIGH at general reset, TDD1742T is set to the memory mode and a programming cycle is initiated. Subsequent reprogramming is performed by applying a pulse to program enable PE1 (pin 23) or PE2 (pin 22). If PE1 is LOW, programming will occur on the LOW-to-HIGH transition of PE2. If PE1 is HIGH, programming will occur on the HIGH-to-LOW transition of PE2. PE1 and PE2 are interchangeable. Reprogramming will also occur by applying a pulse to RESET (pin 11).

At the start of a programming sequence pin 25 goes LOW and may be used to apply power to the memory via an external driver. After a settling time the address bus outputs 000 followed by the remaining seven addresses. During the second half of each address period data, from the memory is latched into the TDD1742T so that the access time of the PROM is not critical.

Note

The program clock is derived from the reference divider chain and its frequency equals $f_{OSC}/4R_0$.

After the full 32 bits have been read the address returns to address 000 before going 3-state. This step transfers data from the internal data latches to the appropriate divider latches. Pin 25 now returns to a high impedance state and power is removed from the memory. Fig. 13 shows the timing for a reset initiated programming sequence; the timing is similar for program enable initiated sequence.



(1) Delay time for PROM settling.
(2) The program clock is derived from the reference divider chain.
(3) Data is valid during the shaded period.

Fig. 13 Timing diagram for TDD1742T PROM control.

Data memory maps

Table 3 Bit programming of the eight 4-bit words

address			data			
AB2	AB1	AB0	DB3	DB2	DB1	DB0
0	0	0	see Table 4			
0	0	1	$n_0 3$	$n_0 2$	$n_0 1$	$n_0 0$
0	1	0	$R_0 0$	$n_0 6$	$n_0 5$	$n_0 4$
0	1	1	$n_1 3$	$n_1 2$	$n_1 1$	$n_1 0$
1	0	0	$R_0 1$	$n_1 6$	$n_1 5$	$n_1 4$
1	0	1	$n_2 3$	$n_2 2$	$n_2 1$	$n_2 0$
1	1	0	M	$n_2 6$	$n_2 5$	$n_2 4$
1	1	1	$R_2 1$	$R_2 0$	$R_1 1$	$R_1 0$

In Table 3

n_0, n_1 and n_2 comprises the main programmable divider.

$n_0 0$ is the LSB of n_0, $n_0 6$ the MSB and so forth.

If M is 1 the modular is ON.

Table 4 Memory map for address 000

DB3	DB2	DB1	DB0	program clock *to output CLK*	mode
0	0	X	X	yes	idle
0	1	0	0	no	idle
all other combinations				not defined	not defined

Where

X = don't care.

For optimum performance (minimum crosstalk) 0100 should be programmed into address 000.

DEVELOPMENT DATA

Memory maps (continued)

Table 5 Reference divider control; part 1

$R_0 1$	$R_0 0$	division ratio
0	0	12
0	1	13
1	0	14
1	1	15

In Table 5:

$R_0 0$ and $R_0 1$ control the ÷ 12/13/14/15 portion of the reference divider.

Table 6 Reference divider control; part 2

$R_1 1$	$R_1 0$	division ratio
0	0	9
0	1	5
1	0	6
1	1	7

In Table 6:

$R_1 0$ and $R_1 1$ control the ÷ 5/6/7/9 portion of the reference divider.

Table 7 Reference divider control; part 3

$R_2 1$	$R_2 0$	division ratio
0	0	1
0	1	2
1	0	4
1	1	8

In Table 7:

$R_2 0$ and $R_2 1$ control the ÷ 1/2/4/8 portion of the reference divider.

Current biassing

Current biassing is provided by 3 external bias resistors A, B and C.

Bias Resistor A: is connected between pin 28 (BRA) and ground. The value of the resistor must be such that $I_{BRA} = 20\ \mu A$, which acts as gain control for analogue phase comparator 1.
Bias Resistor B: is connected between pin 26 (BRB) and ground. The value of the resistor must be such that $I_{BRB} = 3$ to $25\ \mu A$, which acts as gain control for the phase modulator.
Bias Resistor C: is connected between pin 27 (BRC) and ground. The value of the resistor must be such that $I_{BRC} = 5$ to $30\ \mu A$, which provides biassing for the remainder of the analogue circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges			
pin 14	V_{DD1}		−0,5 to + 15 V
pin 8	V_{DD2}		−0,5 to + 15 V
pin 1	V_{DD3}		−0,5 to + 15 V
Voltage on any input	V_I		−0,5 to V_{DD1} + 0,5 V
Relative supply voltage	V_{DD2}-V_{DD1}	max.	0,5 V
Relative supply voltage	V_{DD3}-V_{DD1}	max.	0,5 V
D.C. current into any input or output	± I	max.	10 mA
Power dissipation per package for T_{amb} = 0 to + 85 °C	P_{tot}	max.	400 mW
Power dissipation per output for T_{amb} = 0 to + 85 °C	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to 150 °C
Operating ambient temperature range	T_{amb}		−40 to 85 °C

DEVELOPMENT DATA

D.C. CHARACTERISTICS

$V_{DD1} = V_{DD3} = 7{,}4$ V; $V_{DD2} = 5$ V; $V_{SS} = 0$ V; $T_{amb} = 25\ ^{o}C$ unless otherwise specified; for definitions see note 1.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage					
pin 14	V_{DD1}	7	–	10	V
pin 8	V_{DD2}	4,5	–	5	V
pin 1	V_{DD3}	7	–	10	V
Supply current					
pin 14 (phase modulator OFF)	I_{DD1}	–	–	1,5	mA
pin 8	I_{DD2}	–	–	100	μA
pin 1 (phase modulator OFF)	I_{DD3}	–	–	1,5	mA
Input leakage current (notes 2 and 3)					
logic inputs, MOD	$\pm I_{LI}$	–	–	300	nA
Output leakage current (notes 2 and 3)					
at ½ V_{DD}					
PC2 high impedance OFF state	$\pm I_{LO}$	–	–	50	nA
$\overline{MEMEN}$ high impedance state	$\pm I_{LO}$	–	–	1,6	μA
I/O current					
AB0 to AB2 high impedance state	$I_{I/O}$	5	–	30	μA
Logic input voltage LOW					
CMOS inputs; CMOS I/Os	V_{IL}	–	–	$0{,}3V_{DD1}$	V
TTL inputs; TTL I/Os	V_{IL}	–	–	0,8	V
Logic input voltage HIGH					
CMOS inputs; CMOS I/Os	V_{IH}	$0{,}7V_{DD1}$	–	–	V
TTL inputs; TTL I/Os	V_{IH}	2	–	–	V
Logic output voltage LOW (note 2)					
at $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	50	mV
Logic output voltage HIGH (note 2)					
at $\lvert I_O \rvert < 1$ μA	V_{OH}	V_{DD1}-50	–	–	mV

parameter	symbol	min.	typ.	max.	unit
Logic output voltage LOW (note 2)					
$\overline{\text{MEMEN}}$ at I_{OL} = 4 mA	V_{OL}	–	–	1	V
PC2 at I_{OL} = 1,5 mA	V_{OL}	–	–	0,5	V
CLK; OL at I_{OL} = 1 mA	V_{OL}	–	–	0,5	V
XTAL at I_{OL} = 3 mA	V_{OL}	–	–	0,5	V
FB at I_{OL} = 1 mA	V_{OL}	–	–	0,5	V
AB0; AB1; AB2 at I_{OL} = 0,2 mA	V_{OL}	–	–	0,4	V
Logic output voltage HIGH (notes 2 and 3)					
PC2 at $-I_{OH}$ = 1,5 mA	V_{OH}	$V_{DD1}-0,5$	–	–	V
CLK; OL at $-I_{OH}$ = 1 mA	V_{OH}	$V_{DD1}-0,5$	–	–	V
XTAL at $-I_{OH}$ = 3 mA	V_{OH}	$V_{DD1}-1$	–	–	V
FB at $-I_{OH}$ = 1 mA	V_{OH}	$V_{DD2}-1$	–	–	V
AB0; AB1 at I_{OH} = 0,2 mA	V_{OH}	2,4	–	–	V
AB2 at I_{OH} = 0,8 mA	V_{OH}	2,4	–	–	V
Output PC1					
sink current (notes 2, 3 and Fig. 15)	I_O	1	–	–	mA
source current (notes 2, 3 and Fig. 16)	$-I_O$	1	–	–	mA
Internal resistance of phase comparator 1 (notes 2 and 3) locked state |output swing| $<$ 200 mV specified output range: $0,5\ V_{DD}-0,5$ V to $0,5\ V_{DD}+0,5$ V	R_i	–	2,0	–	Ω

DEVELOPMENT DATA

A.C. CHARACTERISTICS

A dynamic specification is given for the circuit, built-up with external components as shown in Fig. 14, under the following conditions; for definitions see note 1; V_{DD} = 7,4 ± 0,4 V; T_{amb} = 25 °C; input transition times ⩽ 40 ns; $C_A = C_B = C_C$ = 10 nF; R_A chosen so that I_{RA} = 20 μA ± 1 μA; R_B chosen so that I_{RB} = 3 to 25 μA; R_C chosen so that I_{RC} = 5 to 30 μA; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Main programmable divider (DIV(M); pin 7)					
input frequency all divider ratios (square wave input)	$f_{DIV(M)}$	8,5	–	–	MHz
Reference divider					
input frequency all divider ratios (square wave input)	$f_{DIV(R)}$	9	–	–	MHz
Oscillator frequency (OSC; pin 13)	f_{OSC}	9	12	–	MHz
Input capacitance					
DIV(M); OSC	C_I	–	–	3	pF
DB0 to DB3; PE1; PE2; AB0 to AB2	C_I	–	–	5	pF
Propagation delay (see Fig. 17)					
Feedback output to external prescaler					
DIV(M) → FB at C_L = 10 pF					
HIGH to LOW*	t_{PHL}	–	35	70	ns
LOW to HIGH*	t_{PLH}	–	35	70	ns
Average power supply current (notes 3 and 4)					
in-lock state	I_{DD1}	–	2	–	mA
	I_{DD2}	–	0,15	–	mA
	I_{DD3}	–	0,45	–	mA

* Measured from 30% point of negative-going edge at DIV(M) to 50% point of either output edge of FB.

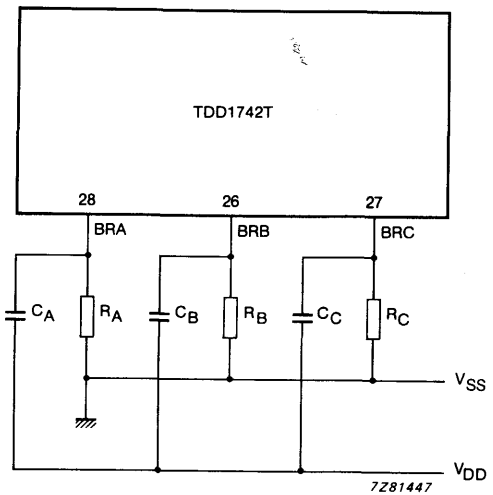


Fig. 14 Test circuit for measuring a.c. characteristics.

Notes to the characteristics

1. Definitions:
   R_A = external biassing resistor between pins BRA and V_{SS}.
   R_B = external biassing resistor between pins BRB and V_{SS}.
   R_C = external biassing resistor between pins BRC and V_{SS}.
   C_A = decoupling capacitor between pins BRA and V_{DD}.
   C_B = decoupling capacitor between pins BRB and V_{DD}.
   C_C = decoupling capacitor between pins BRC and V_{DD}.
   CMOS logic inputs: RESET, OSC.
   CMOS logic outputs: PC2, CLK, OL, XTAL.
   CMOS logic I/O: $\overline{\text{MEMEN}}$.
   TTL logic inputs: DB0 to DB3, PE2, PE1.
   TTL logic output: FB.
   TTL logic I/O: AB0 to AB2.
   Analogue inputs: DIV(M), MOD.
   Analogue output: PC1.
   Analogue biassing pins: BRA, BRB, BRC.
2. All logic inputs at V_{SS} or V_{DD}.
3. R_A connected; its value chosen such that $I_{BRA} = 20\ \mu A$.
   R_B connected; its value chosen such that $I_{BRB} = 20\ \mu A$.
   R_C connected; its value chosen such that $I_{BRC} = 20\ \mu A$.
4. Average power supply current measured at:
   f_{OSC} = 5 MHz, external clock, divider ratio 420;
   $f_{DIV(M)}$ = 2 MHz, divider ratio 168.

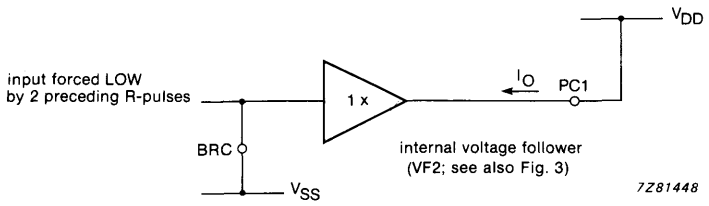


Fig. 15 Equivalent circuit for output PC1 sink current.

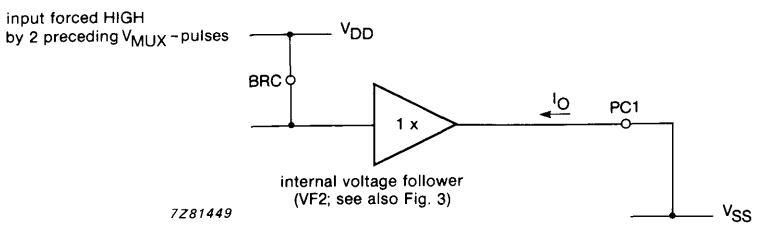


Fig. 16 Equivalent circuit for output PC1 source current.

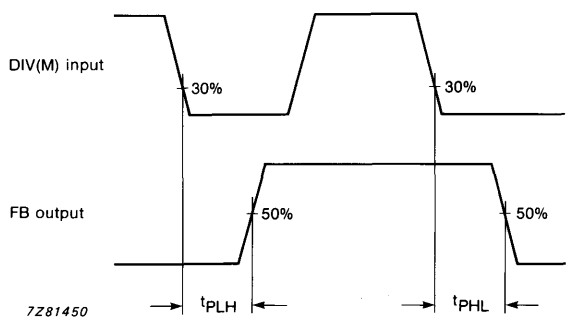


Fig. 17 Waveforms showing propagation delay; DIV (M) → FB.

APPLICATION INFORMATION

Fig. 18 shows a typical application circuit using the TDD1742T in the memory mode with the following design parameters:

Frequency range	150 to 155 MHz
VCO sensitivity	1 MHz/V
Reference frequency	12,5 kHz
Prescaler	÷ 80/81
Reference crystal frequency	5,25 MHz
Reference divider chain	÷ 15; ÷ 7; ÷ 1
Total division ratio	12000 to 12400
Loop bandwidth	300 Hz

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

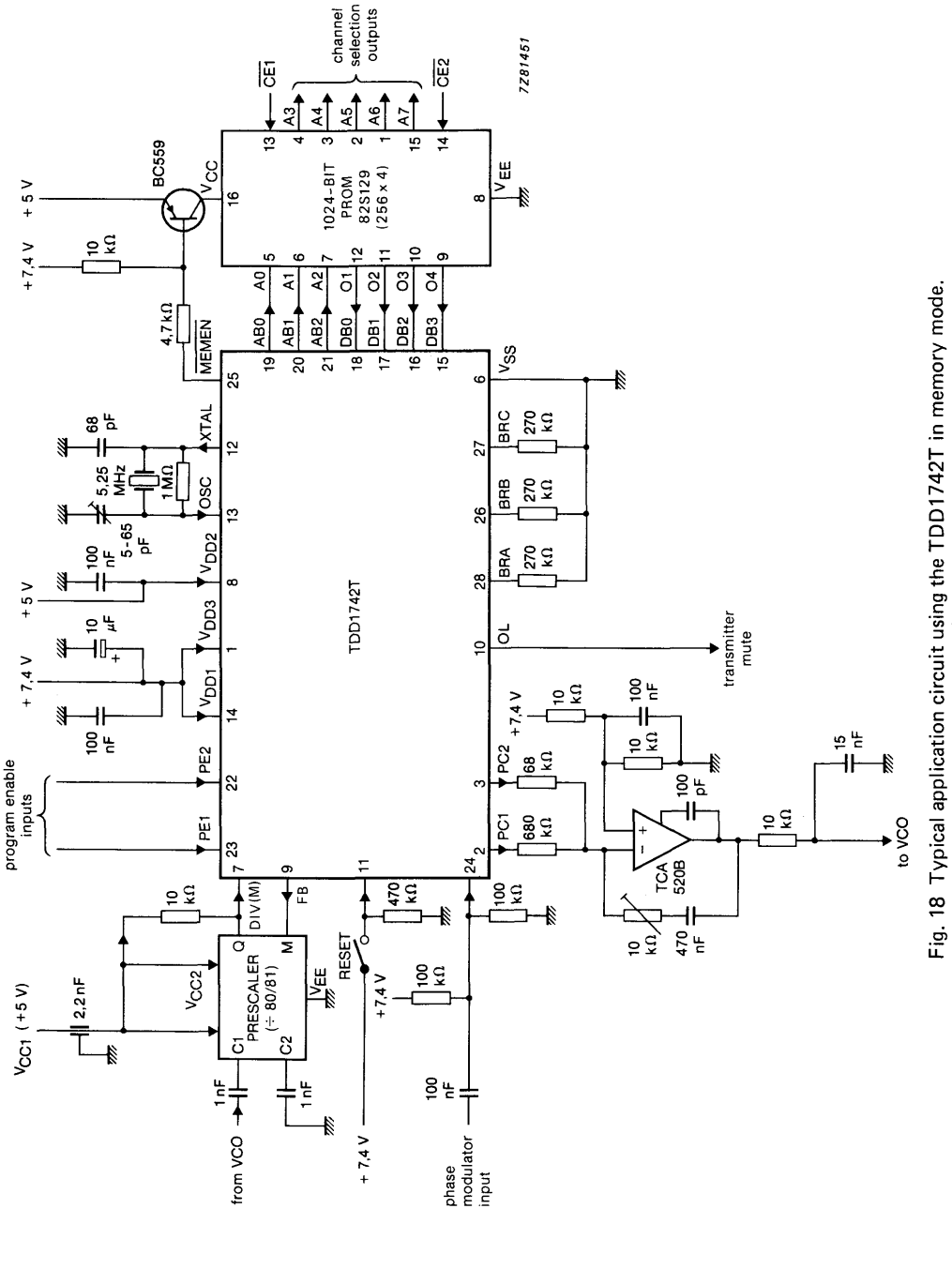


Fig. 18 Typical application circuit using the TDD1742T in memory mode.

DOLBY* B & C TYPE NOISE REDUCTION CIRCUITS

GENERAL DESCRIPTION

The TEA0651/TEA0652 and TEA0654 provide both, Dolby B and Dolby C type audio Noise Reduction (NR). The TEA0651/TEA0652 are NR signal processing ICs in 18-lead DIL packages. They can be used either as a stereo Dolby B NR circuit or as one channel of a switchable Dolby B & C NR circuit. In addition they provide NR ON/OFF switching.
The TEA0654 is a switching IC in a 24-lead DIL package. It contains the switching, the pre-amplifiers for playback and recording functions and a multiplex filter buffer amplifier.
The circuits are pin compatible to Signetics NE651, NE652 and NE654 respectively.

Features

TEA0651/TEA0652

- Dual purpose IC for Dolby B & C NR systems:
  switchable B/C type NR systems, B-type NR systems (stereo without preamplifiers), automotive entertainment systems (playback only) and portable applications
- Dual version for better matching between HIGH and LOW level stages in C-type NR or better channel matching for stereo B-type NR applications
- Full-wave rectifier
- No capacitive divider for side-chain filter needed
- Electronic switching for NR ON/OFF, B and C-type NR
- Dolby level 0 dB = −6 dBm (387,5 mV) offers line output level option of 0 dBm (775 mV)

TEA0654

- Electronic switching for playback/record
- Electronic switching for NR ON/OFF and B/C type NR
- No internal/external matching required for filter networks:
  only one network for spectral skewing and deskewing necessary; only one network for anti-saturation necessary
- Excellent matching between record and playback
- Line output (monitor) level externally set by resistor ratio independent of internal Dolby level
- Playback and record preamplifier and multiplex filter buffer amplifier included

PACKAGE OUTLINES

TEA0651/TEA0652: 18-lead DIL; plastic (SOT102H).
TEA0654: 24-lead DIL; plastic (SOT101A).

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, U.S.A., from whom licensing and application information must be obtained.
Dolby is a registered trademark of Dolby Laboratories Licensing Coporation.

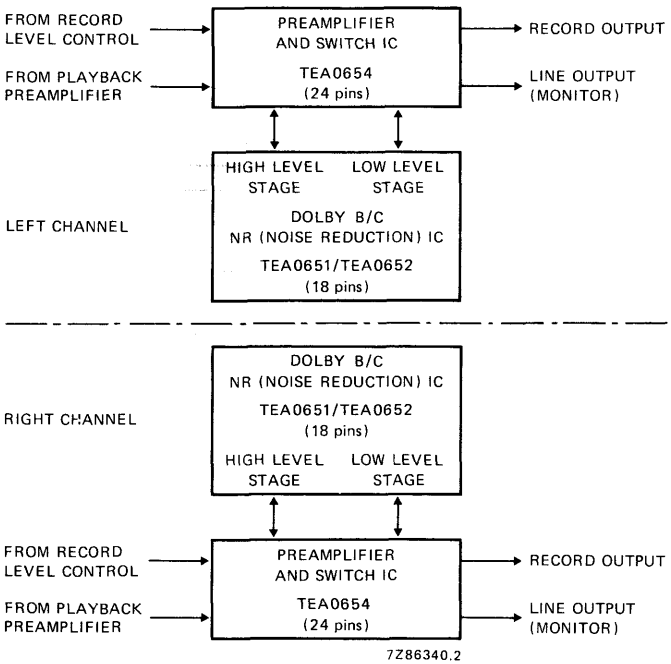
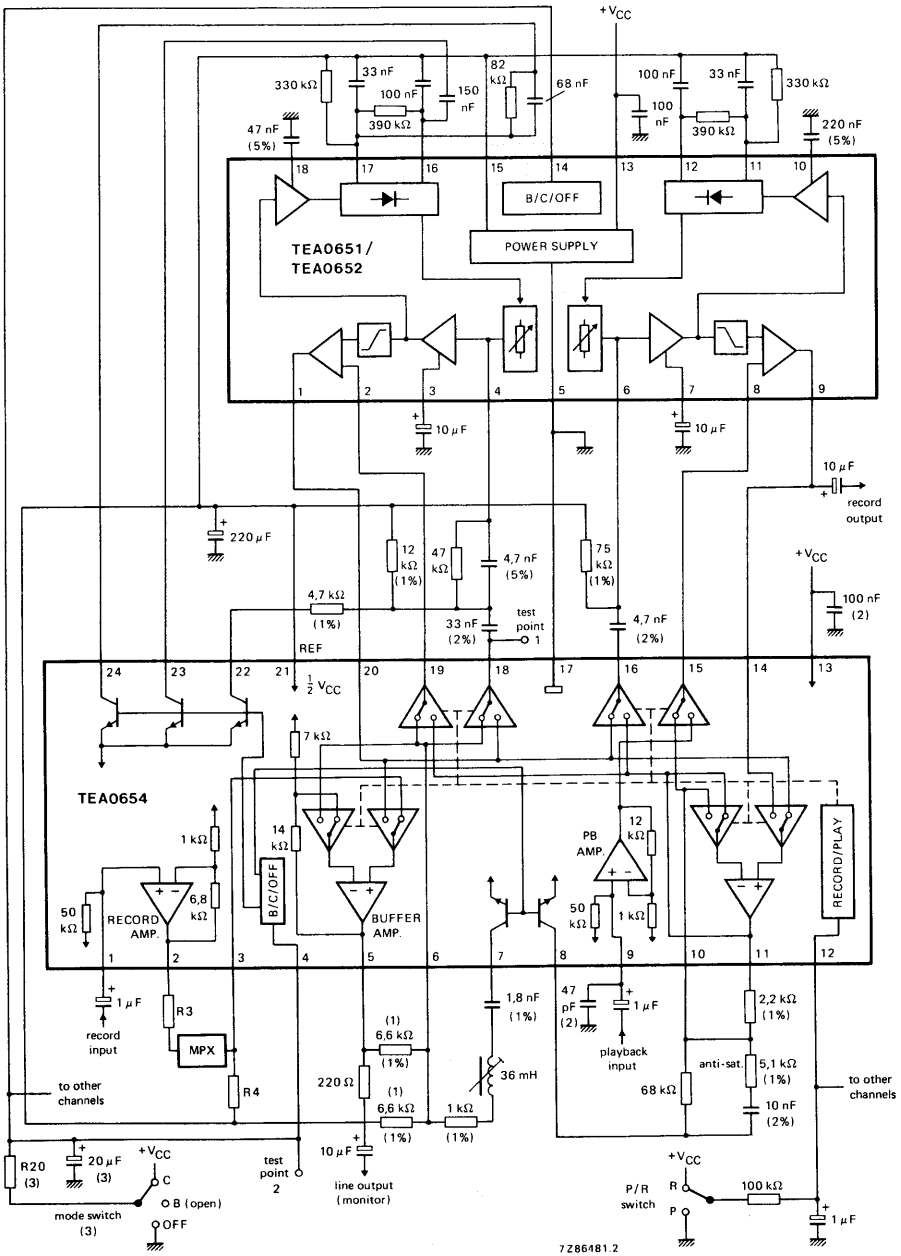


Fig. 1 System block diagram.

Switching levels; see Fig. 2.

pin condition (test point 2)	functions switched for TEA0654 (pin 4)	functions switched for TEA0651/TEA0652 (pin 14)
$+V_{CC}$	Dolby-C, open collector transistors at pins 7 and 8 switched on, at pins 22, 23, 24 switched off	Dolby-C
$\frac{1}{2}V_{CC}$	not applicable	stereo Dolby B, both channels active (Figs 15 and 16)
open (internally pulled to $\frac{1}{4}V_{CC}$)	Dolby-B, open collector transistors at pins 7 and 8 switched off, at pins 22, 23, 24 switched on	Dolby-B, low level stage side chain muted
ground	as pin condition 'open'	NR-OFF both side chains muted



(1) Line output and record input programming resistors.
(2) Optional capacitors.
(3) Time constant for mode switch is optional, R20 is equal to 6,8 kΩ divided by number of switched channels.

Fig. 2 Dolby B/C NR system; switches shown in record position.

SYSTEM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	23	V
Storage temperature range	T_{stg}	−55 to + 150		°C
Operating ambient temperature range	T_{amb}	−30 to	+ 85	°C
Total power dissipation				
TEA0651/TEA0652	P_{tot}	max.	600	mW
TEA0654	P_{tot}	max.	800	mW

SYSTEM CHARACTERISTICS

V_{CC} = 14 V; f = 20 Hz to 20 kHz; T_{amb} = 25 °C; all levels with reference to 387,5 mV = 0 dB = −6 dBm at test point 1 in Fig. 2; record mode; unless otherwise specified; for graphs see Figs 10 to 16.

parameter	conditions			min.	typ.	max.	unit
	mode	f(kHz)					
Supply voltage range	C	–	V_{CC}; note 1	8	14	20	V
Input sensitivity	C	–	record mode	–	50	–	mV
			playback mode note 2	–	30	–	mV
Signal handling at record output note 3	C	–	V_{CC} = 8 V line output is −6 dBm	12	–	–	dB
	C	1	V_{CC} = 14 V THD - 1% line output is −6 dBm	–	18	–	dB
	–	1	V_{CC} = 14 V line output is 0 dB,	12	–	–	dB
Signal-to-noise ratio (S/N)	C	–	R_S = 10 kΩ CCIR/ARM weighted	60	66	–	dB
Switching thresholds note 4	OFF	–	voltage at test point 2	–	–	0,065 x V_{CC}	V
	B	–	voltage at test point 2; note 5	0,2 x V_{CC}	0,25 x V_{CC}	0,3 x V_{CC}	V
	C	–	voltage at test point 2	0,85 x V_{CC}	–	–	V

Notes to system characteristics

1. Operation with minimum of 12 dB headroom; system remains functional to 6 V.
2. Attenuation between pins 2 and 3 of TEA0654 is 4 dB;
3. System headroom is determined by programmable monitor output level (pin 5 of TEA0654).
4. For a typical application see Fig. 10. Worst case considerations for the V_{CC} range from 8 V to 20 V limit the optional external resistor to maximum 6,8 kΩ, divided by number of switched channels.
5. In the open position (B) of the mode switch pin 14 of TEA0651/TEA0652 is pulled to typical 0,25 x V_{CC} by pin 4 of TEA0654.

SYSTEM GRAPHS

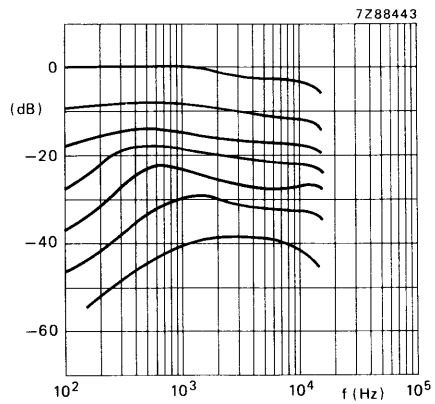


Fig. 3 Encoder frequency response for C-mode.

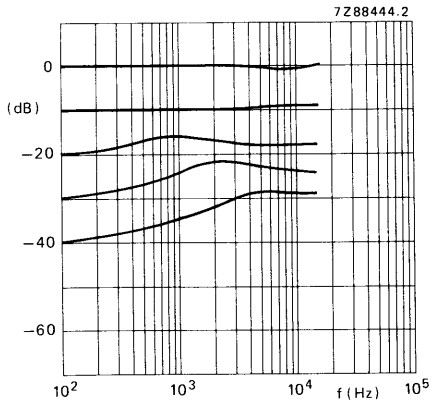


Fig. 4 Encoder frequency response for B-mode.

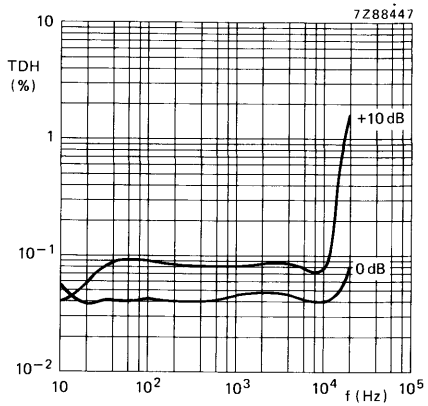


Fig. 5 Total harmonic distortion as a function of frequency for B-mode.

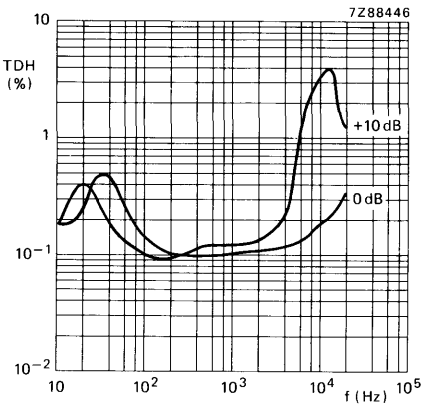


Fig. 6 Total harmonic distortion as a function of frequency for C-mode.

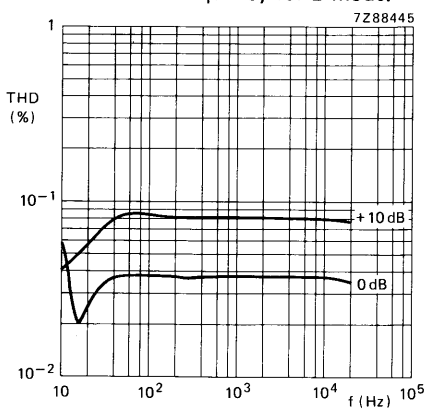


Fig. 7 Total harmonic distortion as a function of frequency for NR OFF-mode.

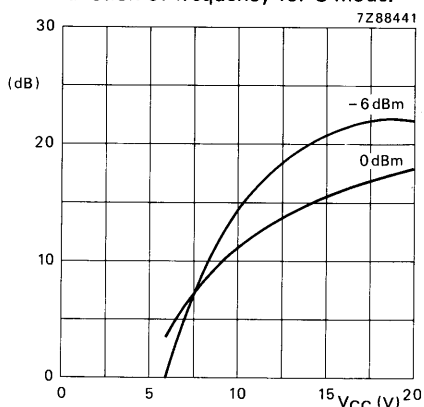


Fig. 8 Headroom at record output and line output (pins 14 and 5 of TEA0654); THD = 1%; f = 1 kHz, at line output levels 0 and −6 dB.

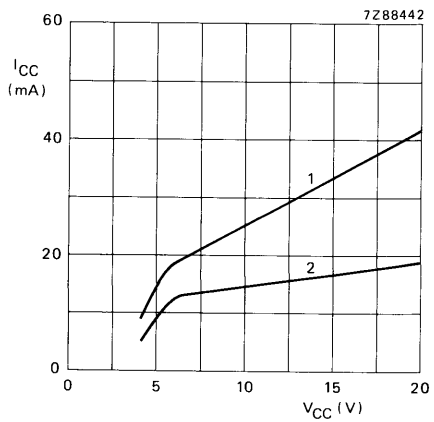


Fig. 9 Supply current as a function of supply voltage. 1: TEA0651/TEA0652 and TEA0654; 2: TEA0651/TEA0652 only.

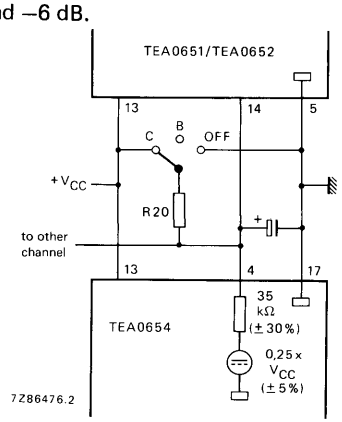


Fig. 10 Optional external time constant for mode switch.

TEA0651/TEA0652: DOLBY B/C TYPE NOISE REDUCTION PROCESSING CIRCUITS

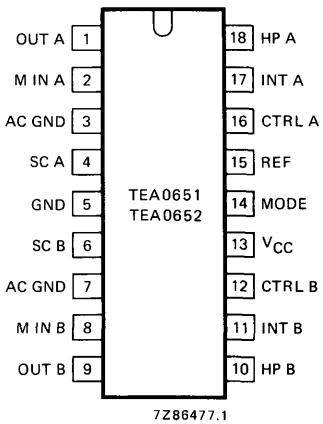


Fig. 11 Pinning diagram of TEA0651/TEA0652.

PINNING

1	OUT A	output channel A
2	M IN A	main chain input channel A
3	AC GND	a.c. ground channel A
4	SC A	side chain channel A
5	GND	ground
6	SC B	side chain channel B
7	AC GND	a.c. ground channel B
8	M IN B	main chain input channel B
9	OUT B	output channel B
10	HP B	high-pass filter channel B
11	INT B	integrating filter channel B
12	CTRL B	control voltage channel B
13	V_{CC}	positive supply voltage
14	MODE	mode B/C/NR OFF switch input
15	REF	reference voltage
16	CTRL A	control voltage channel A
17	INT A	integration filter channel A
18	HP A	high-pass filter channel A

Note

For Dolby-C type application channel A is the HIGH level stage and channel B is the LOW level stage.

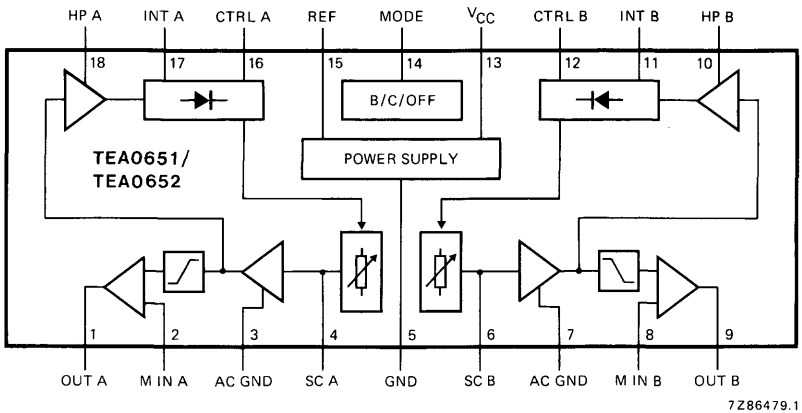


Fig. 12 Block diagram of TEA0651 and TEA0652.

CHARACTERISTICS FOR TEA0651/TEA0652

V_{CC} = 14 V; f = 20 Hz to 20 kHz; T_{amb} = 25 °C; all levels with reference to 387,5 mV = 0 dB = −6 dBm at test point 1; test circuit Fig. 13; record mode; unless otherwise specified.

parameter	conditions			min.	typ.	max.	unit
	mode	f(kHz)					
Supply voltage range	B	–	V_{CC}	8	14	20	V
Supply current I_{CC}	OFF	–	no input signal	–	17	25	mA
Power supply ripple rejection ratio	B	1	test circuit Fig. 14	–	60	–	dB
Voltage gain	OFF	1	note 1	−0,5	–	+ 0,5	dB
Signal handling at record output (note 4)	B	1	V_{CC} = 14 V THD = 1%	–	20	–	dB
		1	V_{CC} = 8 V THD = 1%	12	14	–	dB
		1	V_{CC} = 6 V THD = 1%	–	11	–	dB
Signal-to-noise ratio (S/N)	B	–	R_S = 10 kΩ, internal CCIR/ARM weighted	–	90	–	dB
Switching thresholds	OFF	–	voltage at pin 14	–	–	0,065 x V_{CC}	V
	B	–	voltage at pin 14	0,2 x V_{CC}	0,25 x V_{CC}	0,3 x V_{CC}	V
	C	–	voltage at pin 14	0,85 x V_{CC}	–	–	V
Switching threshold for stereo B appl.	B	–	voltage at pin 14	–	0,5 x V_{CC}	–	V
Channel matching	OFF	1	TPL = 0 dB notes 2, 3	−0,5	–	+ 0,5	dB
Channel separation	B	1	TPL = + 10 dB notes 2, 3	60	70	–	dB

Notes

1. Voltage gain is $20 \log \frac{\text{voltage at pin 1 (9)}}{\text{voltage at pin 2 (8)}}$.
2. TPL is Test Point Level.
3. Test circuit Fig. 15, reference level at channel A and channel B test point.
4. Operation with minimum of 12 dB headroom; system remains functional to 6 V.

CHARACTERISTICS TEA0651 ONLY

parameter	conditions			min.	typ.	max.	unit
	mode	f(kHz)					
Offset voltage	C	–	$\lvert V_{9\text{-}15} \rvert$	–	3	6	mV
Signal-to-noise ratio (S/N)	C	–	R_S = 10 kΩ (internal) CCIR/ARM weighted; pin 9	77	80	–	dB
Total harmonic distortion (THD)	B	10	TPL = 0 dB	–	–	0,1	%
			TPL = + 10 dB	–	0,05	0,1	%
Total harmonic distortion (THD)	C	10	TPL = 0 dB	–	–	0,1	%
		1	TPL = + 10 dB	–	0,15	0,5	%
B-mode frequency response	B	1	TPL = −20 dB	−17,3	−15,8	−14,3	dB
		2	TPL = −25 dB	−19,5	−18,0	−16,5	dB
		5	TPL = −40 dB	−30,2	−29,7	−28,2	dB
		10	TPL = −30 dB	−25,0	−23,5	−22,0	dB
C-mode frequency response	C	0,2	TPL = −40 dB	−32,9	−31,9	−30,9	dB
		0,5	TPL = −20 dB	−14,2	−13,7	−13,2	dB
		0,5	TPL = −30 dB	−18,7	−18,2	−17,7	dB
		1	TPL = −20 dB	−14,6	−14,1	−13,6	dB
		1	TPL = −30 dB	−19,1	−18,6	−18,1	dB
		1	TPL = −40 dB	−25,3	−23,8	−22,3	dB
		5	TPL = 0 dB	−3,3	−2,3	−1,3	dB
		5	TPL = −20 dB	−18,1	−17,1	−16,1	dB
		5	TPL = −30 dB	−22,6	−21,6	−20,6	dB
		5	TPL = −40 dB	−28,0	−26,5	−25,0	dB

CHARACTERISTICS TEA0652 ONLY

parameter	conditions			min.	typ.	max.	unit
	mode	f(kHz)					
Offset voltage	C	–	$\lvert V_{9\text{-}15}\rvert$	–	10	–	mV
Signal-to-noise ratio (S/N)	C	–	R_S = 10 kΩ (internal) CCIR/ARM weighted; pin 9	72	80	–	dB
Total harmonic distortion (THD)	B	10	TPL = 0 dB	–	0,05	0,1	%
			TPL = + 10 dB	–	0,08	0,3	%
Total harmonic distortion (THD)	C	10	TPL = 0 dB	–	0,1	0,3	%
		1	TPL = + 10 dB	–	0,15	0,5	%
B-mode frequency response	B	1	TPL = −20 dB	−17,3	−15,8	−14,3	dB
		2	TPL = −25 dB	−19,5	−18,0	−16,5	dB
		5	TPL = −40 dB	−30,2	−29,7	−28,2	dB
		10	TPL = −30 dB	−25,0	−23,5	−22,0	dB
C-mode frequency response	C	0,2	TPL = −40 dB	−33,4	−31,9	−30,4	dB
		0,5	TPL = −20 dB	−15,7	−13,7	−11,7	dB
		0,5	TPL = −30 dB	−20,2	−18,2	−16,2	dB
		1	TPL = −20 dB	−16,1	−14,1	−12,1	dB
		1	TPL = −30 dB	−20,1	−18,6	−17,1	dB
		1	TPL = −40 dB	−25,8	−23,8	−21,8	dB
		5	TPL = 0 dB	−3,8	−2,3	−0,8	dB
		5	TPL = −20 dB	−19,1	−17,1	−15,1	dB
		5	TPL = −30 dB	−23,6	−21,6	−19,6	dB
		5	TPL = −40 dB	−28,5	−26,5	−24,5	dB

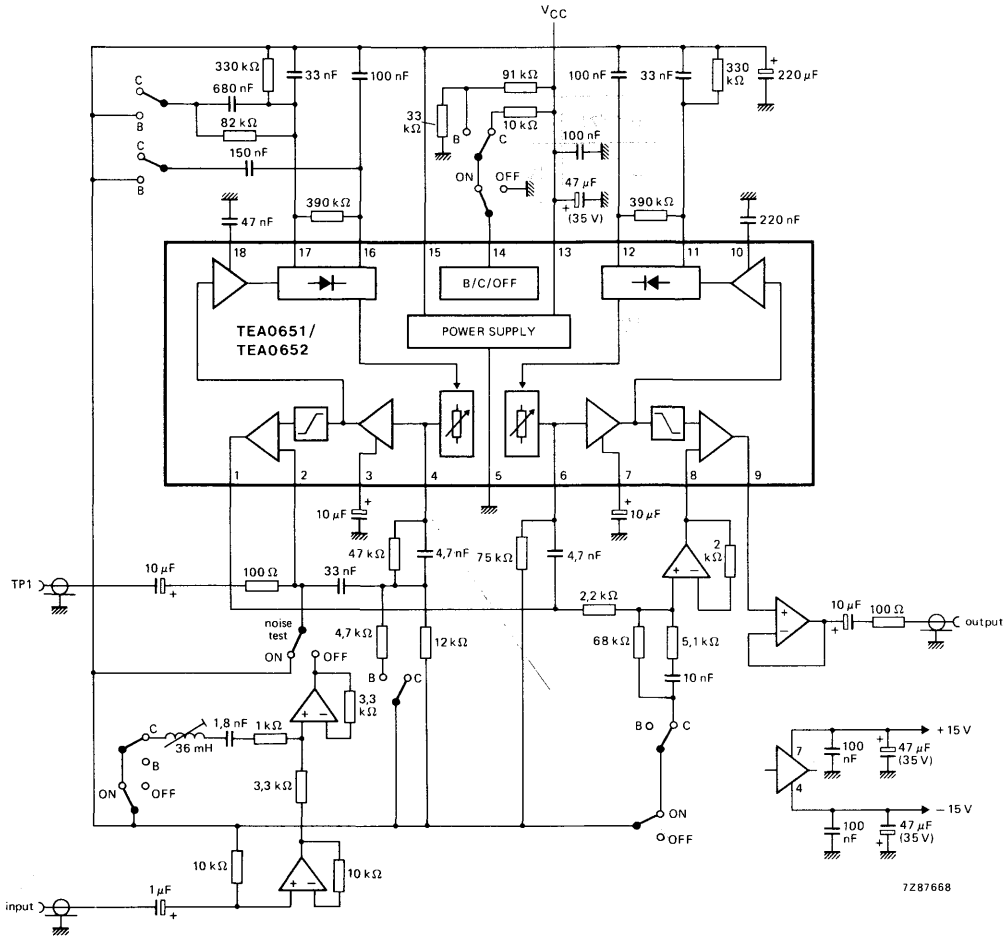


Fig. 13 Test circuit for TEA0651/0652. Encode mode.
Operational amplifiers are NE5535.

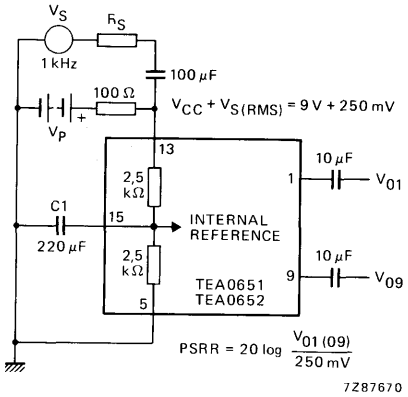


Fig. 14 Test circuit for PSRR for TEA0651/TEA0652.

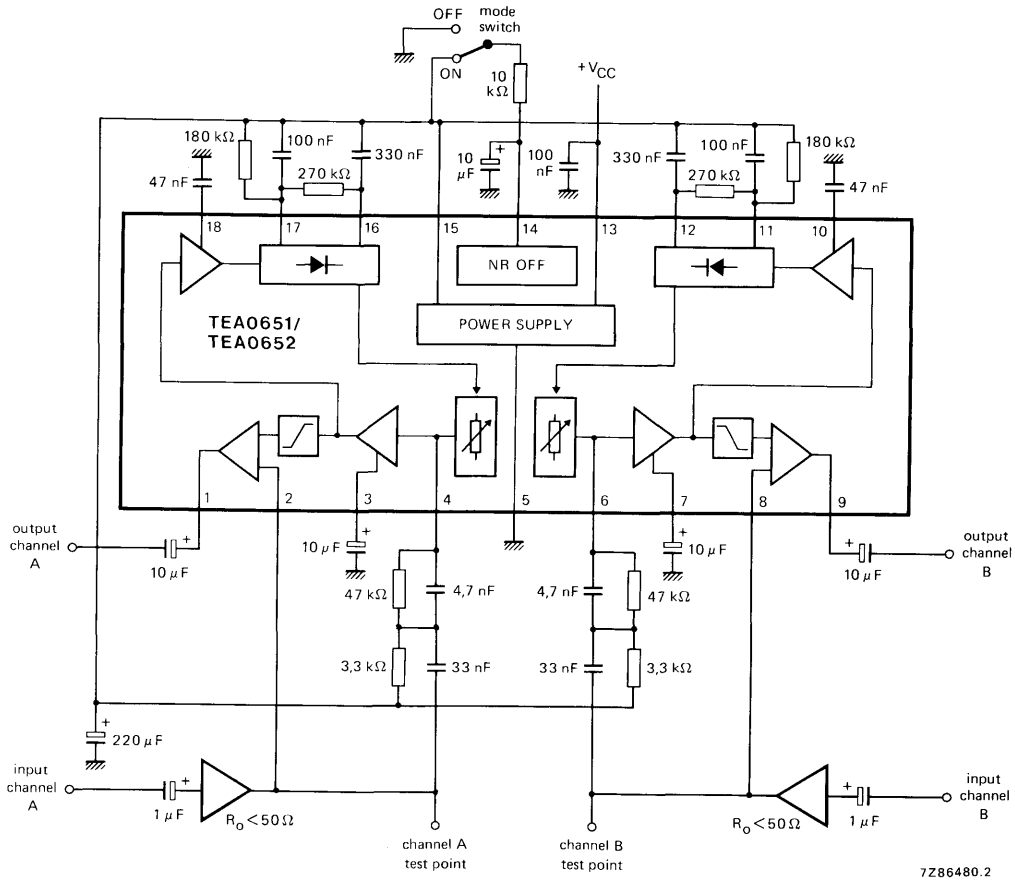


Fig. 15 Test and application circuit of TEA0651/TEA0652 for stereo Dolby B application, shown in encode mode.

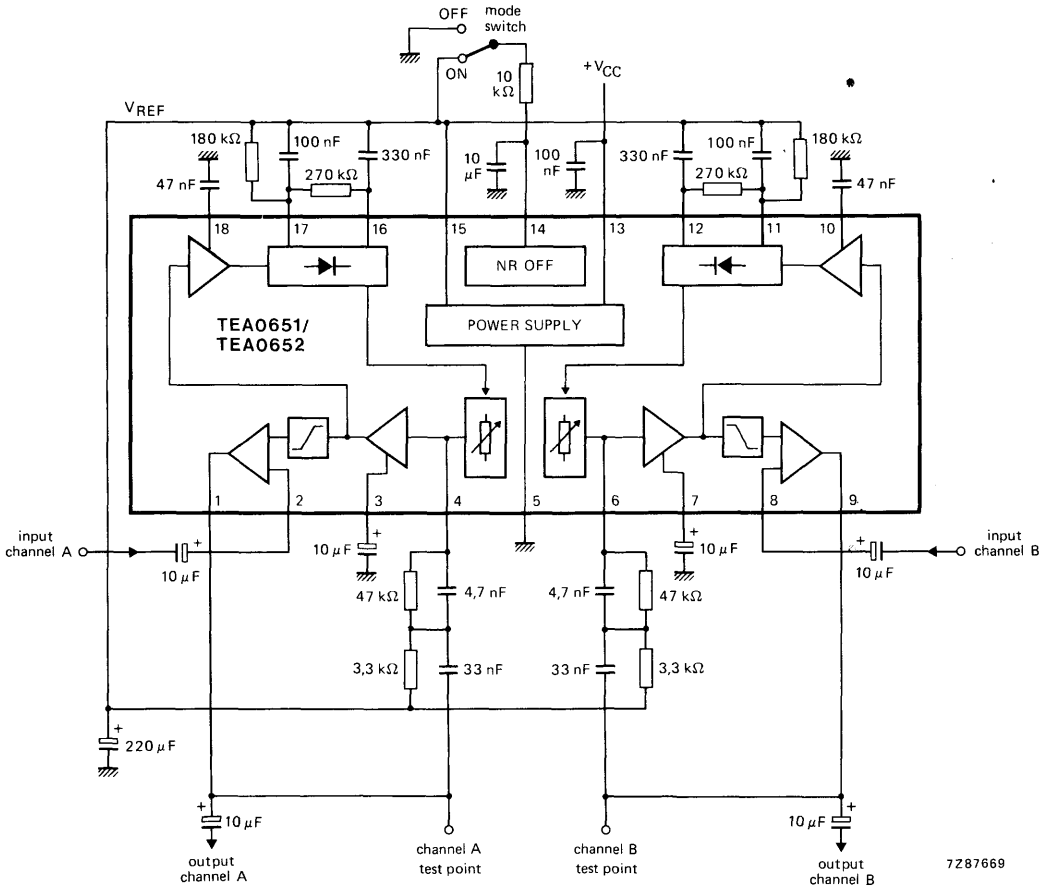


Fig. 16 Typical application circuit for stereo Dolby B noise reduction shown in decode mode.

DATA OF TEA0654 DOLBY B & C TYPE NR SWITCHING CIRCUIT

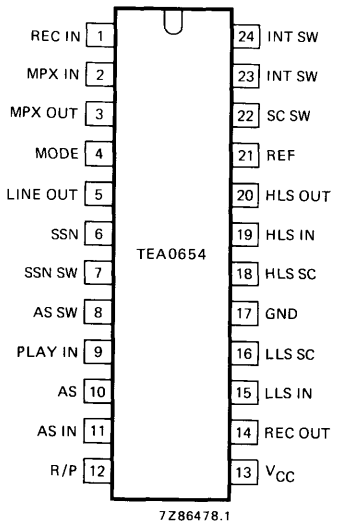


Fig. 17 Pinning diagram of TEA0654.

PINNING

1	REC IN	record input
2	MPX IN	multiplex filter input
3	MPX OUT	multiplex filter output
4	MODE	mode B/C/NR OFF switch input
5	LINE OUT	line output
6	SSN	spectral skewing network
7	SSN SW	spectral skewing network switch
8	AS SW	anti-saturation filter switch
9	PLAY IN	playback input
10	AS	anti-saturation filter
11	AS IN	anti-saturation filter input
12	R/P	record/playback switch input
13	V_{CC}	positive supply voltage
14	REC OUT	record output
15	LLS IN	low level stage main chain input
16	LLS SC	low level stage side chain input
17	GND	d.c. ground
18	HLS SC	high level stage side chain input
19	HLS IN	high level stage main chain input
20	HLS OUT	high level stage output
21	REF	reference voltage
22	SC SW	side chain filter switch
23	INT SW	integrating filter switch
24	INT SW	integrating filter switch

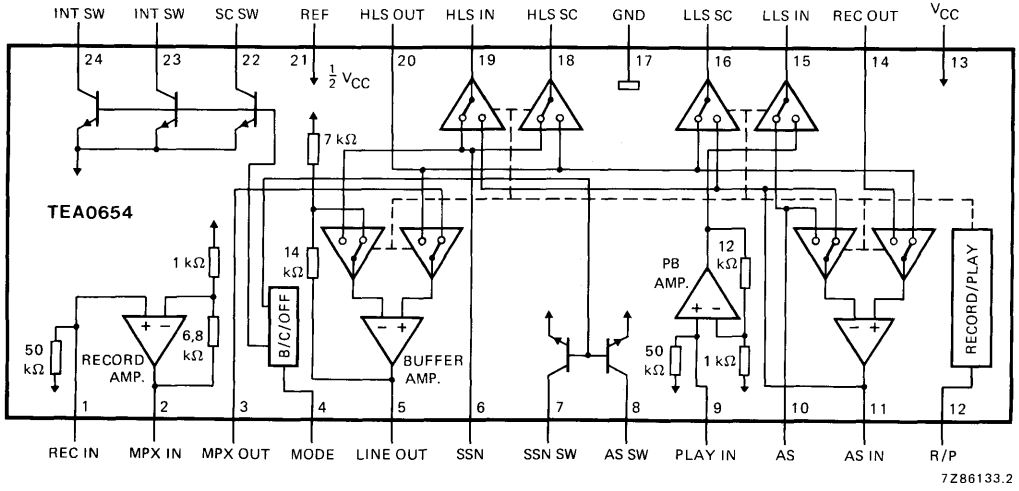


Fig. 18 Block diagram of TEA0654.

CHARACTERISTICS FOR TEA0654

V_{CC} = 14 V; f = 10 kHz; T_{amb} = 25 °C; test circuit Fig. 20; signals referenced to REF (pin 21); d.c. levels with reference to GND (pin 17); unless otherwise specified.

parameter	conditions	min.	typ.	max.	unit
Supply voltage range	V_{CC} (output level at buffer amplifier is + 6 dBm; Dolby level is −6 dBm)	8	14	20	V
Supply current	I_{CC}	11	17	23	mA
Voltage gain of record amplifier	pins 1 to 2	–	17,85	–	dB
Input sensitivity of record amplifier (pin 1)	buffer amplifier output level (pin 5) is 775 mV r.m.s.; MPX filter insertion loss is 4 dB	43	50	58	mV
Voltage gain of playback amplifier	pins 9 to 5	–	22,25	–	dB
Input sensitivity of playback amplifier	buffer amplifier output level (pin 5) is 775 mV r.m.s.	25	30	35	mV
Input resistance	pin 1 and 9	35	50	65	kΩ
Output noise at record output pin 14	R_S = 10 kΩ at pin 1; CCIR/ARM weighted; record mode	–	20	40	μV
Signal handling record and buffer amplifier; pins 2 and 5 (r.m.s. value)	THD = 1%; record mode input level at pin 1	4	–	–	V
Voltage gain of signal switches	record: pins 6 to 14	–	0	–	dB
	playback: pins 14 to 20	–	0	–	dB
Output noise at buffer amplifier pin 5 (r.m.s. value)	R_S = 10 kΩ at pin 9; CCIR/ARM weighted; playback mode	–	65	130	μV
Voltage gain difference between main and side chain op-amp	main chain op-amp output: pins 19 and 15; side chain op-amp output: pins 18 and 16; adjacent op-amps: pins 19 and 18, pins 15 and 16	−0,3	0	+ 0,3	dB
Output noise of signal switches pins 11, 15, 16, 18, 19	R_S = 1 kΩ at pins 6, 14, 20; CCIR/ARM weighted; Fig. 19	–	2,5	–	μV
Signal handling of switches (pin 14) (r.m.s. value)	THD = 1% at pin 14; input level at pin 1	2	–	–	V
Voltage gain of buffer amplifier	pins 3 to 5	–	10	–	dB

parameter	conditions	min.	typ.	max.	unit
Input noise of buffer amplifier pin 3 (r.m.s. value)	R_S = 2,2 kΩ at pin 3; CCIR/ARM weighted; Fig. 19	–	2	–	μV
Signal handling buffer amplifier pin 5 (r.m.s. value)	THD = 1% at pin 5; playback mode; input level at pin 9	4	–	–	V
Output impedance at buffer amplifier pin 5		–	–	100	Ω
Load resistance at buffer amplifier pin 5		10	–	–	kΩ
Load capacitance at buffer amplifier pin 5	For large capacitive loads a series resistor of about 220 Ω is necessary (see Fig. 2)	–	–	200	pF
D.C. switch control levels	playback: pin 12	0	–	1	V
	record: pin 12	$V_{CC}-1$	–	V_{CC}	V
	Dolby-C: pin 4	$\frac{3}{4}V_{CC}+1$	–	V_{CC}	V
	Dolby-B: pin 4	0	–	$\frac{3}{4}V_{CC}-1$	V

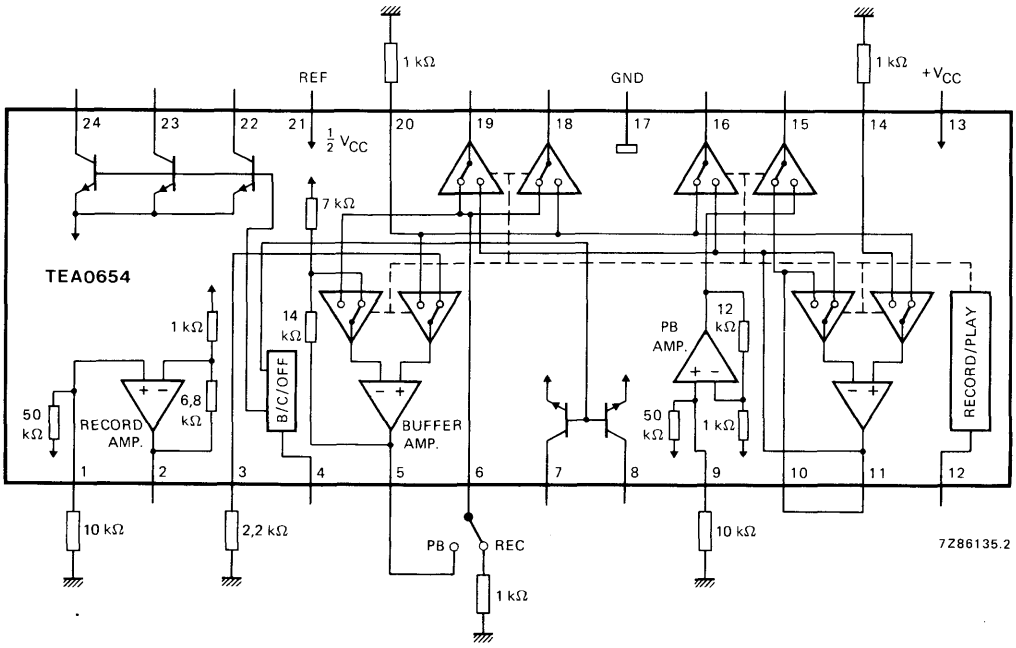


Fig. 19 Test circuit for noise measurements; switch in record position.

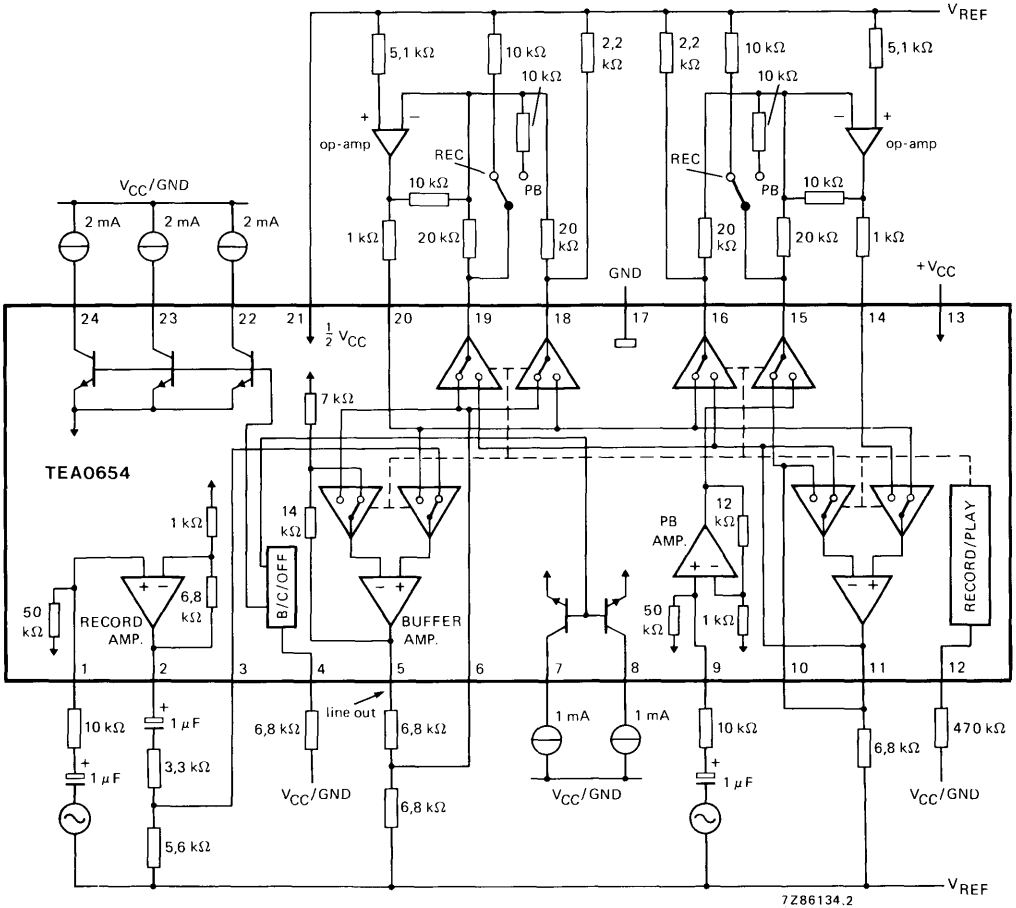


Fig. 20 Test circuit for $V_{CC} \geqslant 11{,}5$ V; switches in record position; external operational amplifier e.g. AD506LH.

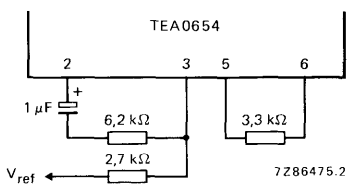


Fig. 21 Modification of Fig. 20 for $V_{CC} \leqslant 11{,}5$ V.

DOLBY B TYPE NOISE REDUCTION CIRCUIT

GENERAL DESCRIPTION

The TEA0653T is a monolithic bipolar IC designed for use in Dolby B type audio Noise Reduction (NR) systems. The device is a dual channel circuit.

Applications

- Automotive cassette players
- Home cassette decks
- Portable cassette players
- Video cassette recorders
- FM receivers

Features

- Dual processors provide optimum matching of channels
- No law adjustments required
- Full wave rectifier
- No capacitor required for side chain filter
- Electronic switching for NR ON/OFF
- Reference level 0 dB = 387,5 mV
- Minimum external components
- Easy to apply in 2 or 3 head systems
- Split supply operation is optional

QUICK REFERENCE DATA

Supply voltage	max.	20 V
Supply current	typ.	17 mA
Signal-to-noise ratio	typ.	90 dB
Storage temperature range		−55 to +150 °C
Operating ambient temperature range		−30 to +85 °C

PACKAGE OUTLINES

TEA0653T: 20-lead mini-pack; plastic (SO28; SOT136A).

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Fancisco, CA94111, U.S.A., from whom licensing and application information must be obtained. Dolby is a registered trademark of Dolby Laboratories Licensing Corporation.

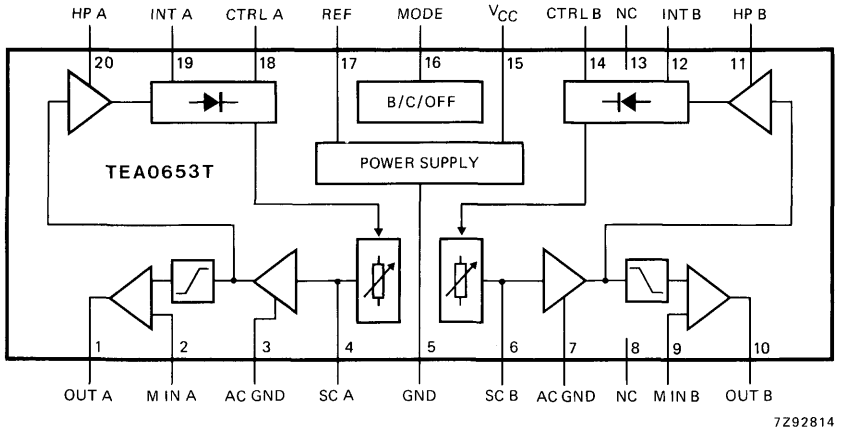


Fig. 1 Block diagram.

PINNING

1	OUT A	output channel A
2	M IN A	main chain input channel A
3	AC GND	a.c. ground channel A
4	SC A	side chain channel A
5	GND	ground
6	SC B	side chain channel B
7	AC GND	a.c. ground channel B
8	N.C.	no connection
9	M IN B	main chain input channel B
10	OUT B	output channel B
11	HP B	high-pass filter channel B
12	INT B	integrating filter channel B
13	N.C.	no connection
14	CTRL B	control voltage channel B
15	V_{CC}	positive supply voltage
16	MODE	mode B/NR OFF switch input
17	REF	reference voltage
18	CTRL A	control voltage channel A
19	INT A	integration filter channel A
20	HP A	high-pass filter channel A

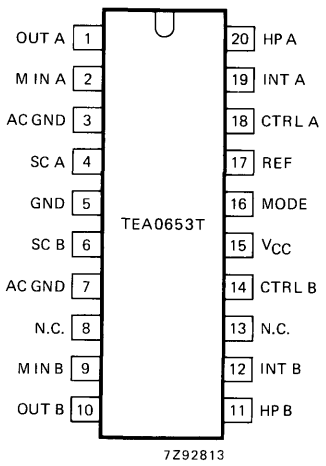


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

Supply voltage pin 15	V_{CC}	8 to 20 V
Storage temperature range	T_{stg}	−55 to +150 °C
Operating ambient temperature range	T_{amb}	−30 to +85 °C

CHARACTERISTICS

V_{CC} = 14 V; f = 20 Hz to 15 kHz; T_{amb} = 25 °C; all levels with reference to 387,5 mV = 0 dB = −6 dBm at test point A or B; test circuit Fig. 4; encode mode; unless otherwise specified.

parameter	conditions			min.	typ.	max.	unit
	mode	f(kHz)					
Supply							
Supply voltage range	B	–	V_{CC} (note 4)	8	14	20	V
Supply current I_{CC}	OFF	–	no input signal	–	17	25	mA
Power supply ripple rejection ratio	B	1	test circuit Fig. 3	–	60	–	dB
Voltage gain	OFF	1	note 1	−0,5	–	+0,5	dB
Signal handling at output (note 4)	B	1	V_{CC} = 14 V THD = 1%	–	20	–	dB
		1	V_{CC} = 8 V THD = 1%	12	14	–	dB
		1	V_{CC} = 6 V THD = 1%	–	11	–	dB
Signal-to-noise ratio (S/N)	B	–	R_S = 10 kΩ internal CCIR/ARM weighted	–	90	–	dB
Switching thresholds	OFF	–	voltage at pin 16	–	–	0,065 xV_{CC}	V
Switching threshold for stereo B appl.	B	–	voltage at pin 16	–	0,5 xV_{CC}	–	V
Channel matching	OFF	–	TPL = 0 dB notes 2, 3	−0,5	–	+0,5	dB
Channel separation	B	1	TPL = 10 dB notes 2, 3	60	70	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions			min.	typ.	max.	unit
	mode	f(kHz)					
Total harmonic distortion (THD)	B	10	TPL = 0 dB	–	0,05	0,1	%
			TPL = +10 dB	–	0,08	0,3	%
B-mode frequency response	B	1	TPL = −20 dB	−17,3	−15,8	−14,3	dB
		2	TPL = −25 dB	−19,5	−18,0	−16,5	dB
		5	TPL = −40 dB	−30,2	−29,7	−28,2	dB
		10	TPL = −30 dB	−25,0	−23,5	−22,0	dB

Notes

1. Voltage gain is $20 \log \frac{\text{voltage at pin 1 (10)}}{\text{voltage at pin 2 (9)}}$
2. TPL is Test Point Level.
3. Test circuit Fig. 3, reference level at channel A and channel B test point.
4. Operation with minimum of 12 dB headroom; system remains functional to 6 V.

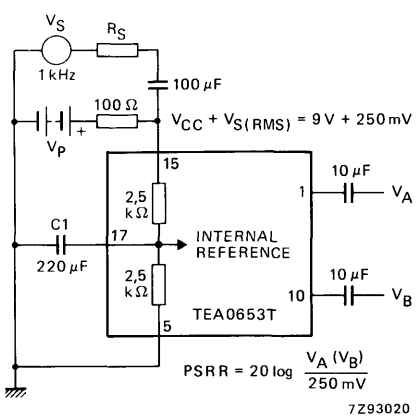


Fig. 3 Test circuit for PSSR for TEA0653T.

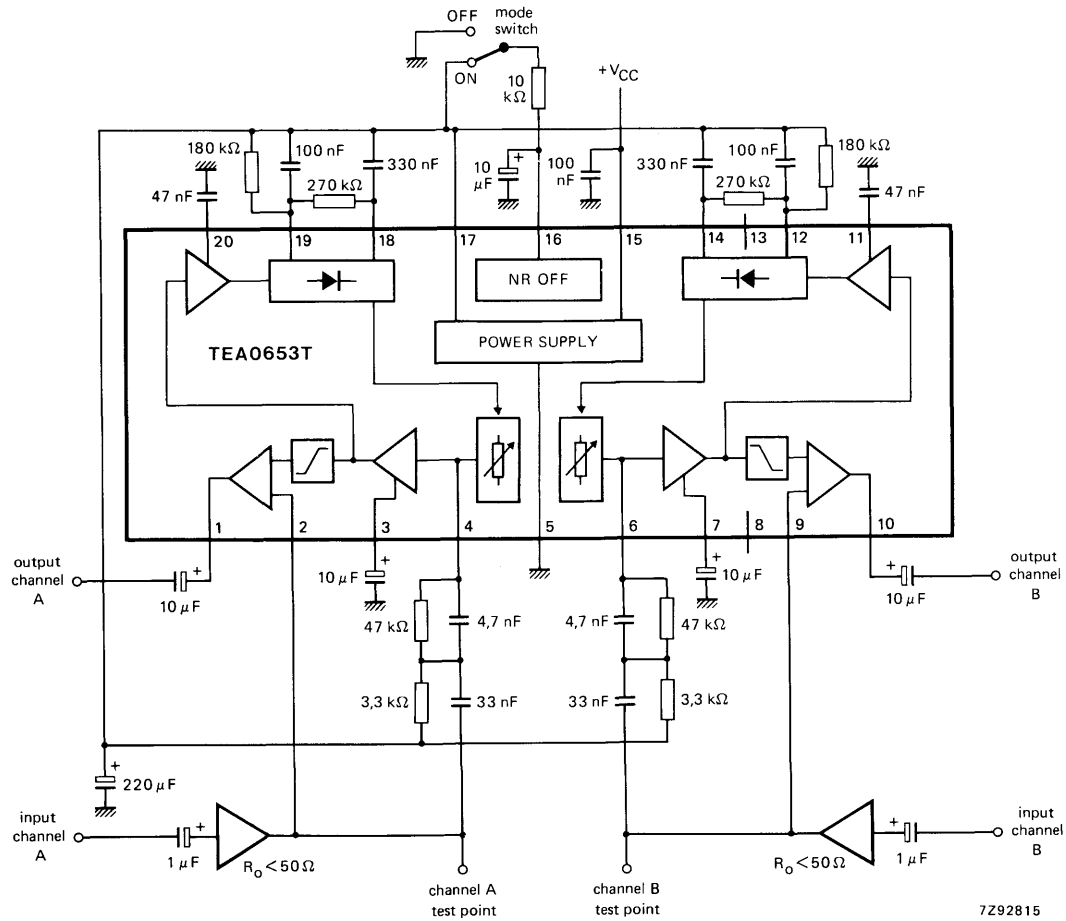


Fig. 4 Test and application circuit for stereo Dolby B, shown in encode mode.

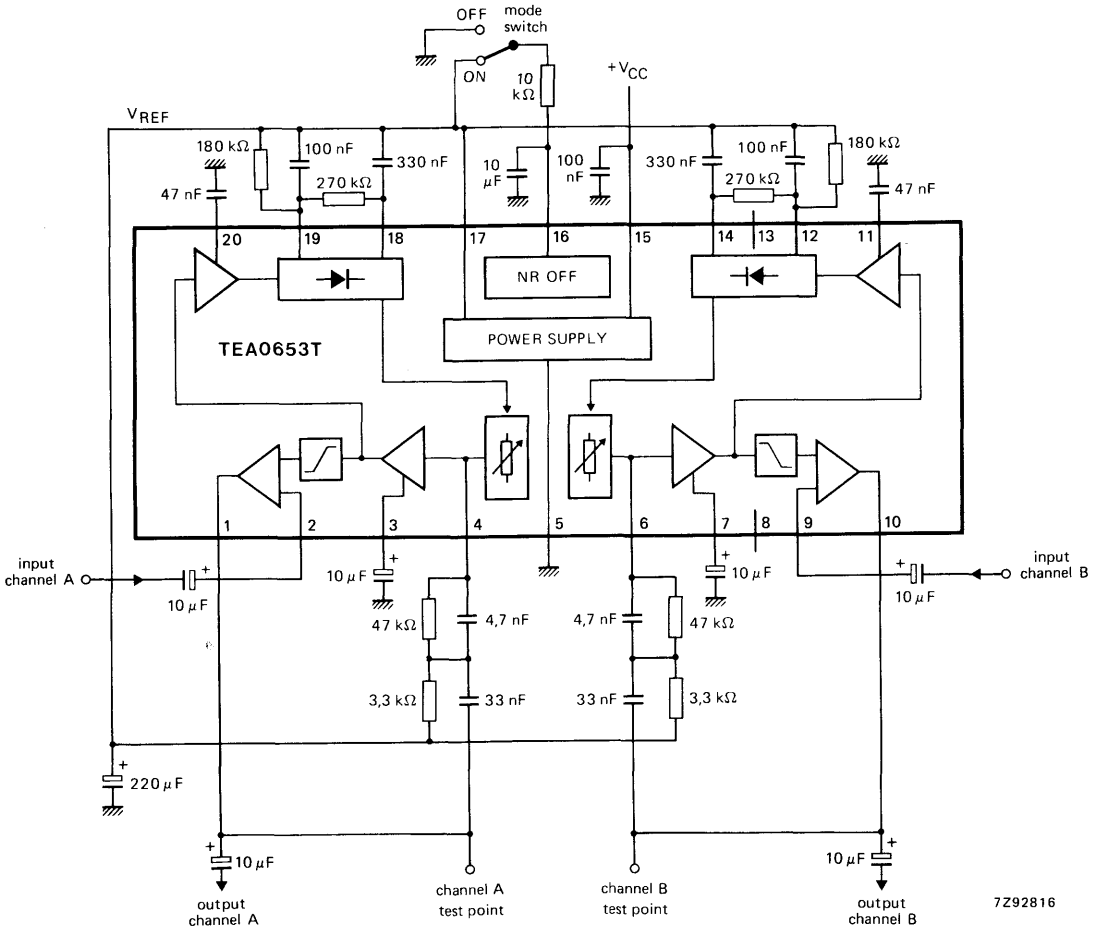


Fig. 5 Application circuit for stereo Dolby B, shown in decode mode.

DUAL DOLBY* B–TYPE NOISE REDUCTION CIRCUIT

GENERAL DESCRIPTION

The TEA0657 is a monolithic bipolar integrated circuit providing two channels of Dolby B-type noise reduction. The circuit contains all internal electronic switching to provide playback or record functions.

In addition the TEA0657 includes preamplifiers for the playback and record modes and multiplex filter buffers for both channels.

The device will operate with power supplies in the range of 9.0 V to 15.0 V, output overload level increasing with increase in supply voltage. Current drain varies with supply voltage and noise reduction ON/OFF so it is advisable to use a regulated power supply or, a supply with a long time constant.

Features

- Dual noise reduction channels
- Full playback/record switching
- Separate playback/record inputs
- Multiplex filter buffers
- Simultaneous switching on both channels
- Dual or single supply operations
- Dolby reference level = 580 mV
- Input sensitivity = 30 mV

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{CC}	9.0	–	15.0	V
Supply current	I_{CC}	–	19	–	mA
Signal plus noise to noise ration					
record mode	(S+N)/N	–	72	–	dB
playback mode	(S+N)/N	–	90	–	dB

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, U.S.A., from whom licensing and application information must be obtained.
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PACKAGE OUTLINE

24-lead DIL; plastic (SOT101B).

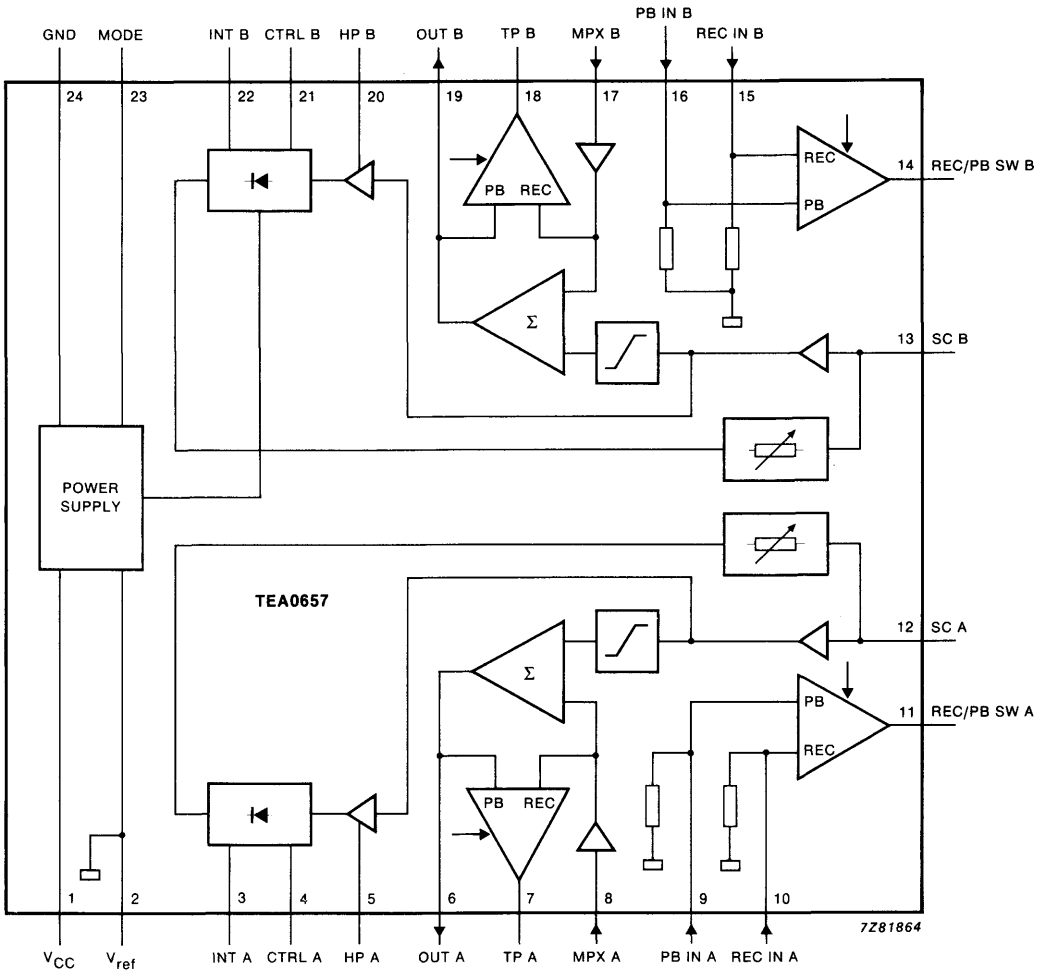


Fig. 1 Block diagram.

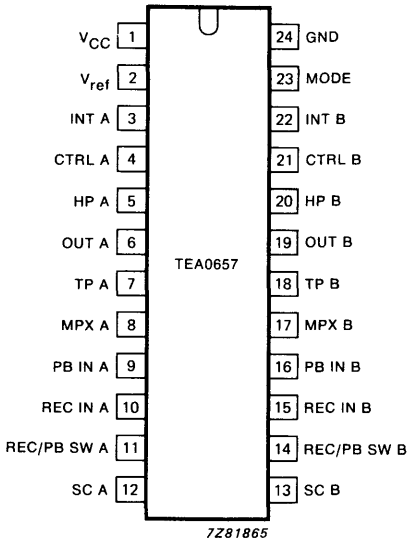


Fig. 2 Pinning diagram.

1	V_{CC}	supply voltage
2	V_{ref}	reference voltage
3	INT A	integrating filter channel A
4	CTRL A	control voltage channel A
5	HP A	high-pass filter channel A
6	OUT A	output channel A
7	TP A	test point channel A, line output channel A
8	MPX A	multiplex buffer channel A
9	PB IN A	playback input channel A
10	REC IN A	record input channel A
11	REC/PB SW A	record/playback switch channel A
12	SC A	side chain channel A
13	SC B	side chain channel B
14	REC/PB SW B	record/playback switch channel B
15	REC IN B	record input channel B
16	PB IN B	playback input channel B
17	MPX B	multiplex buffer input channel B
18	TP B	test point channel B, line output channel B
19	OUT B	output channel B
20	HP B	high-pass filter channel B
21	CTRL B	control voltage channel B
22	INT B	integrating filter channel B
23	MODE	record/playback select switch
24	GND	ground

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Noise reduction is enabled when pin 22 is open-circuit and OFF when connected to pin 24 via a 5.1 kΩ resistor (see Fig. 3).
Pin 24 performs the functions of a logic input for noise reduction switching in both channels and provides smoothing for the control signal in one channel. It is important that no voltage is applied to this pin when in the NR ON mode as this will cause irregular noise reduction characteristics in the selected channel.

Record/playback is achieved by applying a DC voltage to pin 23. The circuit will enable the appropriate input for the selected mode.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	–	16.0	V
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	–	+ 150	°C
Input voltage (pin 1)	V_I	−0,3	V_{CC}	V
Electrostatic handling (note 1)				

Note to the ratings

Note 1, Classification A:

Human body model; C = 100 pF; R = 1.5 kΩ; V ⩾ 2 kV.
Charge device model; C = 200 pF; R = 0 Ω; V ⩾ 500 V.

DEVELOPMENT DATA

CHARACTERISTICS

V_{CC} = 12 V; f = 20 Hz to 20 kHz; T_{amb} = + 25 °C; all levels referenced to 580 mV RMS (0 dB) at TP (pin 7 or 18); test circuit Fig. 4; Record mode; NR ON; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{CC}	9	12	15	V
Supply current		I_{CC}	–	19	–	mA
Voltage gain (pins 9 or 10 to 11)	f = 1 kHz	G_v	–	20	–	dB
Voltage gain (pins 8 to 7)	f = 1 kHz	G_v	–	9	–	dB
Channel matching	NR OFF		−0.5	–	+ 0.5	dB
Distortion						
2nd and 3rd harmonic	f = 1 kHz, 0 dB	THD	–	0.08	0.15	%
	f = 10 kHz, + 10 dB	THD	–	0.15	0.3	%
Signal handling; (V_{CC} = 9 V)	1% distortion at 1 kHz		12	–	–	dB
Signal-to-noise plus noise ratio						
record mode	internal CCIR ARM weighted	(S+N)/N	–	72	–	dB
playback mode	R_S = 10 kHz	(S+N)/N	–	90	–	dB
Supply voltage ripple rejection	f = 1 kHz; 250 mV	SVRR	–	40	–	dB
Frequency response, (referenced to TP)	f = 1 kHz;					
	0 dB	Δf	−1.5	–	−1.5	dB
	−20 dB	Δf	−17.3	−15.8	−14.3	dB
	f = 5 kHz					
	−30 dB	Δf	−23.3	−21.8	−20.3	dB
	−40 dB	Δf	−30.2	−29.7	−28.2	dB
	f = 10 kHz					
	0 dB	Δf	−1.1	0.4	1.9	dB
	−30 dB	Δf	−25.0	−23.5	−22.5	dB
Input resistance; (pins 9, 10, 15 and 16)		R_I	–	50	–	kΩ
Channel separation	0 dB at TP; f = 1 kHz	α_{cr}	–	65	–	dB
Back-to-back frequency response shift;						
as a function of T_{amb}	0 to −70 °C		–	± 0.5	–	dB
as a function of V_{CC}	9 V to 15 V		–	± 0.5	–	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
PB/REC separation	30 mV; 1 kHz; at playback input, measure V_{OUT}	$\alpha_{PB/REC}$	–	72	–	dB
Minimum load resistance on output; (pins 6 and 9)	12 dB; 1 kHz; 1% THD	R_{Lmin}	10	–	–	kΩ
Switching thresholds	V_{PB}					
playback; pin 23		V_{PB}	0.7 V_{CC}	V_{CC}	–	V
record; pin 28		V_{REC}	–	GND	0.4 V_{CC}	V
NR OFF; pin 22		V_{OFF}	–	–	0.2 V_{CC}	V

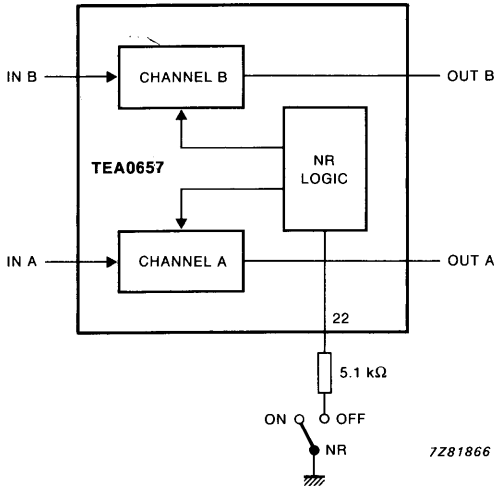
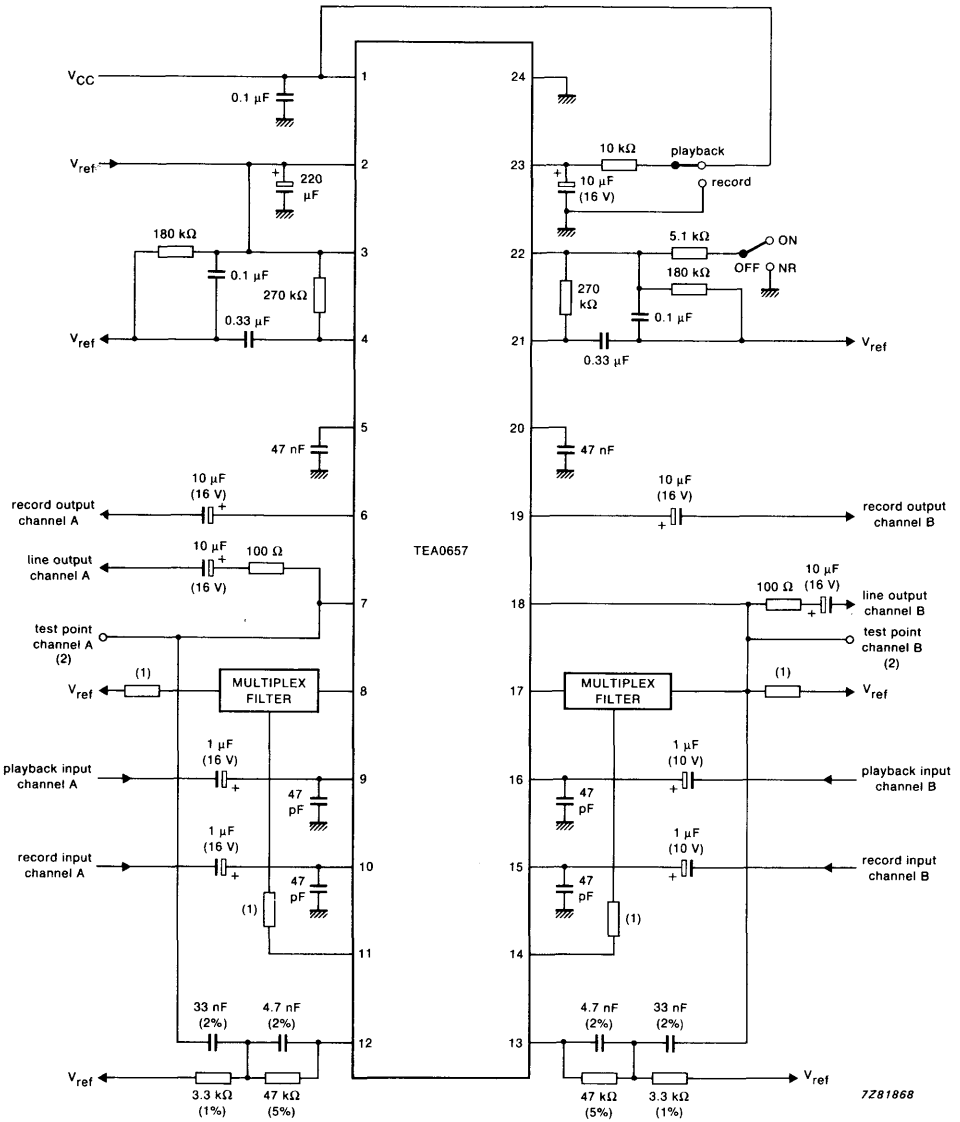


Fig. 3 External NR switch circuit for TEA0657.

DEVELOPMENT DATA



All values within ± 10% unless otherwise specified.

Notes:

(1) Value determined by multiplexer in use.
(2) Dolby level = 580 mV at test points.

Fig. 4 Test and application circuit.

DOLBY* B and C TYPE NOISE REDUCTION CIRCUIT

GENERAL DESCRIPTION

The TEA0665 is designed for use in Dolby B and Dolby C type audio Noise Reduction (NR) systems. The device provides the high and low level stages for one channel of a Dolby C-type NR system, including NR ON/OFF switching and all electronic switching necessary for Dolby C-type systems. In addition the TEA0665 includes a preamplifier for the record and playback functions and a multiplex buffer amplifier. The circuit offers two different line-output levels (−6 and 0 dBm) and a low-pass filter, which can be fed into the signal path in playback mode.

Features

- Few external components required
- Included RECORD/PLAY preamplifiers plus multiplex filter buffer amplifier
- Two different line-output levels
- All electronic switching

PACKAGE OUTLINES

TEA0665: 28-lead DIL; plastic (SOT117).
TEA0665T: 28-lead mini-pack; plastic (SO28; SOT136A).

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, U.S.A., from whom licensing and application information must be obtained.
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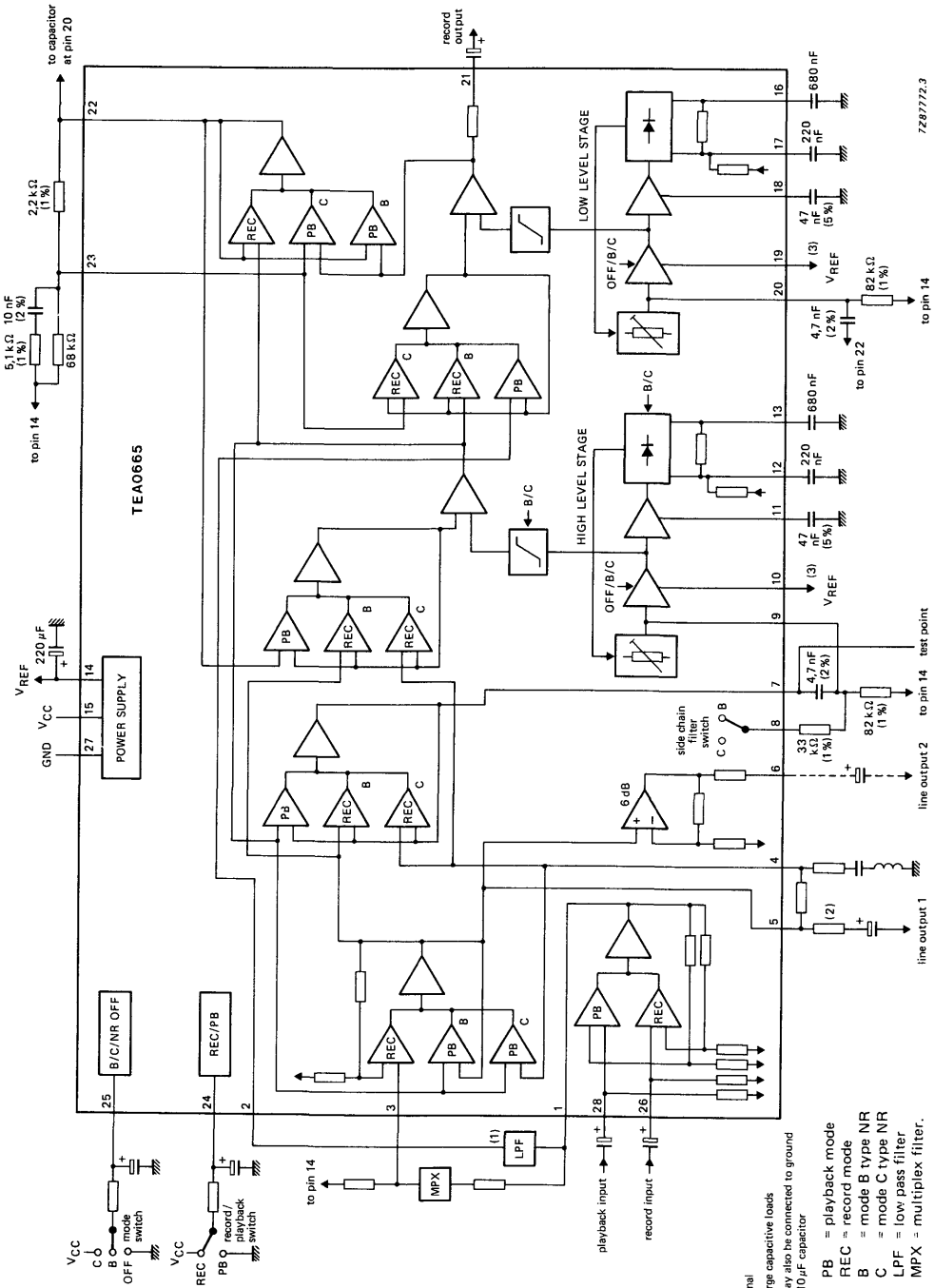


(1) optional
(2) for large capacitive loads
(3) pin may also be connected to ground via a 10 µF capacitor

Where: PB = playback mode
REC = record mode
B = mode B type NR
C = mode C type NR
LPF = low pass filter
MPX = multiplex filter.

Fig. 1 Block diagram and application circuit.

DEVELOPMENT DATA

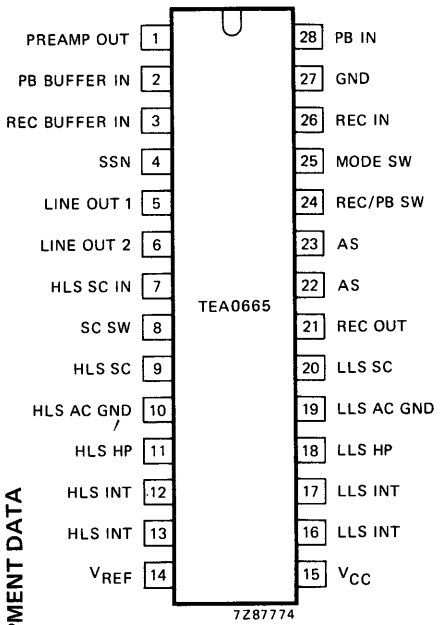


Fig. 2 Pinning diagram.

PINNING

1	PREAMP OUT	record/playback preamplifier output
2	PB BUFFER IN	playback amplifier input buffer
3	REC BUFFER IN	record amplifier input buffer
4	SSN	spectral skewing network
5	LINE OUT 1	line output 1
6	LINE OUT 2	line output 2
7	HLS SC IN	high level stage side chain input
8	SC SW	side chain filter switch
9	HLS SC	high level stage side chain
10	HLS AC GND	high level stage AC ground
11	HLS HP	high level stage high pass filter
12	HLS INT	high level stage integrating filter
13	HLS INT	high level stage integrating filter
14	V_{REF}	reference voltage
15	V_{CC}	positive supply voltage
16	LLS INT	low level stage integrating filter
17	LLS INT	low level stage integrating filter
18	LLS HP	low level stage high pass filter
19	LLS AC GND	low level stage AC ground
20	LLS SC	low level stage side chain
21	REC OUT	record output
22	AS	anti-saturation filter
23	AS	anti-saturation filter
24	REC/PB SW	record/playback switch input
25	MODE SW	mode switch input
26	REC IN	record input
27	GND	ground
28	PB IN	playback input

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	V_{CC}	max. 18	V
Input voltage (pins 26 and 28)	V_I	max. −0,3 to V_{CC}	V
Total power dissipation	P_{tot}	600	mW
Storage temperature range	T_{stg}	−55 to + 150	°C
Operating ambient temperature range	T_{amb}	−40 to + 85	°C

CHARACTERISTICS

V_{CC} = 14 V; f = 20 Hz to 15 kHz; T_{amb} = 25 °C; all levels with reference to 387,5 mV = 0 dB = −6 dBm at test point pin 7; test circuit Fig. 5; record mode; unless otherwise specified.

parameter	conditions			symbol	min.	typ.	max.	unit
	mode	f (kHz)						
Supply								
Supply voltage range	C	–	note 1					
single				V_{CC}	8	14	16	V
(split)				V_{CC}	(± 4)	(± 7)	(± 8)	V
Supply current	OFF	–	no input signal	I_{CC}	–	17	25	mA
Input sensitivity	C		note 2					
of record amplifier			pin 26	V_i	43	50	57	mV
of playback amplifier			pin 28	V_i	25	30	35	mV
Signal handling	C	1	V_{CC} = 8 V					
of record output			THD = 1%		12	15	–	dB
(note 3; see Fig. 8)		1	V_{CC} = 14 V					
			THD = 1%		–	20	–	dB
Line output 1			note 3		−0,5	0	+ 0,5	dB
Line output 2; amplifier gain V_o/V_i (pin 6 to pin 5)				G_v	+ 5,5	+ 6	+ 6,5	dB
Total harmonic distortion	OFF	1	TPL = 0 dB*	THD	–	0,02	0,1	%
			TPL = + 10 dB	THD	–	0,05	0,3	%
Total harmonic distortion	B	1	TPL = 0 dB	THD	–	0,1	0,15	%
			TPL = + 10 dB	THD	–	0,08	0,3	%
		10	TPL = 0 dB	THD	–	0,06	0,1	%
Total harmonic distortion	C	1	TPL = 0 dB	THD	–	0,15	0,3	%
			TPL = + 10 dB	THD	–	0,13	0,5	%
Signal plus noise-to-noise ratio	C		R_S = 10 kΩ CCIR/ARM weighted	(S+N)/N	62	66	–	dB

* TPL is Test Point Level.

DEVELOPMENT DATA

parameter	conditions			symbol	min.	typ.	max.	unit
	mode	f (kHz)						
Frequency response	B	2	TPL = −25 dB		−19,0	−18,0	−17,0	dB
		5	TPL = −40 dB		−30,7	−29,7	−28,7	dB
		10	TPL = −30 dB		−24,5	−23,5	−22,5	dB
	C	0,2	TPL = −40 dB		−33,4	−31,9	−30,4	dB
		1	TPL = −30 dB		−20,1	−18,6	−17,1	dB
		1	TPL = −20 dB		−16,1	−14,1	−12,1	dB
		5	TPL = −0 dB		−3,8	−2,3	−0,8	dB
		5	TPL = −20 dB		−19,1	−17,1	−15,1	dB
		5	TPL = −40 dB		−28,5	−26,5	−24,5	dB
Switching thresholds			note 4; pin 24					
for record				V_{24-27}	8,5	–	14	V
for playback				V_{24-27}	0	–	4	V
Switching thresholds			note 5; pin 25					
	OFF			V_{25-27}	0	–	3,5	V
(switch in open position)	B			V_{25-27}	–	7	–	V
(external voltage)	B			V_{25-27}	6,3	7	7,7	V
	C			V_{25-27}	10,8	–	14	V
Switch input current			pin 25					
	OFF		$V_{25-27} = 0$ V	$-I_{25}$	–	–	40	μA
	C		$V_{25-27} = V_{CC}$	I_{25}	–	–	40	μA
Frequency response shift as a function of temperature deviation, range −40 to + 85 °C, measured as deviation from 25 °C	C			Δf	–	± 0,5	–	dB
as a function of voltage deviation, range 8 to 16 V, measured as deviation from 14 V				Δf	–	± 0,1		dB
Input resistance								
			pin 26	R_{26-27}	35	50	65	kΩ
			pin 28	R_{28-27}	35	50	65	kΩ
Output resistance								
			pin 6	R_{6-27}	–	160	220	Ω
			pin 21	R_{21-27}	–	60	100	Ω

Notes to the characteristics

1. Operation with minimum of 12 dB headroom; system remains functional to 7 V.
2. Attenuation between pins 1 and 3 is 3,5 dB (MPX-filter).
   Playback input sensitivity is 45 mV if a switchable MPX-low pass filter is used in playback mode (pins 2 and 3 short-circuited).
3. System headroom is determined by the line output channel in use.
   For low supply voltages line output 2 (pin 6) will saturate at high signal levels. Headroom for line output 1 (pin 5) tracks with record output (pin 21).
4. The equation for REC/PB switch input voltage is:

   REC: $V_{24\text{-}27} > 0{,}55\ V_{CC} - V_{BE} + 1{,}5\ V$,

   PB: $V_{24\text{-}27} < 0{,}45\ V_{CC} - V_{BE} - 1{,}5\ V$.
5. The equation for C/B/OFF mode switch input voltage is:

   OFF: $V_{25\text{-}27} < 0{,}38\ V_{CC} - V_{BE} - 1\ V$,

   B: $0{,}45\ V_{CC} < V_{25\text{-}27} < 0{,}55\ V_{CC}$ (external voltage),

   B: $0{,}5\ V_{CC}$ (switch in open position),

   C: $V_{25\text{-}27} > 0{,}75\ V_{CC} - V_{BE} + 1\ V$.

   The voltage drop across the external time constant resistor must be taken in to account.

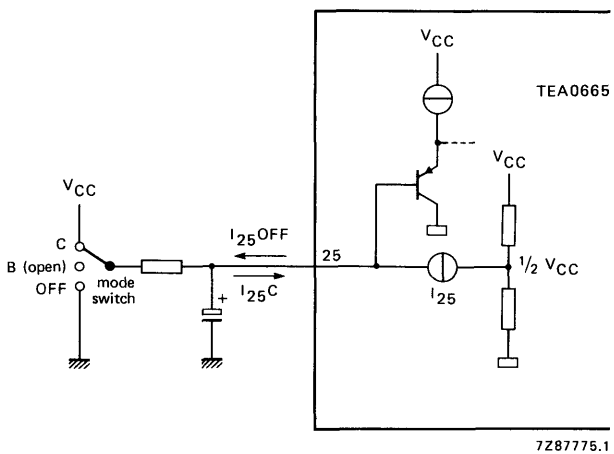


Fig. 3 Mode switch input configuration.

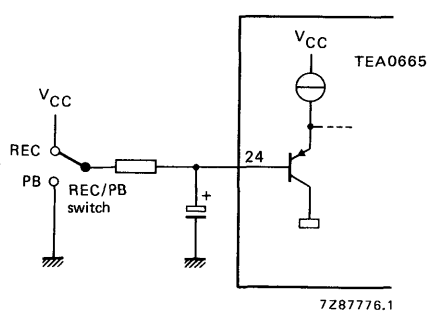


Fig. 4 REC/PB switch input configuration.

DEVELOPMENT DATA

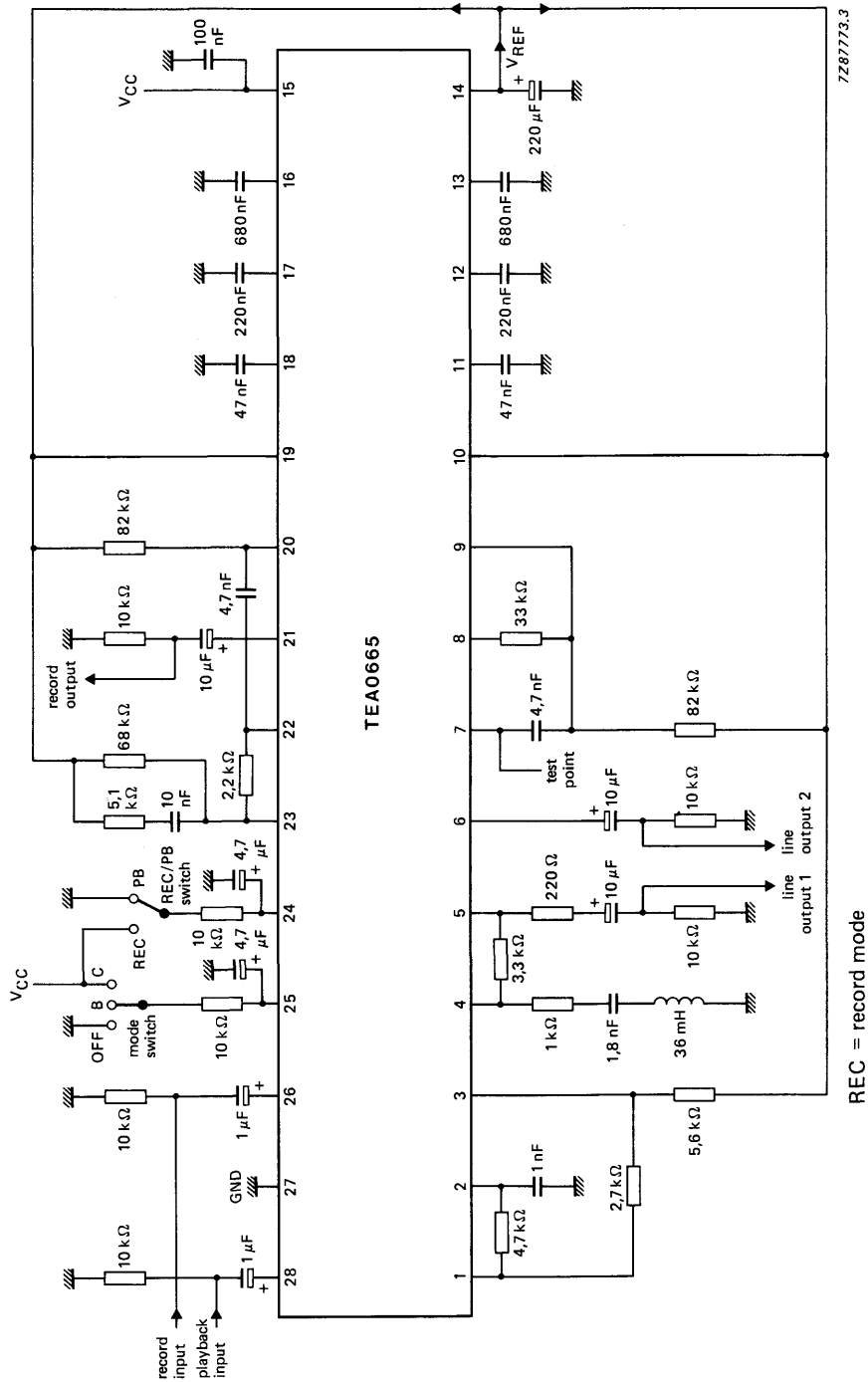


Fig. 5 Test circuit.

SYSTEM GRAPHS

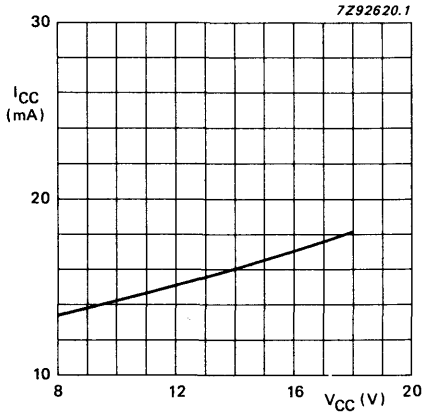


Fig. 6 Supply current as a function of supply voltage; $I_{CC} = f(V_{CC})$; no input signal.

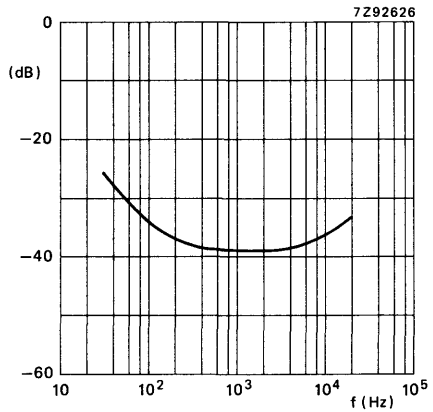


Fig. 7 Power supply ripple rejection measured at REC OUT as a function of frequency; level at pin 15 = 100 mV (rms). R_G = 10 kΩ; record mode; NR OFF.

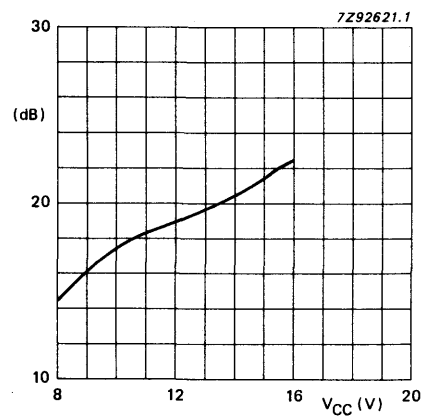


Fig. 8 Signal handling = $f(V_{CC})$ measured at REC OUT as a function of the supply voltage; THD = 1%.

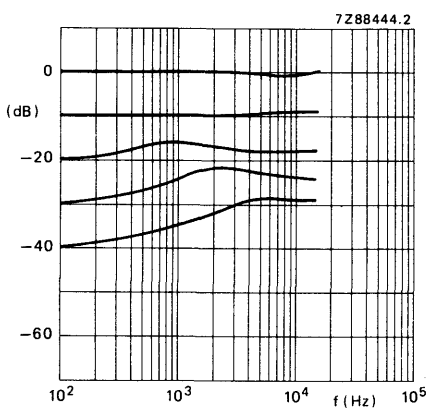


Fig. 9 Encoder frequency response for B-mode.

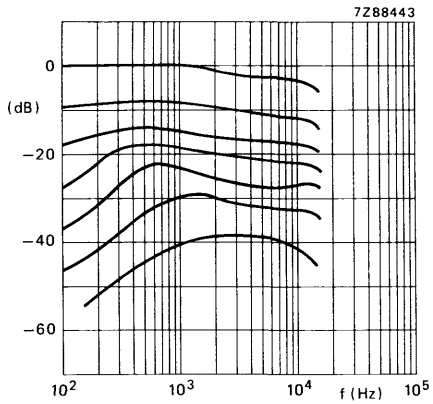


Fig. 10 Encoder frequency response for C-mode.

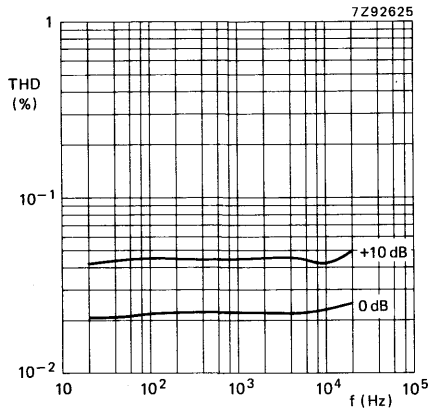


Fig. 11 Total harmonic distortion measured at REC OUT as a function of frequency; for NR OFF mode; V_{CC} = 14 V; LPF 80 kHz.

DEVELOPMENT DATA

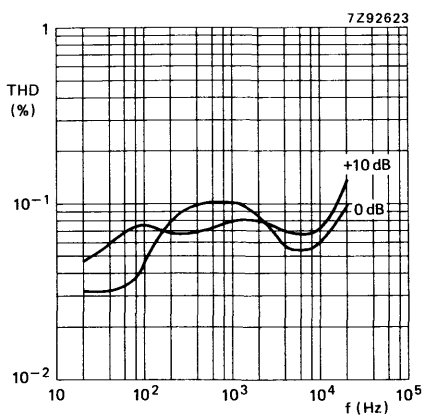


Fig. 12 Total harmonic distortion measured at REC OUT as a function of frequency; for B-mode; V_{CC} = 14 V; LPF 80 kHz.

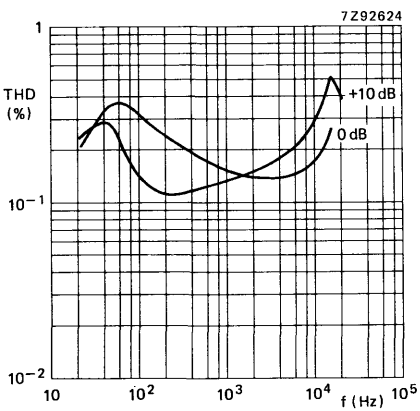


Fig. 13 Total harmonic distortion measured at REC OUT as a function of frequency; for C-mode; V_{CC} = 14 V; LPF 80 kHz.

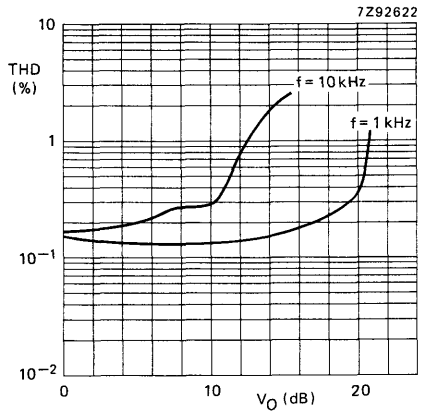


Fig. 14 Total harmonic distortion as a function of the record output level (pin 21); for C-mode; V_{CC} = 14 V; LPF 80 kHz.

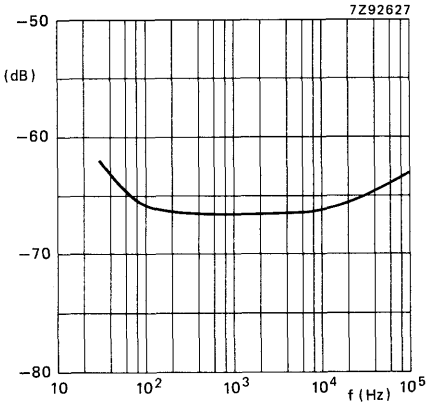


Fig. 15 Crosstalk from record input (pin 26) to line output as a function of frequency in playback mode; record input level is 50 mV; NR OFF; R_G = 10 kΩ.

DOLBY* B and C TYPE NOISE REDUCTION CIRCUIT

GENERAL DESCRIPTION

The TEA0666 is designed for use in Dolby B and Dolby C type audio Noise Reduction (NR) systems. The device provides the high and low level stages for one channel of a Dolby C-type NR system, including NR ON/OFF switching and all electronic switching necessary for Dolby C-type systems. In addition the TEA0666 includes a preamplifier for the record and playback functions and a multiplex buffer amplifier. The circuit offers two different line-output levels (−6 and 0 dBm) and a low-pass filter, which can be fed into the signal path in playback mode.

TEA0666 is a selected version of TEA0665 with respect to frequency response, making it especially suitable for high end applications such as 3-head cassette decks and other group A products.

Features

- Few external components required
- Included RECORD/PLAY preamplifiers plus multiplex filter buffer amplifier
- Two different line-output levels
- All electronic switching

PACKAGE OUTLINES

TEA0666: 28-lead DIL; plastic (SOT117).
TEA0666T: 28-lead mini-pack; plastic (SO28; SOT136A).

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, U.S.A., from whom licensing and application information must be obtained.
Dolby is a registered trademark of Dolby Laboratories Licensing Corporation.

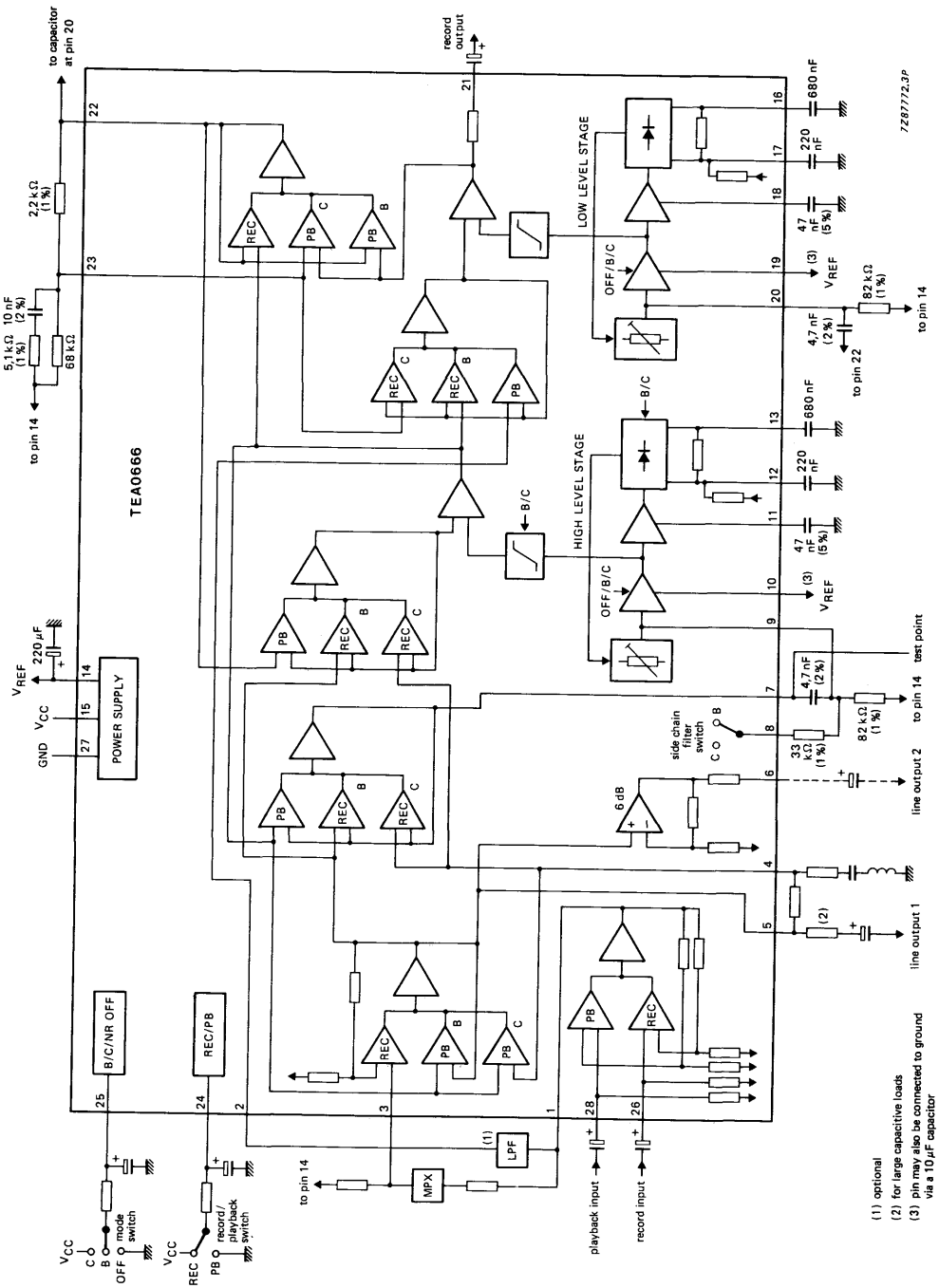


Fig. 1 Block diagram and application circuit.

DEVELOPMENT DATA

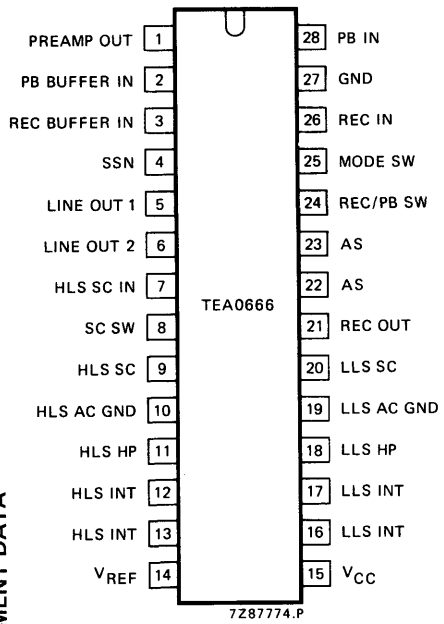


Fig. 2 Pinning diagram.

PINNING

1	PREAMP OUT	record/playback preamplifier output
2	PB BUFFER IN	playback amplifier input buffer
3	REC BUFFER IN	record amplifier input buffer
4	SSN	spectral skewing network
5	LINE OUT 1	line output 1
6	LINE OUT 2	line output 2
7	HLS SC IN	high level stage side chain input
8	SC SW	side chain filter switch
9	HLS SC	high level stage side chain
10	HLS AC GND	high level stage AC ground
11	HLS HP	high level stage high pass filter
12	HLS INT	high level stage integrating filter
13	HLS INT	high level stage integrating filter
14	V_{REF}	reference voltage
15	V_{CC}	positive supply voltage
16	LLS INT	low level stage integrating filter
17	LLS INT	low level stage integrating filter
18	LLS HP	low level stage high pass filter
19	LLS AC GND	low level stage AC ground
20	LLS SC	low level stage side chain
21	REC OUT	record output
22	AS	anti-saturation filter
23	AS	anti-saturation filter
24	REC/PB SW	record/playback switch input
25	MODE SW	mode switch input
26	REC IN	record input
27	GND	ground
28	PB IN	playback input

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	V_{CC}	max.	18 V
Input voltage (pins 26 and 28)	V_I	max.	−0,3 to V_{CC} V
Total power dissipation	P_{tot}		600 mW
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−40 to + 85 °C

CHARACTERISTICS

V_{CC} = 14 V; f = 20 Hz to 15 kHz; T_{amb} = 25 °C; all levels with reference to 387,5 mV = 0 dB = −6 dBm at test point pin 7; test circuit Fig. 5; record mode; unless otherwise specified.

parameter	conditions			symbol	min.	typ.	max.	unit
	mode	f (kHz)						
Supply								
Supply voltage range	C	–	note 1					
single				V_{CC}	8	14	16	V
(split)				V_{CC}	(± 4)	(± 7)	(± 8)	V
Supply current	OFF	–	no input signal	I_{CC}	–	17	25	mA
Input sensitivity	C		note 2					
of record amplifier			pin 26	V_i	43	50	57	mV
of playback amplifier			pin 28	V_i	25	30	35	mV
Signal handling	C	1	V_{CC} = 8 V					
of record output			THD = 1%		12	15	–	dB
(note 3; see Fig. 8)		1	V_{CC} = 14 V					
			THD = 1%		–	20	–	dB
Line output 1			note 3		−0,5	0	+ 0,5	dB
Line output 2; amplifier gain V_o/V_i (pin 6 to pin 5)				G_v	+ 5,5	+ 6	+ 6,5	dB
Total harmonic distortion	OFF	1	TPL = 0 dB*	THD	–	0,02	0,1	%
			TPL = + 10 dB	THD	–	0,05	0,3	%
Total harmonic distortion	B	1	TPL = 0 dB	THD	–	0,1	0,15	%
			TPL = + 10 dB	THD	–	0,08	0,3	%
		10	TPL = 0 dB	THD	–	0,06	0,1	%
Total harmonic distortion	C	1	TPL = 0 dB	THD	–	0,15	0,3	%
			TPL = + 10 dB	THD	–	0,13	0,5	%
Signal plus noise-to-noise ratio	C		R_S = 10 kΩ CCIR/ARM weighted	(S+N)/N	62	66	–	dB

* TPL is Test Point Level.

DEVELOPMENT DATA

parameter	conditions			symbol	min.	typ.	max.	unit
	mode	f (kHz)						
Frequency response	B	2	TPL = −25 dB		−18,7	−18,0	−17,3	dB
		5	TPL = −40 dB		−30,4	−29,7	−29,0	dB
		10	TPL = −30 dB		−24,2	−23,5	−22,8	dB
	C	0,2	TPL = −40 dB		−32,9	−31,9	−30,9	dB
		1	TPL = −30 dB		−19,3	−18,6	−17,9	dB
		1	TPL = −20 dB		−14,8	−14,1	−13,4	dB
		5	TPL = −0 dB		−2,8	−2,3	−1,8	dB
		5	TPL = −20 dB		−17,8	−17,1	−16,4	dB
		5	TPL = −40 dB		−27,0	−26,5	−26,0	dB
Switching thresholds			note 4; pin 24					
for record				V_{24-27}	8,5	–	14	V
for playback				V_{24-27}	0	–	4	V
Switching thresholds			note 5; pin 25					
	OFF			V_{25-27}	0	–	3,5	V
(switch in open position)	B			V_{25-27}	–	7	–	V
(external voltage)	B			V_{25-27}	6,3	7	7,7	V
	C			V_{25-27}	10,8	–	14	V
Switch input current			pin 25					
	OFF		V_{25-27} = 0 V	$-I_{25}$	–	–	40	μA
	C		$V_{25-27} = V_{CC}$	I_{25}	–	–	40	μA
Frequency response shift as a function of temperature deviation, range −40 to + 85 °C, measured as deviation from 25 °C	C			Δf	–	± 0,5	–	dB
as a function of voltage deviation, range 8 to 16 V, measured as deviation from 14 V				Δf	–	± 0,1		dB
Input resistance								
			pin 26	R_{26-27}	35	50	65	kΩ
			pin 28	R_{28-27}	35	50	65	kΩ
Output resistance								
			pin 6	R_{6-27}	–	160	220	Ω
			pin 21	R_{21-27}	–	60	100	Ω

Notes to the characteristics

1. Operation with minimum of 12 dB headroom; system remains functional to 7 V.
2. Attenuation between pins 1 and 3 is 3,5 dB (MPX-filter).
   Playback input sensitivity is 45 mV if a switchable MPX-low pass filter is used in playback mode (pins 2 and 3 short-circuited).
3. System headroom is determined by the line output channel in use.
   For low supply voltages line output 2 (pin 6) will saturate at high signal levels. Headroom for line output 1 (pin 5) tracks with record output (pin 21).
4. The equation for REC/PB switch input voltage is:

   REC: $V_{24\text{-}27} > 0{,}55\ V_{CC} - V_{BE} + 1{,}5\ V$,

   PB: $V_{24\text{-}27} < 0{,}45\ V_{CC} - V_{BE} - 1{,}5\ V$.
5. The equation for C/B/OFF mode switch input voltage is:

   OFF: $V_{25\text{-}27} < 0{,}38\ V_{CC} - V_{BE} - 1\ V$,

   B: $0{,}45\ V_{CC} < V_{25\text{-}27} < 0{,}55\ V_{CC}$ (external voltage),

   B: $0{,}5\ V_{CC}$ (switch in open position),

   C: $V_{25\text{-}27} > 0{,}75\ V_{CC} - V_{BE} + 1\ V$.

The voltage drop across the external time constant resistor must be taken in to account.

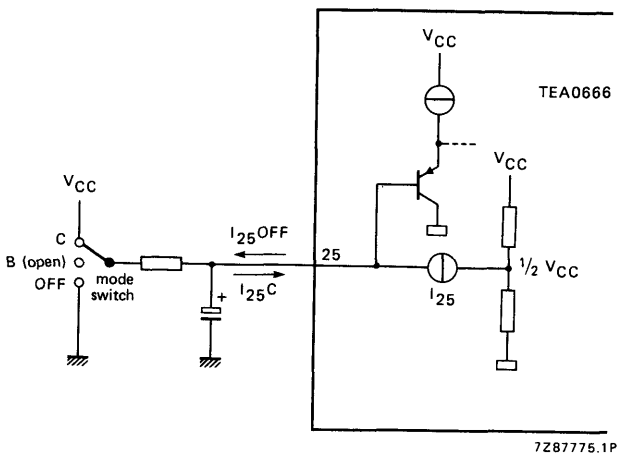


Fig. 3 Mode switch input configuration.

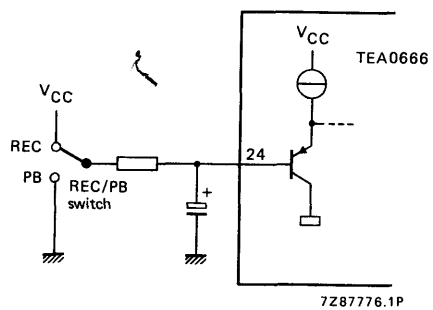
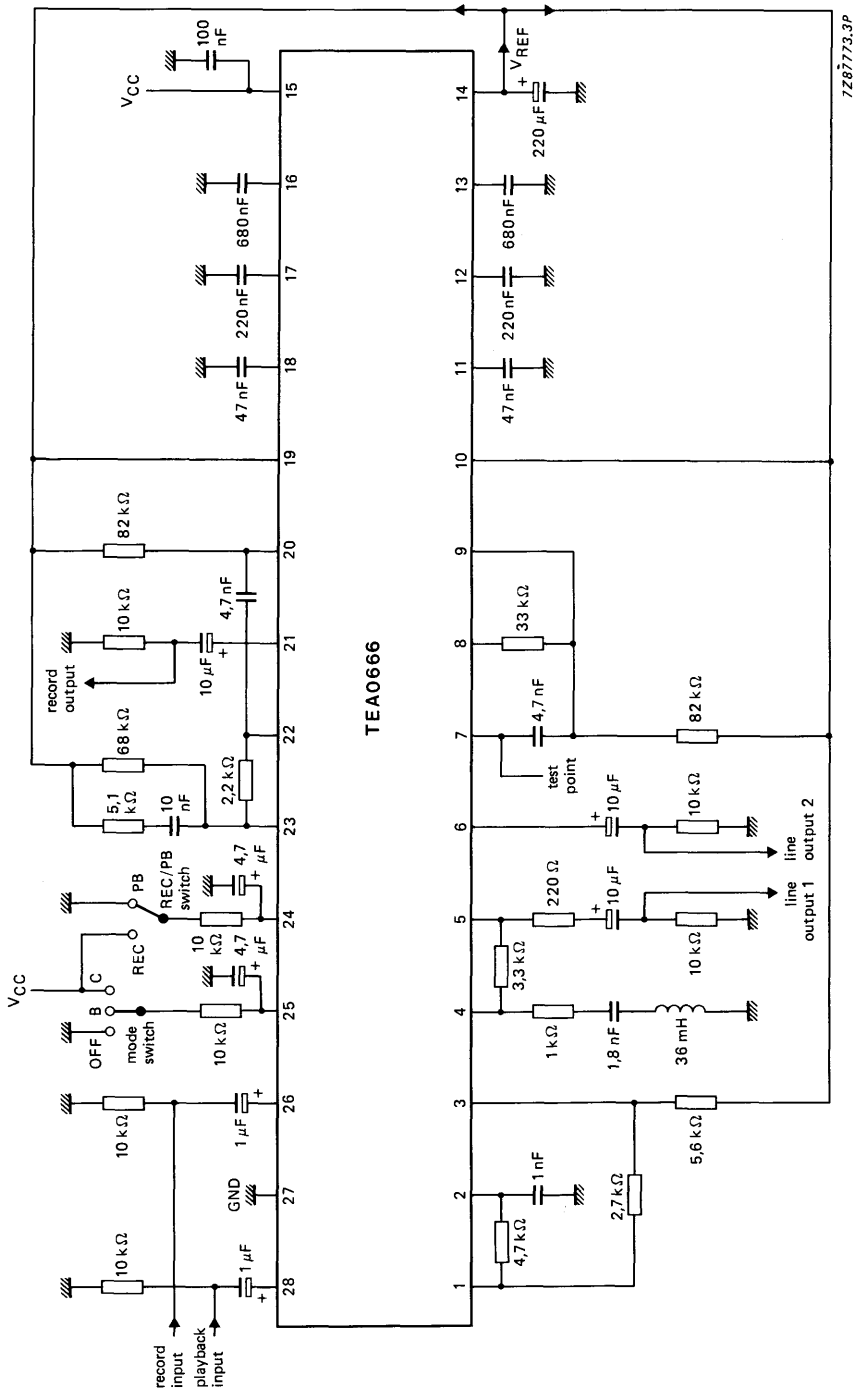


Fig. 4 REC/PB switch input configuration.

DEVELOPMENT DATA



REC = record mode
PB = playback mode

Tolerances: resistors 1%
capacitors 1%

Fig. 5 Test circuit.

SYSTEM GRAPHS

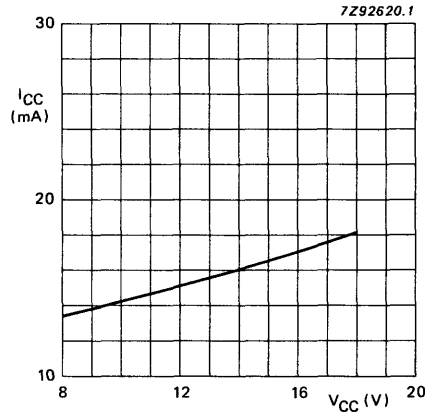


Fig. 6 Supply current as a function of supply voltage; $I_{CC} = f(V_{CC})$; no input signal.

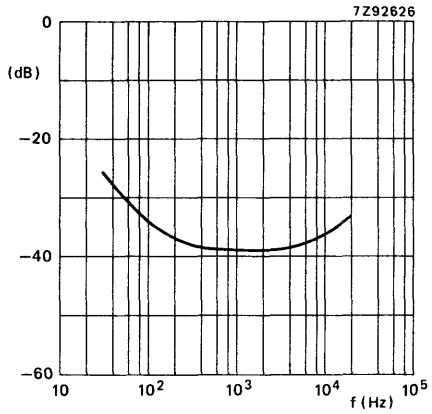


Fig. 7 Power supply ripple rejection measured at REC OUT as a function of frequency; level at pin 15 = 100 mV (rms). R_G = 10 kΩ; record mode; NR OFF.

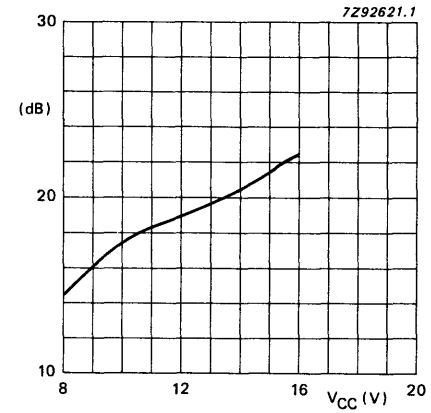


Fig. 8 Signal handling = $f(V_{CC})$ measured at REC OUT as a function of the supply voltage; THD = 1%.

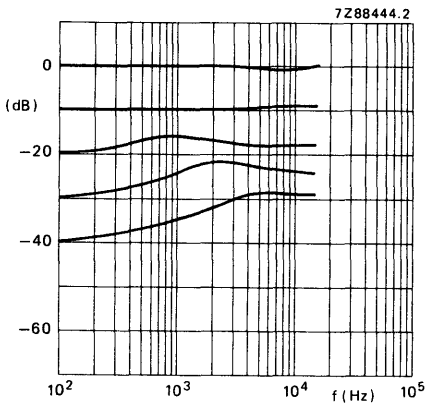


Fig. 9 Encoder frequency response for B-mode.

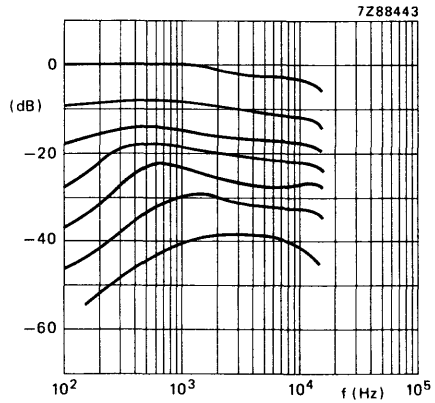


Fig. 10 Encoder frequency response for C-mode.

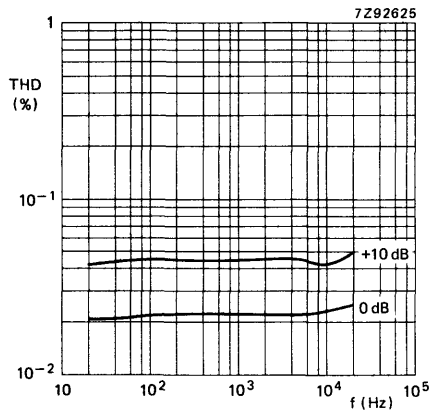


Fig. 11 Total harmonic distortion measured at REC OUT as a function of frequency; for NR OFF mode; V_{CC} = 14 V; LPF 80 kHz.

DEVELOPMENT DATA

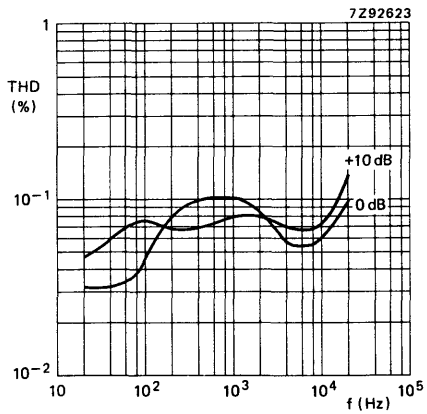


Fig. 12 Total harmonic distortion measured at REC OUT as a function of frequency; for B-mode; V_{CC} = 14 V; LPF 80 kHz.

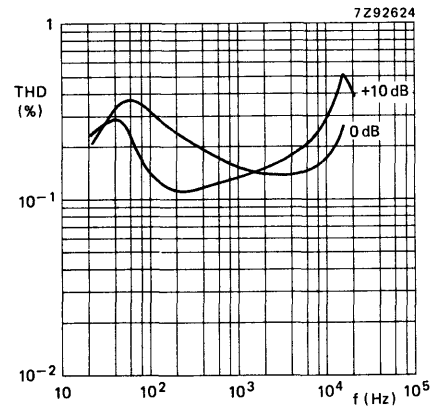


Fig. 13 Total harmonic distortion measured at REC OUT as a function of frequency; for C-mode; V_{CC} = 14 V; LPF 80 kHz.

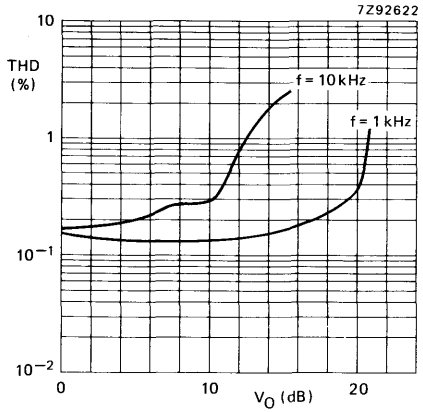


Fig. 14 Total harmonic distortion as a function of the record output level (pin 21); for C-mode; V_{CC} = 14 V; LPF 80 kHz.

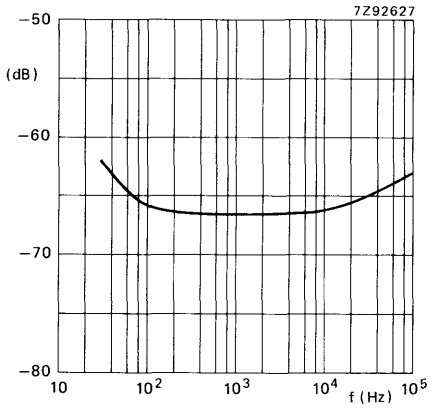


Fig. 15 Crosstalk from record input (pin 26) to line output as a function of frequency in playback mode; record input level is 50 mV; NR OFF; R_G = 10 kΩ.

LOW VOLTAGE DOLBY B/C TYPE

DESCRIPTION

The TEA0670T is a monolithic IC intended for use in low voltage Dolby* B and C type noise reduction applications. This IC design features both record and playback modes with all internal electronic switching.

FEATURES

- B and C type noise reduction
- Low voltage operation 1.8 to 8 V
- Playback and record modes
- 0 dB (Dolby level) = 100 mV
- Record input sensitivity 50 mV
- Playback sensitivity 20 mV
- All electronic switching

APPLICATION

- Portable tape recorders/players.

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

* Dolby is a registered trademark of Dolby Laboratories Licensing Corporation, San Francisco, California (U.S.A.).

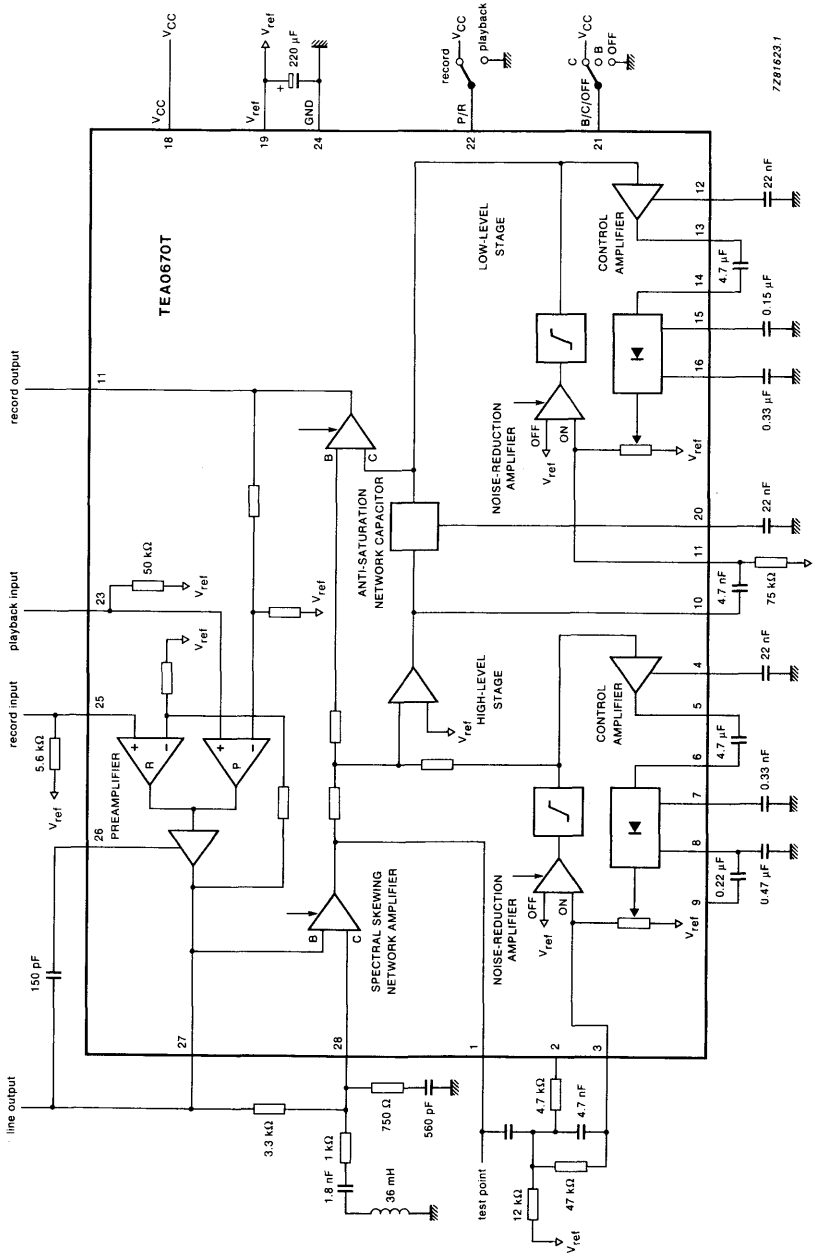


Fig. 1 Block diagram and test circuit.

Pin functions

1. Test point
2. Internal switch
3. High level stage side chain input
4. High level stage high pass
5. High level stage D-amplifier output
6. High level stage rectifier input
7. High level stage attack
8. High level stage decay
9. Internal switch
10. High level stage output
11. Low level side chain input
12. Low level stage high pass
13. Low level stage D-amplifier output
14. Low level stage rectifier input
15. Low level stage attack
16. Low level stage decay
17. Record output
18. V_{CC}
19. V_{ref}
20. Anti-saturation network capacitor
21. Mode switch
22. Playback/record switch
23. Playback input
24. Ground
25. Record input
26. Compensation capacitor
27. Line output
28. Spectral skewing network

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	–	8	V
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C
Electrostatic handling; classification A*				

* Classification A:
Human body model; C = 100 pF; R = 1.5 kΩ; V ⩾ 4 kV
Charge device model; C = 200 pF; R = 0 Ω; V ⩾ 500 V
Pins 3 and 11 are NOT similarly protected.

DEVELOPMENT DATA

CHARACTERISTICS

V_{CC} = 3 V; T_{amb} = 25 °C; all levels are referenced to 0 dB = 100 mV at the test-point; unles otherwise specified.

parameter	B/C	NR	R/P*	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		OFF	R		V_{CC}	1.8	3.0	–	V
Minimum operational voltage		OFF	R	THD = 1%	V_{CC}	–	1.5	–	V
Supply current									
	C	OFF	R	0 dB; f = 1 kHz	I_{CC}	–	7	–	mA
	C	ON	R	0 dB; f = 1 kHz	I_{CC}	–	9	–	mA
Input resistance				at pin 23	R_I	35	50	65	kΩ
Signal plus noise-to-noise ratio									
		OFF	R	CCIR (Dolby)	(S+N)/N	–	78	–	dB
	B	ON	R	R_S = 10 kΩ	(S+N)/N	–	74	–	dB
	C	ON	R		(S+N)/N	–	66	–	dB
Distortion 2nd and 3rd harmonics									
	B	OFF	R	0 dB; f = 1 kHz	THD	–	0.02	–	%
	B	ON	R	0 dB; f = 1 kHz	THD	–	0.05	0.1	%
	C	ON	R	0 dB; f = 1 kHz	THD	–	0.1	–	%

* R = record mode; P = playback mode.

CHARACTERISTICS (continued)

parameter	B/C	NR	R/P*	conditions	symbol	min.	typ.	max.	unit
Signal handling									
	C	ON	R	THD = 1%					
				V_{CC} = 1.8 V		12	–	–	dB
	C	ON	R	V_{CC} = 3 V		–	14	–	dB
Frequency response referenced to test point									
	B	ON	R	f = 10 kHz; 0 dB		–1.6	0.4	2.4	dB
	B	ON	R	f = 1 kHz; –20 dB		–17.8	–15.8	–13.8	dB
	B	ON	R	f = 5 kHz; –30 dB		–23.8	–21.8	–19.8	dB
	B	ON	R	f = 5 kHz; –40 dB		–31.7	–29.7	–27.7	dB
	C	ON	R	f = 10 kHz; –0 dB		–5.5	–3.5	–1.5	dB
	C	ON	R	f = 1 kHz; –20 dB		–16.1	–14.1	–12.1	dB
	C	ON	R	f = 5 kHz; –40 dB		–28.5	–26.5	–24.5	dB
	C	ON	R	f = 200 Hz; –40 dB		–33.9	–31.9	–29.9	dB
Switching thresholds									
	B	OFF				0	GND	$0.1V_{CC}$	V
	B					–	**	–	V
	C					$0.95V_{CC}$	V_{CC}	V_{CC}	V
			P			0	GND	0.2	V
			R			$0.7V_{CC}$	V_{CC}	V_{CC}	V
Preamplifier gain									
	B	OFF	R			–	6	–	dB
	B	OFF	P			–	14	–	dB

DEVELOPMENT DATA

* R = record mode; P = playback mode.
** Open-circuit.

1-CHIP AM RADIO

GENERAL DESCRIPTION

The TEA5551T is a 1-chip monolithic integrated radio circuit which is designed for use as a pocket receiver with headphones in a supply voltage range (V_S) of 1.8 V to 4.5 V.
The circuit consists of a complete AM part and dual AF amplifier with low quiescent current. The AF part has low radiation (HF noise) and good overdrive performance. The dual AF amplifier makes the device suitable for operation in an AM/FM stereo receiver with or without stereo cassette player.
The IC has a 1-pin switch for AM or other applications.

Features

- Low voltage operation (V_S = 1.8 V to 4.5 V)
- Low current consumption (I_{tot} = 5 mA at V_S = 3 V)
- All pins provided with ESD protection

AM part

- High sensitivity (V_i = 1.5 μV for V_o = 10 mV)
- Good IF suppression
- Good signal handling ($V_{i(max)}$ = 80 mV)
- Switch for AM or other applications

AF part

- A fixed integrated gain of 32 dB
- Few external components required
- Very low quiescent current
- Low HF radiation and good AF overdrive performance
- 0 to 20 kHz limited frequency response
- 25 mW per channel output power in 32 Ω

QUICK REFERENCE DATA (at T_{amb} = 25 °C)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_S	1.8	3.0	4.5	V
Supply current		$I_5 + I_{10}$	–	5	–	mA
AM part	m = 0.3					
RF sensitivity						
RF input voltage						
	$V_{o(AF)}$ = 10 mV	$V_{i(RF)}$	–	1.5	–	μV
	S/N = 26 dB	$V_{i(RF)}$	–	15	–	μV
	S/N = 50 dB	$V_{i(RF)}$	–	10	–	mV
AF output voltage	$V_{i(RF)}$ = 1 mV	$V_{o(AF)}$	–	80	–	mV
Total harmonic distortion	$V_{i(RF)}$ = 100 μV to 30 mV	THD	–	0.8	–	%
Signal handling capability	m = 0.8; THD = 10%	$V_{i(RF)}$	–	80	–	mV
AF part	both channels driven					
Output power	R_L = 32 Ω; THD = 10%					
at V_S = 3.0 V		P_o	–	25	–	mW
at V_S = 4.5 V		P_o	–	60	–	mW
Voltage gain	P_o = 10 mW	G_v	–	32	–	dB
Channel separation	1 kHz	α	–	50	–	dB

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).

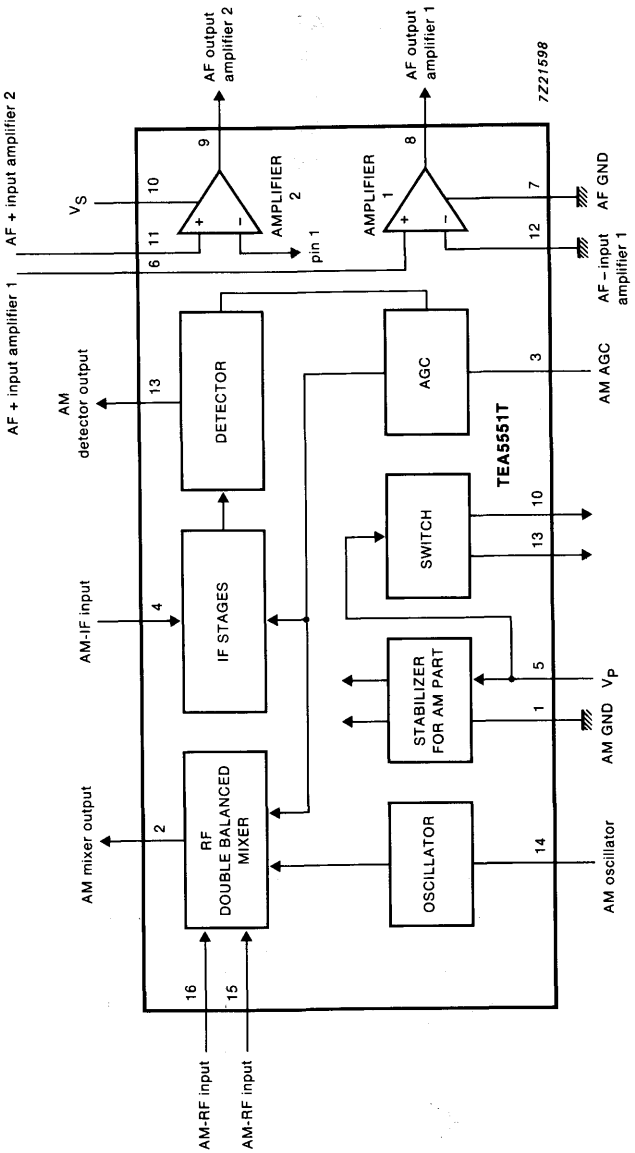


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

1	AM GND	9	AF output amplifier 2
2	AM mixer output	10	AF supply voltage (V_S)
3	AM AGC	11	AF + input amplifier 2
4	AM–IF input	12	AF – input amplifier 1
5	AM supply voltage (V_P)	13	AM detector output
6	AF + input amplifier 1	14	AM oscillator
7	AF GND	15	AM–RF input
8	AF output amplifier 1	16	AM–RF input

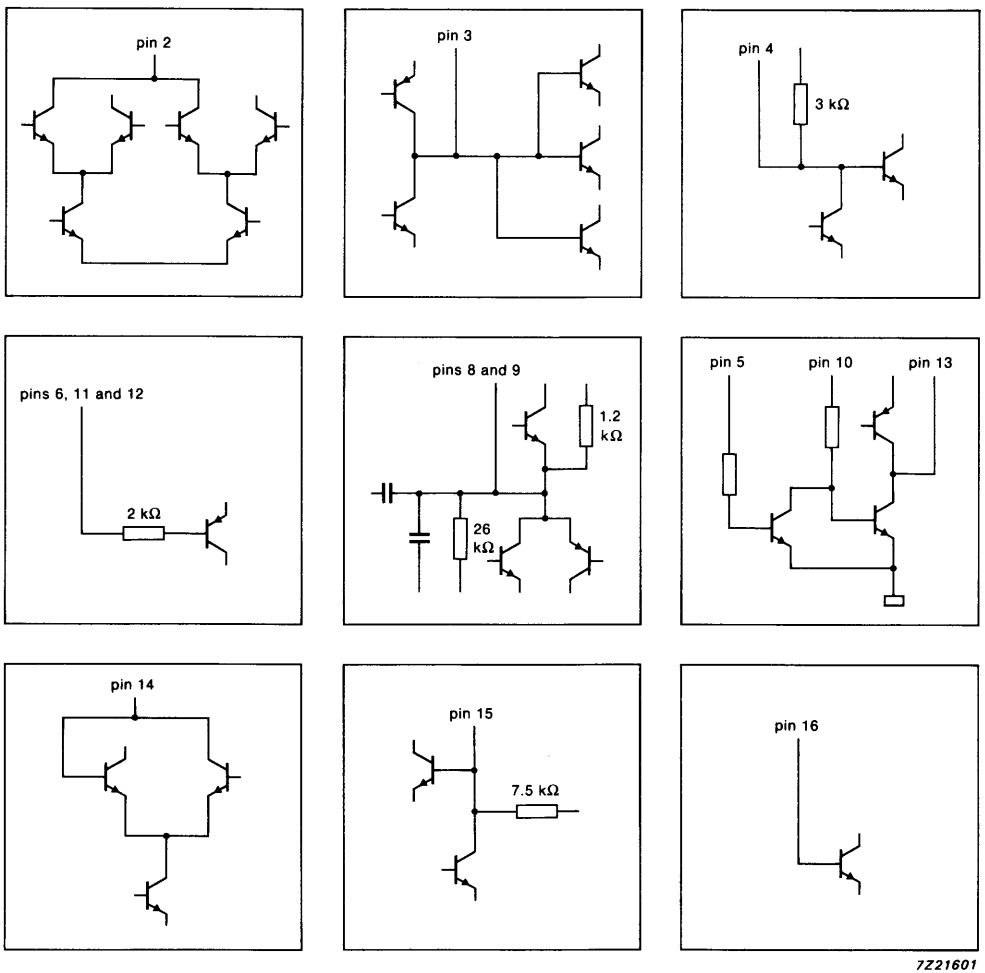


Fig. 2 All pins provided with ESD protection diodes to substrate.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_S	–	6	V
Supply current (peak)		I_M	–	150	mA
Crystal temperature		T_c	–	150	°C
Short-circuit protection	V_S = 4.5 V	t_{sc}	–	5	s
Total power dissipation		P_{tot}	see Fig. 3		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−25	+60	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 110 K/W

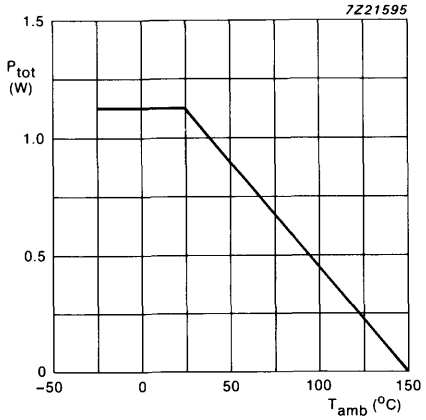


Fig. 3 Power derating curve.

DC CHARACTERISTICS

All voltages are referenced to pin 1 and pin 7; all input currents are positive; all parameters are measured in test circuit of Fig. 6 at V_S = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_S	1.8	3.0	4.5	V
Voltages					
pin 5	V_5	1.6	2.8	4.3	V
pin 10	V_{10}	1.8	3.0	4.5	V
HF part					
Total current consumption (pin 5)	I_5	–	2.2	–	mA
Oscillator current (pin 14)	I_{14}	–	100	–	μA
Mixer current (pin 2)	I_2	–	200	–	μA
Voltages					
pin 3	V_3	–	150	–	mV
pin 13	V_{13}	–	600	–	mV
pin 15	V_{15}	–	1.1	–	V
pin 16	V_{16}	–	1.1	–	V
AF part					
Total current consumption (pin 10)	I_5	–	3.0	–	mA
Input bias current (pin 11 connected to pin 16)	$I_{11} + I_{16}$	–	40	–	nA
DC output voltage					
pin 8	V_8	–	1.5	–	V
pin 9	V_9	–	1.5	–	V

DEVELOPMENT DATA

AC CHARACTERISTICS

All parameters are measured in test circuit of Fig. 6 at V_S = 3 V; T_{amb} = 25 °C unless otherwise specified.
RF conditions: Input frequency 1 MHz; 30% modulation where f_{mod} = 1 kHz; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
RF sensitivity						
RF input voltage	$V_{o(AF)}$ = 10 mV	$V_{i(RF)}$	–	1.5	–	μV
Loss in sensitivity	$V_{o(AF)}$ = 10 mV; V_S = 1.8 V	$\Delta V_{i(RF)}$	–	6	–	dB
Noise						
Signal-to-noise ratio for RF input signal voltage of						
$V_{i(RF)}$ = 2 μV		S/N	–	6	–	dB
$V_{i(RF)}$ = 15 μV		S/N	–	26	–	dB
$V_{i(RF)}$ = 1 mV		S/N	–	46	–	dB
AF output voltage						
	$V_{i(RF)}$ = 1 mV	$V_{o(AF)}$	–	80	–	mV
	$V_{i(RF)}$ = 1 mV; V_S = 1.8 V	$V_{o(AF)}$	–	55	–	mV
Total harmonic distortion						
	$V_{i(RF)}$ = 100 μV to 30 mV	THD	–	0.8	–	%
	$V_{i(RF)}$ = 80 mV; m = 0.8	THD	–	10	–	%
AGC range						
Change in RF input voltage for 10 dB change in AF output voltage	$V_{i(RF1)}$ = 50 mV	$V_{i(RF1)}$/ $V_{i(RF2)}$	–	86	–	dB
Optimum source impedance		Z_{source}	–	3	–	kΩ
IF suppression						
at $V_{o(AF)}$ = 10 mV	note 1	α	–	20	–	dB
Oscillator (pin 14)	f_{osc} = 1468 kHz					
Oscillator voltage		V_i	–	100	–	mV
	V_5 = 1.5 V	V_i	–	*	–	mV

Note to the AC characteristics

1. $\alpha = \dfrac{V_i \text{ at } f_i = 468 \text{ kHz}}{V_i \text{ at } f_i = 1 \text{ MHz}}$

* Value to be fixed.

AC CHARACTERISTICS

All parameters are measured in test circuit of Fig. 6 at V_S = 3 V; T_{amb} = 25 °C unless otherwise specified

AF conditions: f = 1 kHz; R_L = 32 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power						
	THD = 10%	P_o	–	25	–	mW
	THD = 10%; V_S = 1.8 V	P_o	–	8	–	mW
	THD = 10%; V_S = 4.5 V	P_o	–	60	–	mW
Total harmonic distortion	P_o = 10 mW	THD	–	0.5	–	%
Voltage gain	P_o = 10 mW	G_v	–	32	–	dB
Noise						
Noise output voltage	R_S = 5 kΩ; B = 15 kHz	V_{no}	–	240	–	μV
HF noise output voltage	R_S = 5 kΩ; B = 5 kHz; f = 500 kHz	$V_{no(RF)}$	–	20	–	μV
Input circuit						
Input impedance	pin 11 connected to pin 12	Z_i	–	3	–	MΩ
Mute switch						
AC impedance (pin 13 to ground)	V_5 = 0 V; I_{13} = 0.32 mA	R_S	–	200	–	Ω

DEVELOPMENT DATA

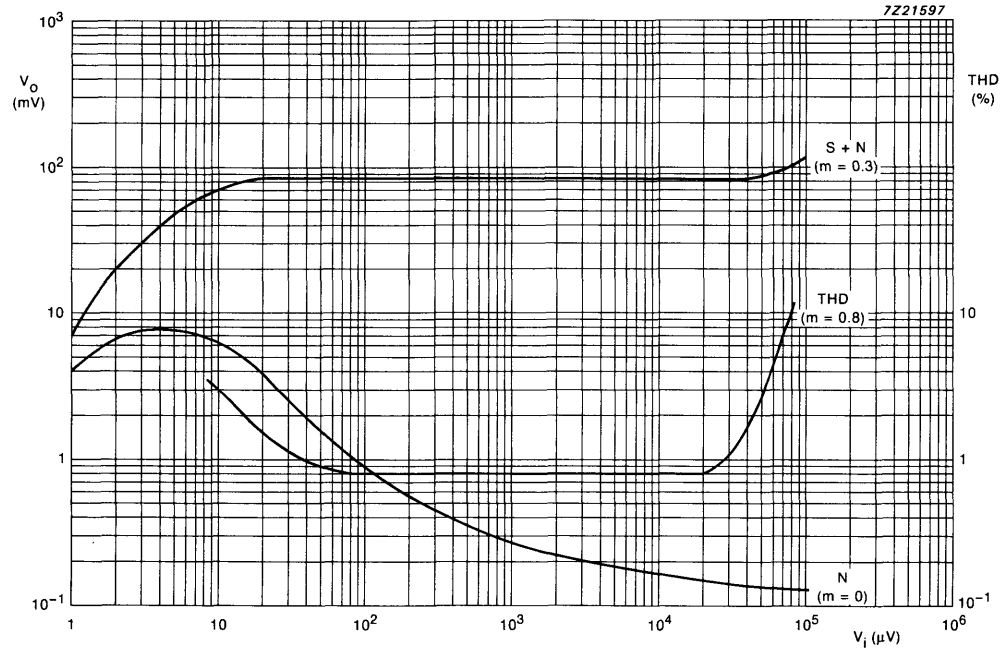


Fig. 4 Typical signal (S) and noise (N) output voltages, where V_o is the AF output voltage at pin 13, as a function of the input voltage V_i. V_i is the input voltage at pin 16. Also shown is the total harmonic distortion (THD).
Conditions: f_o = 1 MHz; f_m = 1 kHz; V_S = 3 V; R_g = 50 Ω; m = 0.3 (unless otherwise specified).

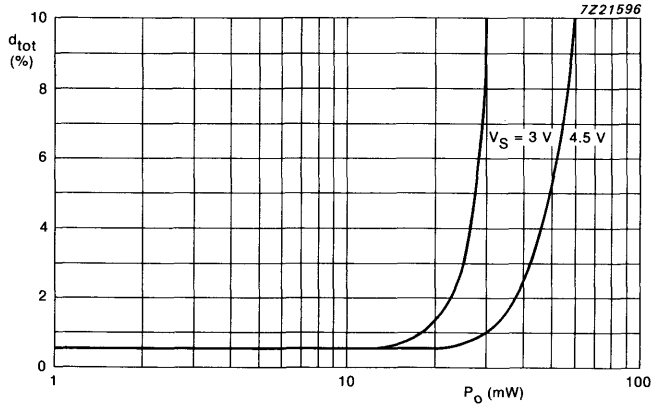
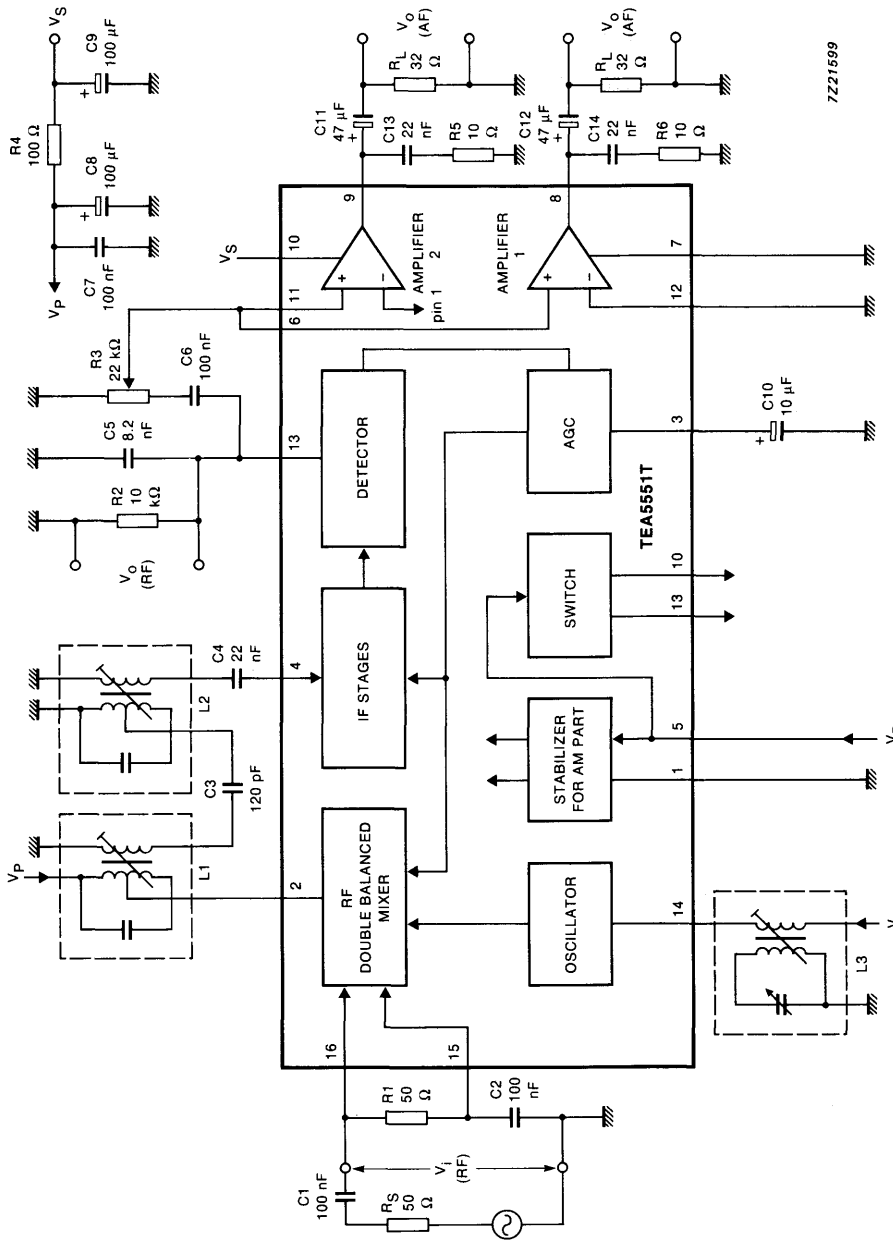


Fig. 5 Total distortion (d_{tot}) as a function of output power (P_o).
Conditions: V_S = 3 V and 4.5 V; R_L = 32 Ω; f = 1 kHz.

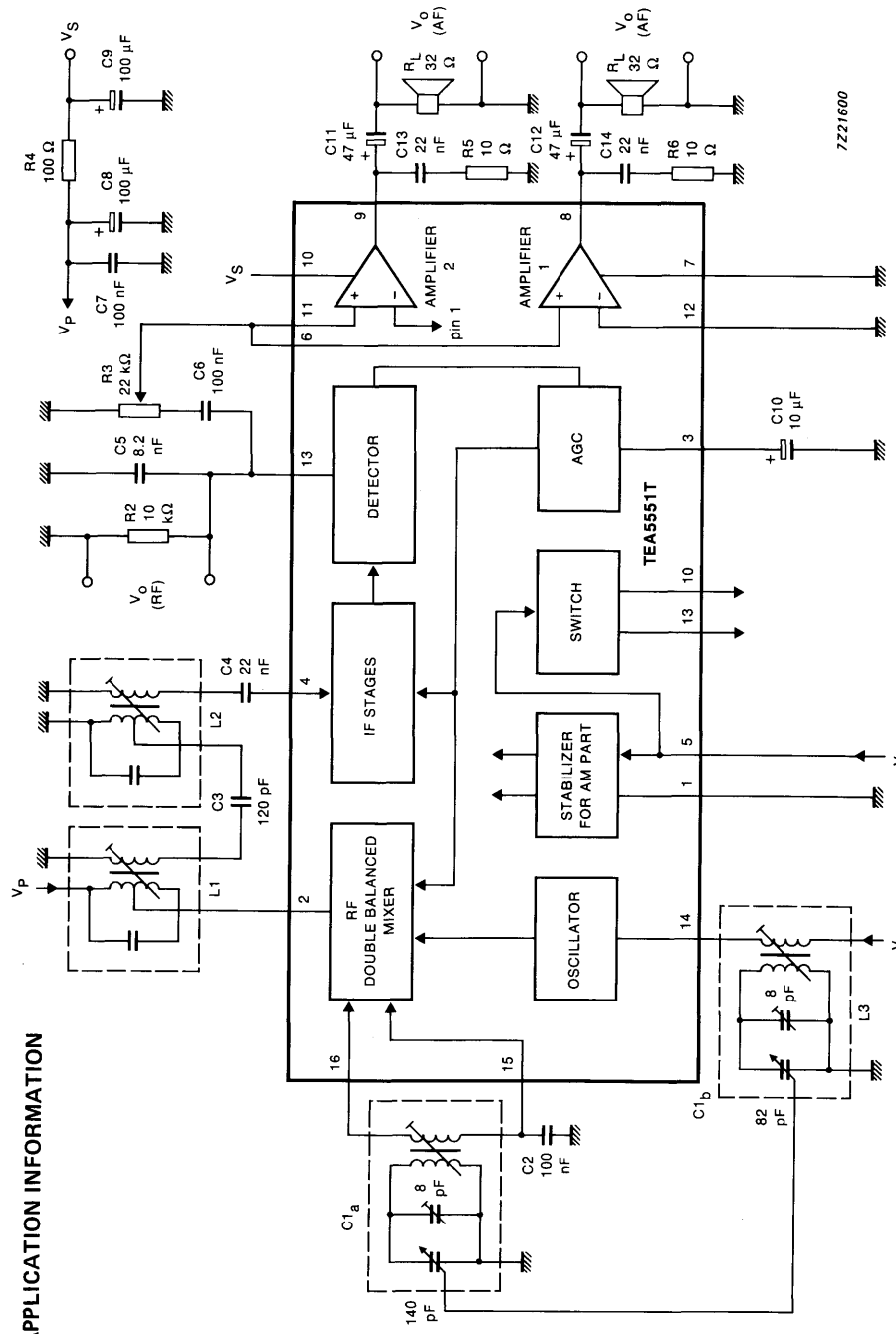
DEVELOPMENT DATA



Coil data: L1 7MCS2199
L2 7MCS2197
L3 7BRS10869X

Fig. 6 Test circuit.

APPLICATION INFORMATION

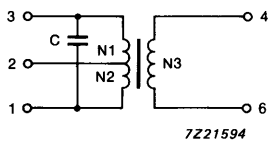


Coil data: L1 7MCS2199
L2 7MCS2197
L3 7BRS10869X

Fig. 7 Application circuit.

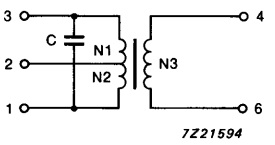
COIL DATA

AM coils (Figs 6 and 7)



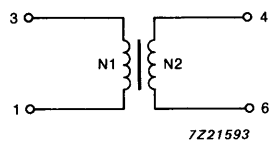
N1 = 60
N2 = 80
N3 = 15
C = 180 pF (internal)
L1–L3 = 643 μH
Qo = 110
Wire = 0.07 mm dia.
Coil type 7P–TOKO
Material 7MC

Fig. 8 IF bandpass filter (L1). TOKO sample no. 7MCS2199.



N1 = 125
N2 = 15
N3 = 6
C = 180 pF (internal)
L1–L3 = 643 μH
Qo = 110
Wire = 0.07 mm dia.
Coil type 7P–TOKO
Material 7MC

Fig. 9 IF bandpass filter (L2). TOKO sample no. 7MCS2197.



N1 = 90
N2 = 6
L1–L3 = 295 μH
Qo = 110
Wire = 0.07 mm dia.
Coil type 7P–TOKO
Material 7BR

Fig. 10 Oscillator coil (L3). TOKO sample no. 7BRS10869X.

RF/IF CIRCUIT FOR AM/FM RADIO

GENERAL DESCRIPTION

The TEA5570 is a monolithic integrated radio circuit for use in portable receivers and clock radios. The IC is also applicable to mains-fed AM and AM/FM receivers and car radio-receivers. Apart from the AM/FM switch function the IC incorporates for AM a double balanced mixer, 'one-pin' oscillator, i.f. amplifier with a.g.c. and detector, and a level detector for tuning indication. The FM circuitry comprises i.f. stages with a symmetrical limiter for a ratio detector. A level detector for mono/stereo switch information and/or indication complete the FM part.

Features

- Simple d.c. switching for AM to FM by only one d.c. contact to ground (no switch contacts in the i.f. channel, a.f. or level detector outputs)
- AM and FM gain control
- Low current consumption (I_{tot} = 6 mA)
- Low voltage operation (V_P = 2,7 to 9 V)
- Ability to handle large AM signals; good i.f. suppression
- Applicable for inductive, capacitive and diode tuning
- Double smoothing of a.g.c. line
- Short-wave range up to 30 MHz
- Lumped or distributed i.f. selectivity with coil and/or ceramic filters
- AM and a.g.c. output voltage control
- Distribution of PCB wiring provides good frequency stability
- Economic design for 'AM only' receivers

QUICK REFERENCE DATA (at T_{amb} = 25 °C)

Supply voltage	$V_P = V_{7-16}$	typ.	5,4 V
Supply current	I_7	typ.	6,2 mA
AM performance (pin 2) for m = 0,3			
Sensitivity			
at V_o = 10 mV	V_i	typ.	1,7 μV
at S/N = 26 dB	V_i	typ.	16 μV
A.F. output voltage at V_i = 1 mV	V_o	typ.	100 mV
Total harmonic distortion at V_i = 1 mV	THD	typ.	0,5 %
FM performance (pin 1) for Δf = ± 22,5 kHz			
limiting sensitivity, −3 dB	V_i	typ.	110 μV
Signal-to-noise ratio for V_i = 1 mV	S/N	typ.	65 dB
A.F. output voltage at V_i = 1 mV	V_o	typ.	100 mV
Total harmonic distortion at V_i = 1 mV	THD	typ.	0,3 %
AM suppression at V_i = 10 mV	AMS	typ.	50 dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

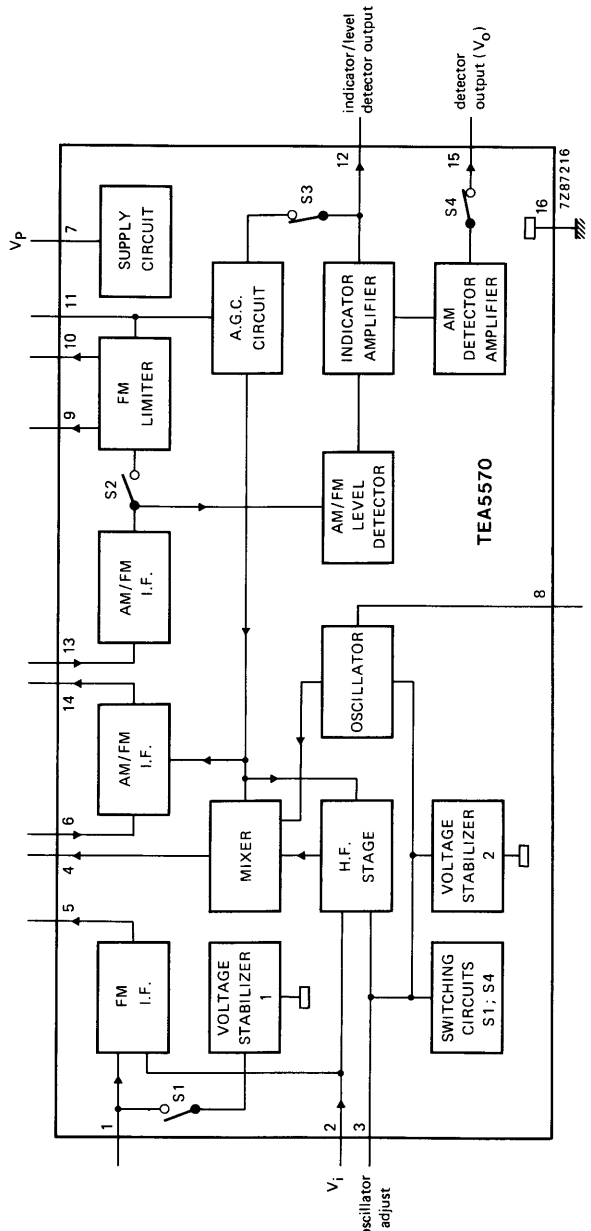


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_P = V_{7-16}$	max.	12 V
Voltage at pins 4, 5, 9 and 10 to pin 16 (ground)	V_{n-16}	max.	12 V
Voltage range at pin 8	V_{8-16}		$V_P \pm 0{,}5$ V
Current into pin 5	I_5	max.	3 mA
Total power dissipation	P_{tot}	see Fig. 2	
Storage temperature range	T_{stg}	−55 to +150	°C
Operating ambient temperature range	T_{amb}	−30 to +85	°C

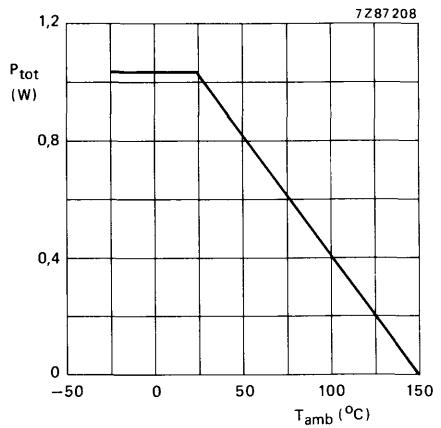


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 7)					
Supply voltage (note 1)	$V_P = V_{7\text{-}16}$	2,4	5,4	9,0	V
Voltages					
at pin 1 (FM)	$V_{1\text{-}16}$	–	1,42	–	V
at pin 1; $-I_1$ = 50 μA (FM)	$V_{1\text{-}16}$	–	1,28	–	V
at pins 2 and 3 (AM)	$V_{2,3\text{-}16}$	–	1,42	–	V
at pin 6	$V_{6\text{-}16}$	–	0,7	–	V
at pin 11	$V_{11\text{-}16}$	–	1,4	–	V
at pin 13	$V_{13\text{-}16}$	–	0,7	–	V
at pin 14	$V_{14\text{-}16}$	–	4,3	–	V
Currents					
Supply current	I_7	4,2	6,2	8,2	mA
Current supplied from pin 1 (FM)	$-I_1$	–	–	50	μA
Current supplied from pin 12	$-I_{12}$	–	–	20	μA
Current supplied from pin 15	$-I_{15}$	–	30	–	μA
Current into pin 4 (AM)	I_4	–	0,6	–	mA
Current into pin 5 (FM) (note 4)	I_5	–	0,35	–	mA
Current into pin 8 (AM)	I_8	–	0,3	–	mA
Current into pins 9, 10 (FM)	$I_{9,10}$	–	0,65	–	mA
Current into pin 14	I_{14}	–	0,4	–	mA
Power consumption	P	–	40	–	mW

A.C. CHARACTERISTICS

AM performance

V_P = 6 V; T_{amb} = 25 °C; r.f. condition: f_i = 1 MHz, m = 0,3, f_m = 1 kHz; transfer impedance of the i.f. filter $|Z_{tr}| = v_6/I_4$ = 2,7 kΩ; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
R.F. sensitivity (pin 2)					
at V_o = 30 mV	V_i	3,5	5,0	7,0	μV
at S + N/N = 6 dB	V_i	–	1,3		μV
at S + N/N = 26 dB	V_i	–	16	20	μV
at S + N/N = 50 dB	V_i	–	1	–	mV
Signal handling (THD ⩽ 10% at m = 0,8)	V_i	200	–	–	mV
A.F. output voltage at V_i = 1 mV	V_o	80	100	125	mV
Total harmonic distortion					
at V_i = 100 μV to 100 mV (m = 0,3)	THD	–	0,5	–	%
at V_i = 2 mV (m = 0,8)	THD	–	1,0	2,5	%
at V_i = 200 mV (m = 0,8)	THD	–	4,0	10	%
I.F. suppression at V_o = 30 mV (note 2)	α	26	35	–	dB
Oscillator voltage (pin 8; note 3)					
at f_{osc} = 1455 kHz	$V_{8\text{-}16}$	120	160	200	mV
Indicator current (pin 12) at V_i = 1 mV	I_{12}	–	200	230	μA

FM performance

V_P = 6 V; T_{amb} = 25 °C; i.f. condition: f_i = 10,7 MHz, Δf = ± 22,5 kHz, f_m = 1 kHz; transfer impedance of the i.f. filter $|Z_{tr}| = v_6/i_5$ = 275 Ω; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I.F. part					
I.F. sensitivity (adjustable; note 4)					
Input voltage					
at −3 dB before limiting	V_i	90	110	130	μV
at S + N/N = 26 dB	V_i	–	6	–	μV
at S + N/N = 65 dB	V_i	–	1	–	mV
A.F. output voltage at V_i = 1 mV	V_o	80	100	125	mV
Total harmonic distortion at V_i = 1 mV	THD	–	0,3	–	%
AM suppression (note 5)	AMS	–	50	–	dB
Indicator/level detector (pin 12)					
Indicator current	I_{12}	–	250	325	μA
D.C. output voltage					
at V_i = 300 μV	$V_{12\text{-}16}$	–	0,25	–	V
at V_i = 2 mV	$V_{12\text{-}16}$	–	1,0	–	V
AM to FM switch					
Switching current at $V_{3\text{-}16} < 1$ V	$-I_3$	–	–	400	μA

Notes to characteristics

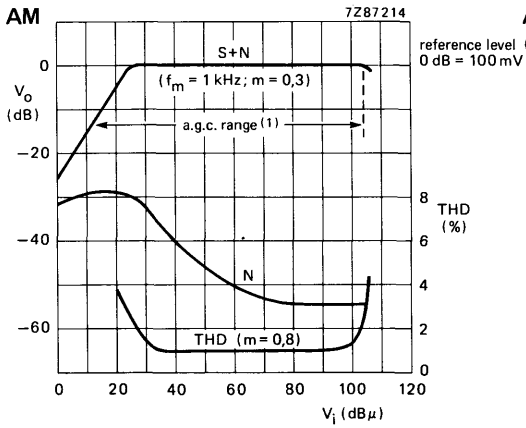
1. Oscillator operates at $V_{7\text{-}16} > 2{,}25$ V.
2. I.F. suppression is defined as the ratio $\alpha = 20 \log \frac{V_{i1}}{V_{i2}}$ where: V_{i1} is the input voltage at f = 455 kHz and V_{i2} is the input voltage at f = 1 MHz.
3. Oscillator voltage at pin 8 can be preset by R_{osc} (see Fig. 10).
4. Maximum current into pin 5 can be adjusted by R1 (see Fig. 10);
   $I_5 = \frac{V_{3\text{-}16}}{R1} - I_3$ when $V_{3\text{-}16} = 800$ mV; $I_3 = 400\ \mu$A.
5. AM suppression is measured with $f_m = 1$ kHz, m = 0,3 for AM; $f_m = 400$ Hz, $\Delta f = \pm 22{,}5$ kHz for FM.

Facility adaptation

Facility adaptation is achieved as follows (see Fig. 10):

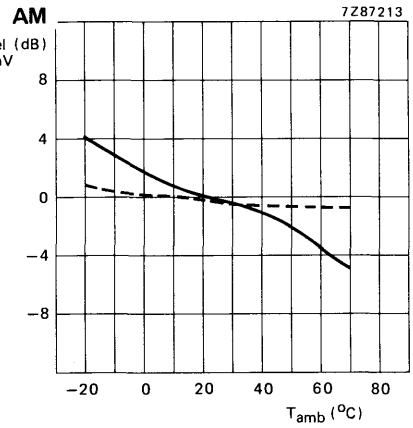
Facility	Component
FM sensitivity	R1 fixes the current at pin 5 ($I_5 = \frac{V_{3\text{-}16}}{R1} - 400\ \mu$A) (gain adjustable ± 10 dB; see note 4)
AM sensitivity	R11 and coil tapping
AM oscillator biasing	R_{osc}
AM output voltage	R7, R11
AM a.g.c. setting	R7

Typical graphs



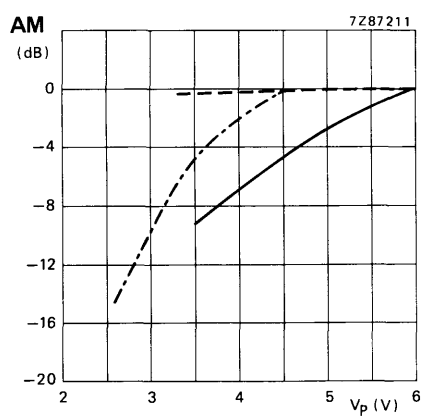
(1) A.G.C. range (figure of merit, FOM).

Fig. 3 Signal, noise and distortion as a function of input voltage (V_i). Measured at f_i = 1 MHz in test circuit Fig. 10.



——— sensitivity (V_i) at V_o = 30 mV; m = 0,3.
– – – – output voltage (V_o) at V_i = 2 mV; m = 0,3.

Fig. 4 Sensitivity (V_i), output voltage (V_o) as a function of temperature behaviour (T_{amb}). Measured at f_i = 1 MHz in test circuit Fig. 10.



——— sensitivity (V_i) at V_o = 30 V; m = 0,3: 6,0 V application.
—·—·— sensitivity (V_i) at V_o = 30 mV; m = 0,3: 4,5 V application.
– – – – output voltage (V_o) at V_i = 0,2 mV; m = 0,3.

Fig. 5 Sensitivity (V_i) and output voltage (V_o) as a function of supply voltage (V_P). Measured at f_i = 1 MHz in test circuit Fig. 10, for application V_P = 6 V. Also shown is the sensitivity for V_P = 4,5 V application (Fig. 16).

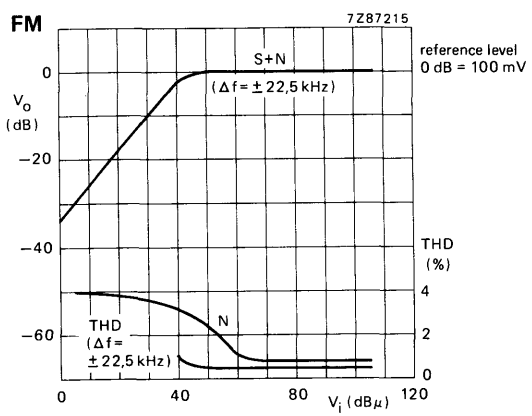
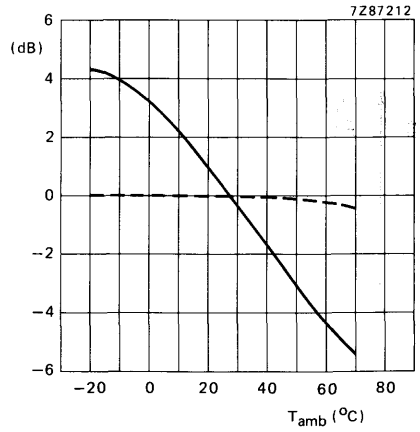


Fig. 6 Signal, noise and distortion as a function of input voltage (V_i). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

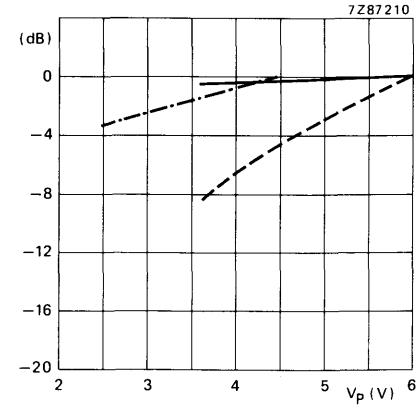
FM



——— sensitivity at −3 dB limiting.
– – – – output voltage (V_o) at V_i = 1 mV; $\Delta f = \pm 22$ kHz.

Fig. 7 Sensitivity (V_i), output voltage (V_o) as a function of temperature behaviour (T_{amb}). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

FM



——— sensitivity at −3 dB limiting: V_P = 6,0 V application.
–·–·– sensitivity at −3 dB limiting: V_P = 4,5 V application.
– – – – output voltage (V_o) at V_i = 1 mV; $\Delta f = \pm 22{,}5$ kHz.

Fig. 8 Sensitivity (V_i) and output voltage (V_o) as a function of supply voltage (V_P). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

AM/FM

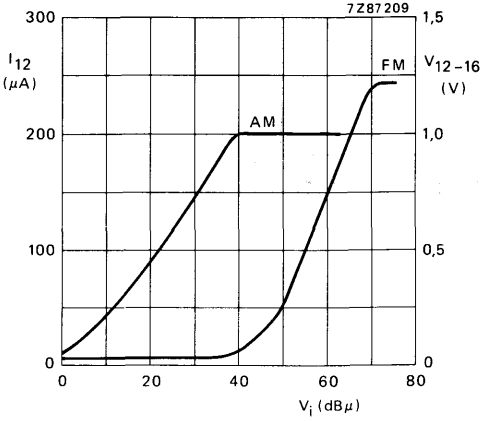


Fig. 9 Indicator output current (I_{12}) and d.c. output voltage ($V_{12\text{-}16}$): AM f_i = 1 MHz; FM f_i = 10,7 MHz as a function of input voltage (V_i). Measured in Fig. 10; V_P = 6 V; $R_{12\text{-}16}$ = 5 kΩ.

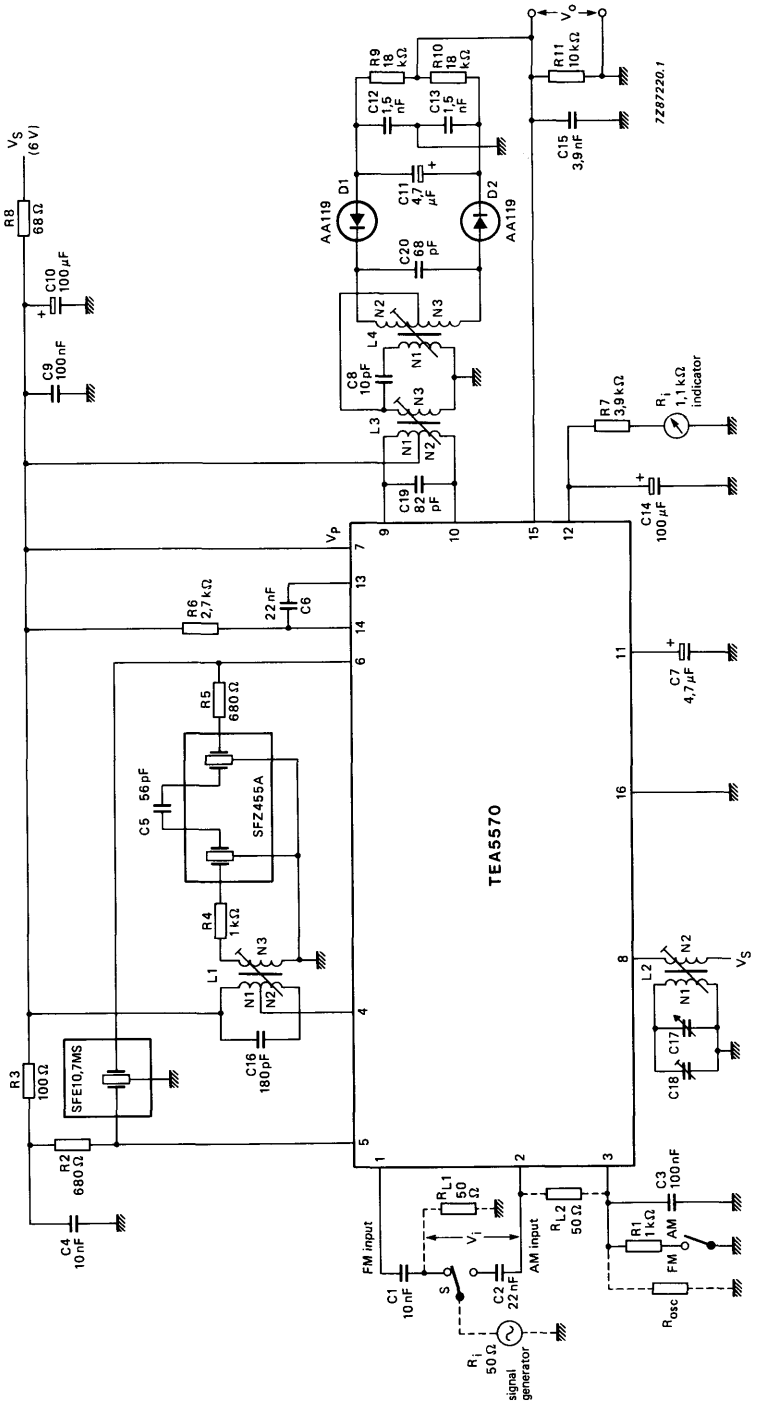


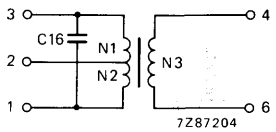
Fig. 10 Test circuit.

Coil data

The transfer impedance of the i.f. filter is:
AM: $|Z_{tr}| = v_6/i_4 = 2{,}7\ k\Omega$ (SFZ 455A).
FM: $|Z_{tr}| = v_6/i_5 = 275\ \Omega$ (SFE 10,7 MS).
See also Figs 11, 12, 13 and 14.

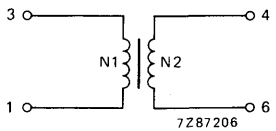
COIL DATA

AM i.f. coils (Fig. 10)



N1 = 73
N2 = 73
N3 = 9
C16 = 180 pF (internal)
Wire = 0,07 mm dia.

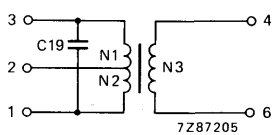
Fig. 11 I.F. bandpass filter (L1). TOKO sample no. 7 MC-7 P.



N1 = 90
N2 = 7
Wire = 0,07 mm dia.

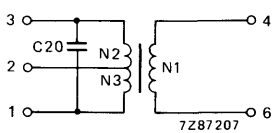
Fig. 12 Oscillator coil (L2). TOKO sample no. 7 BR-7 P.

FM i.f. coils (Fig. 10)



N1 = 5
N2 = 5
N3 = 4
C19 = 82 pF (internal)
Wire = 0,1 mm dia.

Fig. 13 Primary ratio detector coil (L3). TOKO sample no. 119 AN-7 P.

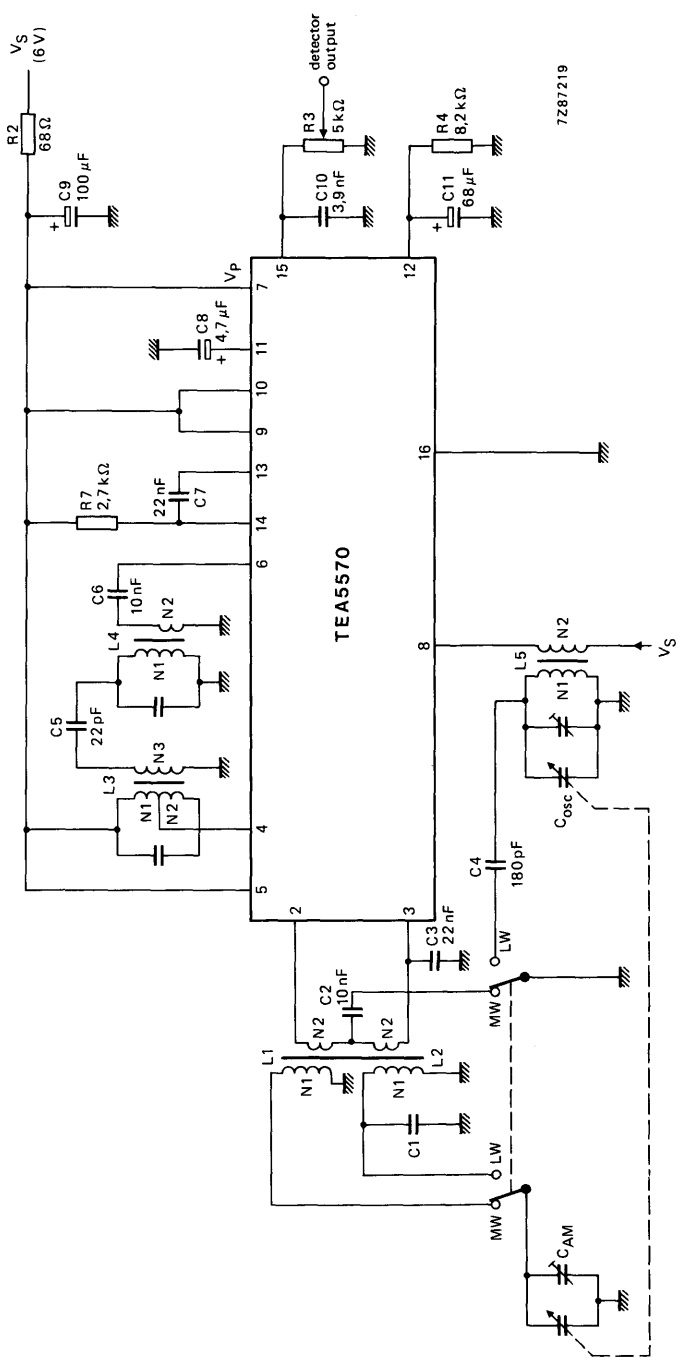


N1 = 2
N2 = 6
N3 = 6
C20 = 68 pF (internal)
Wire = 0,1 mm dia.

Fig. 14 Secondary ratio detector coil (L4). TOKO sample no. 119 AN-7 P.

APPLICATION INFORMATION

Figs 15 and 17 show the circuit diagrams for the application of 6 V AM MW/LW and 4,5 V AM/FM channels respectively, using the TEA5570. Fig. 16 shows the circuitry of the TEA5570.



Coil data

L3 N1 = 73 L4 N1 = 146 L5 N1 = 90
N2 = 73 N2 = 9 N2 = 6
N3 = 9 C = 180 pF
C = 180 pF

Fig. 15 Typical application circuit for 6 V AM MW/LW reception using the TEA5570.

APPLICATION INFORMATION (continued)

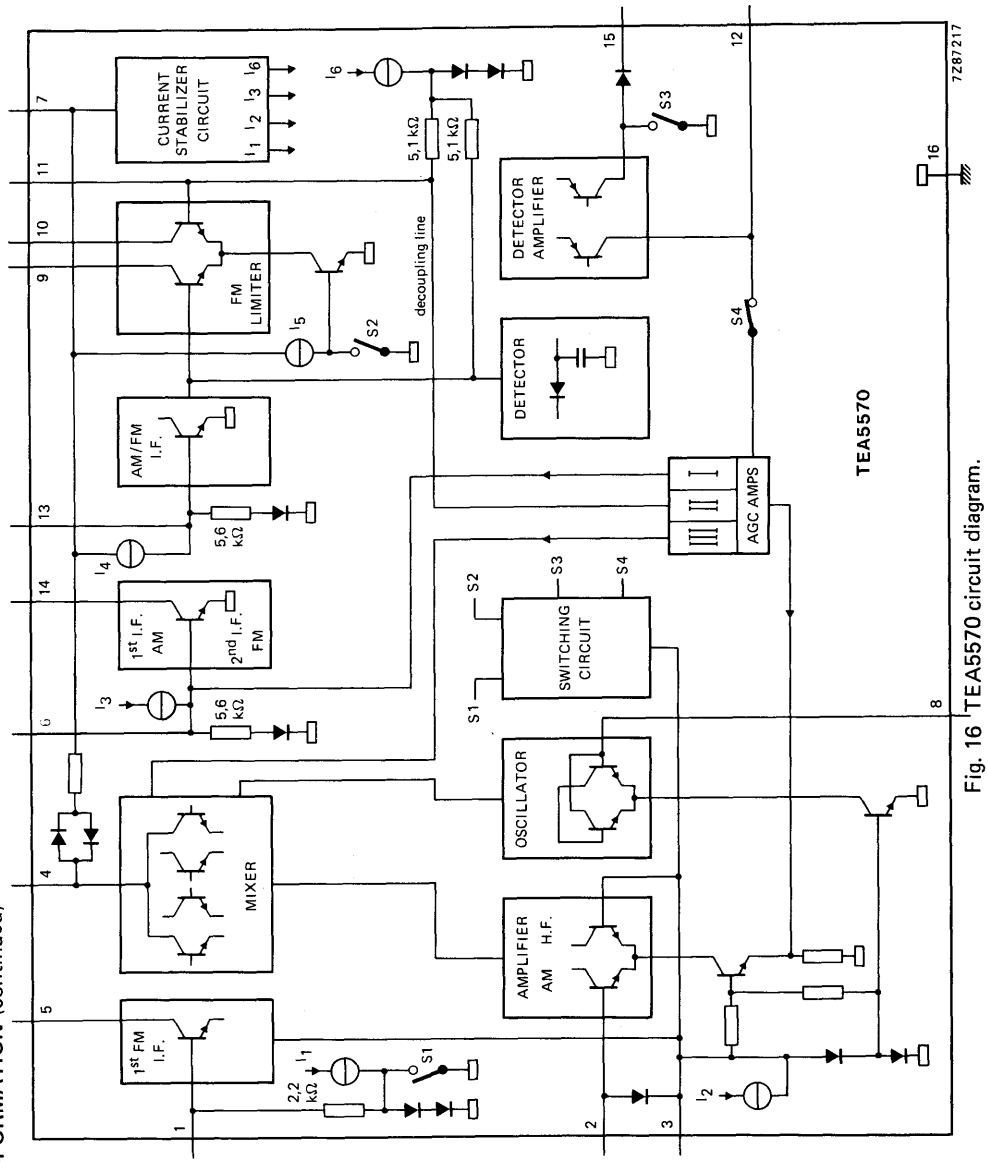


Fig. 16 TEA5570 circuit diagram.

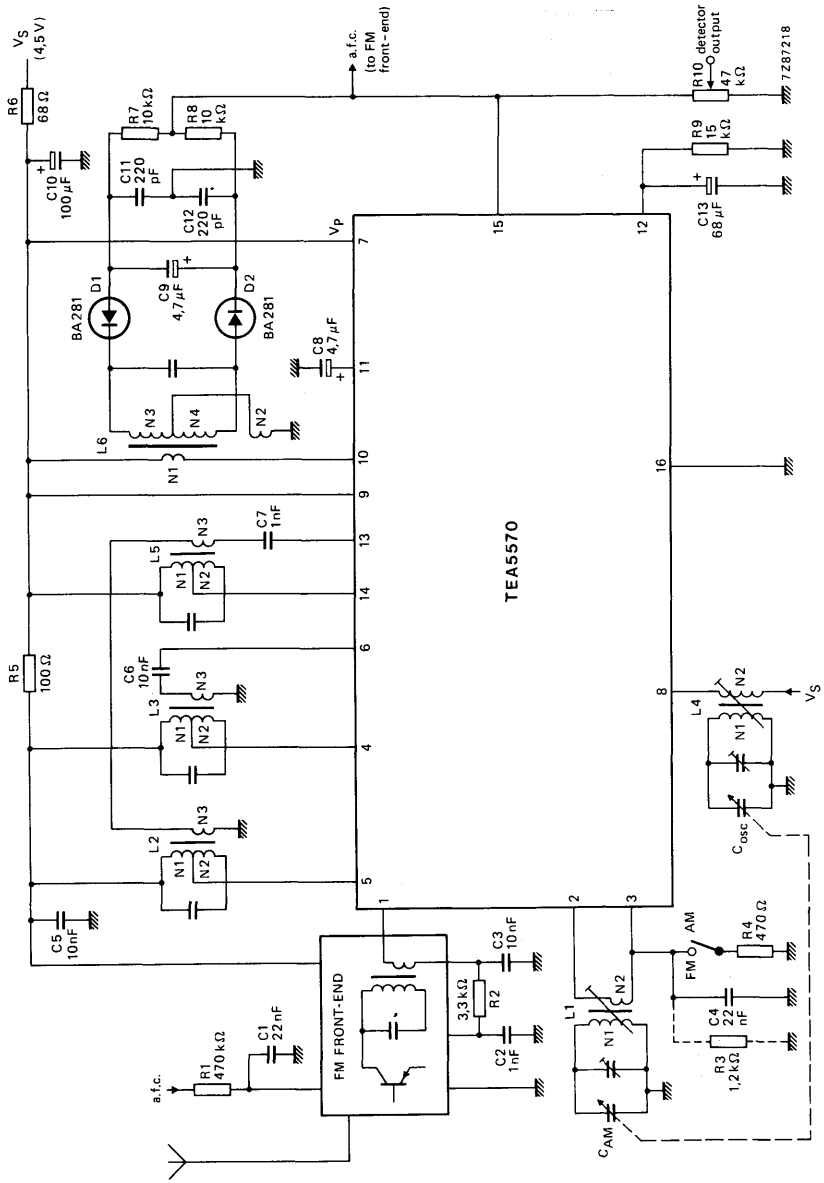


Fig. 17 Typical application circuit for 4,5 V AM/FM reception using the TEA5570 with coils and single-tuned ratio detector (with silicon diodes).

DETAILED APPLICATION INFORMATION WILL BE SUPPLIED ON REQUEST.

Coil data

L2	N1 = 3	L3	N1 = 33	L4	N1 = 90	L5	N1 = 33
	N2 = 8		N2 = 113		N2 = 6		N2 = 113
	N3 = 1		N3 = 9				N3 = 9
	C = 82 pF		C = 180 pF				

L6	N1 = 50	
	N2 = 5	
	N3 = 4,5	
	N4 = 6,5	
	C = 82 pF	

PLL STEREO DECODER

GENERAL DESCRIPTION

The TEA5580 PLL stereo decoder is for car, portable and mains-fed medium-fi radios and radio recorders. It features a 228 kHz voltage-controlled oscillator (VCO) that is locked to the 19 kHz stereo pilot tone by a phase-locked loop (PLL) system. Subcarrier frequencies of 19, 38, 57 and 114 kHz are regenerated via I^2L logic from the VCO output.

The PLL phase detector suppresses phase distortion due to the 57 kHz pilot tone from the German 'Verkehrs Warnfunk' (VWF) traffic warning system. Typical suppression of the 19 kHz stereo pilot tone is 50 dB, or up to 60 dB with adjustment of the pilot-cancelling resistor (R3, Figs 3 and 4). Adjacent channel interference is prevented by the use of two demodulators, one driven by the 38 kHz decoding signal and the other at 114 kHz to suppress the third harmonic of the multiplexed input signal.

The gain of the input amplifier can be adjusted by an external resistor and the circuit includes compensation for an IF filter typical roll-off frequency of 50 kHz (2 dB down at 38 kHz).

The supply voltage range of the circuit is 3,6 V to 16 V.

Features

- Wide supply voltage range
- Automatic mono/stereo switching (pilot presence detector)
- Smooth stereo-to-mono change-over at weak signals (signal-dependent stereo channel separation)
- LED driver for stereo/mono indicator
- Suppresses:
  - third harmonics (114 kHz) of multiplexed signal to prevent interference from strong adjacent channels;
  - phase distortion due to the 57 kHz signal from VWF transmitters
- Pilot cancelling circuit to give added suppression of 19 kHz pilot tone
- IF filter roll-off compensation

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

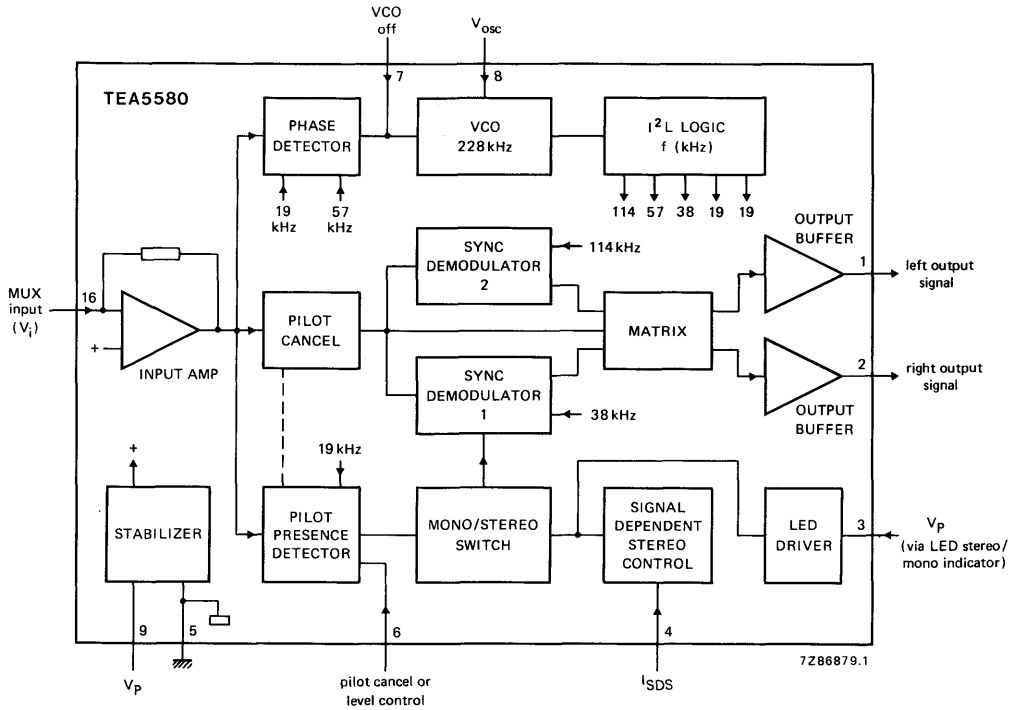


Fig. 1 Block diagram.

Note

Do **not** connect pins 10, 11, 12, 13, 14 or 15.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pins 3 and 9)	V_{3-5}, V_{9-5}	–	18	V
LED-driver current (peak value)	$-I_{3M}$	–	75	mA
Total power dissipation	P_{tot}	see derating curve Fig. 2		
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 80	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 75 K/W

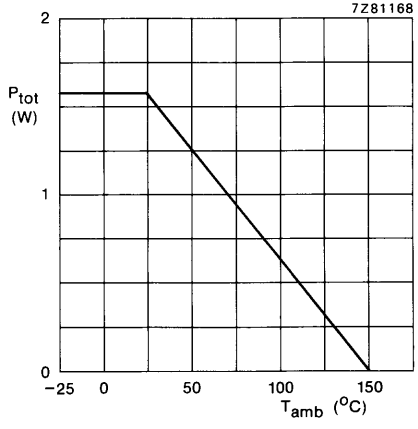


Fig. 2 Power derating curve.

CHARACTERISTICS

Measured in the circuit of Fig. 3; V_P = 7,5 V; T_{amb} = 25 °C; all d.c. voltages are with respect to pin 5; all currents are positive into the IC; a.c. measurements have an input MUX-signal of 1 V (peak-to-peak); V_{pilot} = 32 mV; f_m = 1 kHz; de-emphasizing time = 50 μs; oscillator adjusted to I_{osc} at V_i = 0 V; values are measured with an external roll-off network of 50 kHz (2 dB down at 38 kHz) at the input (dashed components R1 and C1 in Fig. 3); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
D.C. Characteristics					
Supply voltage (note 1)	V_P	3,6	7,5	16	V
Total current consumption at V_P = 7,5 V (note 2)	I_P	–	10	13,5	mA
Dissipation at V_P = 7,5 V (note 2)	P_{tot}	–	75	–	mW
Bias voltage (pin 16)	V_{16-5}	–	1,4	–	V
Input current (pin 4)	I_4	–	–	400	μA
D.C. output current (pin 1)	$-I_1$	195	275	390	μA
D.C. output current (pin 2)	$-I_2$	195	275	390	μA
Output current (pin 3) (LED driver transistor)	$-I_3$	–	–	50	mA
Switch "VCO-OFF" voltage at pin 7	V_{off}	–	2,2	–	V
Switch "VCO-OFF" current into pin 7	I_7	–	–	50	μA
A.C. Characteristics					
Overall gain (mono)	Go (V_o/V_i)	7	8	9,5	dB
Gain input amplifier (adjustable) (Fig. 5)	G	0	–	20	dB
AF output voltage (mono) (r.m.s. value)	$V_{1-5} = V_{2-5}$	800	900	–	mV
Output channel unbalance	$\Delta V_o/V_o$	–	± 0,2	± 1,0	dB
Total harmonic distortion at $V_{o(rms)}$ = 0,9 V (note 3)	THD	–	0,2	0,5	%
Total harmonic distortion at $V_{o(rms)}$ = 1,0 V	THD	–	1,0	–	%
Channel separation L = 1; R = 0	α	26	40	–	dB
Signal-to-noise ratio bandwidth 20 Hz to 16 kHz	S/N	–	76	–	dB
Bandwidth IEC 79 (A-curve)	S/N	–	82	–	dB
Input impedance (external)	$\lvert Z_i \rvert$	–	47	–	kΩ
Output impedance (external) R = 12 kΩ; C = 3,9 nF	$\lvert Z_o \rvert$	–	9,3	–	kΩ

parameter	symbol	min.	typ.	max.	unit
SDS control (Fig. 6)					
10 dB channel separation	I_4	–	50	–	μA
Full stereo channel separation > 26 dB	I_4	100	–	–	μA
Full mono channel separation < 1 dB	I_4	–	–	10	μA
Stereo/mono switch					
R3 = 180 kΩ; note 4; Fig. 7					
Switching to stereo	V_i	–	18	24	mV
Switching to mono	V_i	8	–	–	mV
Hysteresis	ΔV_i	–	4	–	mV
Carrier and harmonic suppression at the output (note 5)					
Pilot signal suppression f = 19 kHz; R3 = 180 kΩ; note 4; Fig. 4	α_{19}	40	50	–	dB
Subcarrier suppression f = 38 kHz	α_{38}	–	50	–	dB
f = 57 kHz	α_{57}	–	50	–	dB
f = 228 kHz	α_{228}	–	80	–	dB
Intermodulation suppression (note 6) f_m = 10 kHz; spurious signal f_s = 1 kHz	α_2	–	60	–	dB
f_m = 13 kHz; spurious signal f_s = 1 kHz	α_3	–	60	–	dB
VWF tone suppression f = 57 kHz (note 7)	α_{57}	–	80	–	dB
SCA tone rejection f = 67 kHz (note 8)	α_{67}	–	80	–	dB
ACI rejection (note 9) f = 114 kHz	α_{114}	–	90	–	dB
f = 190 kHz	α_{190}	–	60	–	dB

Notes see next page.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Ripple rejection					
f = 100 Hz; V_{ripple} = 200 mV; measured including RC network in supply line					
V_P = 7,5 V	RR_{100}	–	42	–	dB
V_P = 6,0 V	RR_{100}	–	46	–	dB
V_P = 3,6 V	RR_{100}	–	35	–	dB
VCO					
Oscillator frequency adjustable with R8	f_{osc}	–	228	–	kHz
Capture range (deviation from 228 kHz centre frequency) V_{pilot} = 9% (note 10)	$\Delta f/f$	–	8	–	%
Temperature coefficient	TC	–	+ 400 x 10^{-6}	–	K^{-1}

Notes to the characteristics

1. Minimum supply voltage only applicable in 6 V portable.
2. Without LED-driver current.
3. Guaranteed for mono, mono + pilot, stereo.
4. Also adjustable.
5. Reference output voltage at 1 kHz (measured channel R, pin 2).
6. Intermodulation suppression (BFC: Beat-Frequency Components):

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 1 kHz})}\ ;\ f_s = (2 \times 10\ \text{kHz}) - 19\ \text{kHz}$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 1 kHz})}\ ;\ f_s = (3 \times 13\ \text{kHz}) - 38\ \text{kHz}$$

measured with 91% mono signal; f_m = 10 or 13 kHz; 9% pilot signal.

7. Traffic radio (VWF) tone suppression:

$$\alpha_{57} = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 1 kHz} \pm 23\ \text{Hz})}$$

measured with 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 kHz; 60% AM modulated with f_{mod} = 23 Hz).

8. SCA (Subsidary Communication Authorization) tone rejection:

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 9 kHz})}\ ;\ f_s = (2 \times 38\ \text{kHz}) - 67\ \text{kHz}$$

measured with 81% mono signal; f_m = 1 kHz; 9% pilot signal; 10% SCA-subcarrier (f_s = 67 kHz, unmodulated).

9. ACI (Adjacent Channel Interference) rejection at:

$$\alpha_{114} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 4\ \text{kHz})};\ f_s = (3 \times 38\ \text{kHz}) - 110\ \text{kHz}$$

$$\alpha_{190} = \frac{V_{o(signal)}\ (\text{at } 1\ \text{kHz})}{V_{o(spurious)}\ (\text{at } 4\ \text{kHz})};\ f_s = (5 \times 38\ \text{kHz}) - 186\ \text{kHz}$$

measured with 90% mono signal; f_s = 1 kHz; 9% pilot signal; 1% spurious signal (f_s = 110 or 186 kHz, unmodulated).

10. The capture range of the PLL may be decreased to 4% by changing the value of C2 to 470 nF (see Fig. 4), if a small ambient temperature range is provided.

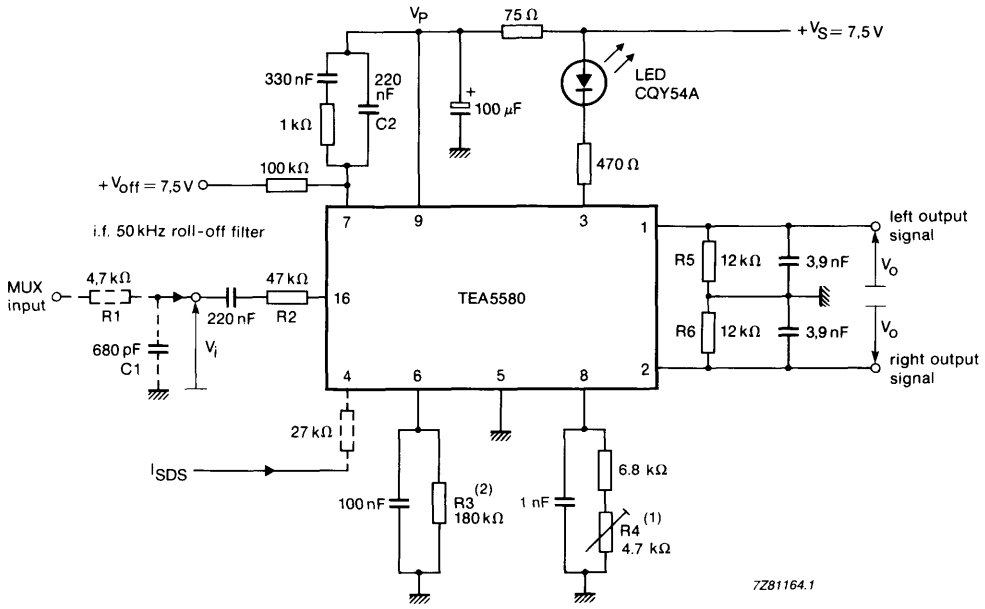


Fig. 3 Car radio application and test circuit.

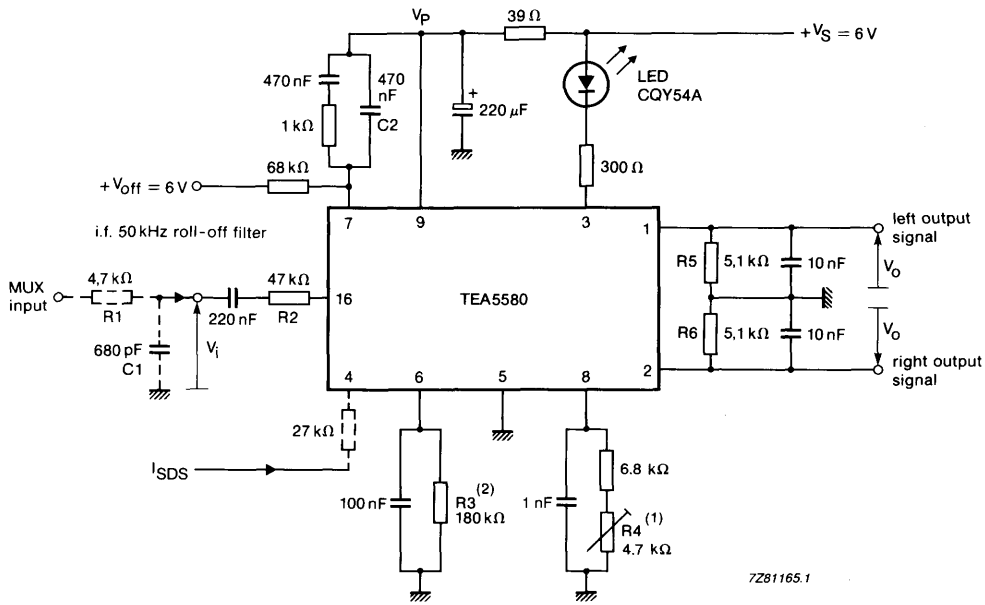
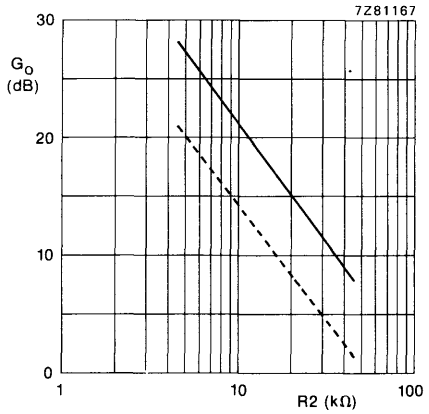


Fig. 4 Portable application circuit.

Notes to Figs 3 and 4

(1) R4: VCO frequency adjustment (228 kHz).

(2) R3: pilot cancelling or pilot level adjustment; best adjustment obtained with 470 kΩ potentiometer (see Figs 7 and 8); adjust for pilot cancellation of approx. 58 dB ± 10 dB and pilot sensitivity (mono to stereo) of approx. 23 mV ± 3 mV.



——— R5 = R6 = 12 kΩ
– – – R5 = R6 = 5,1 kΩ

Fig. 5 Overall gain as a function of input resistance (R2).

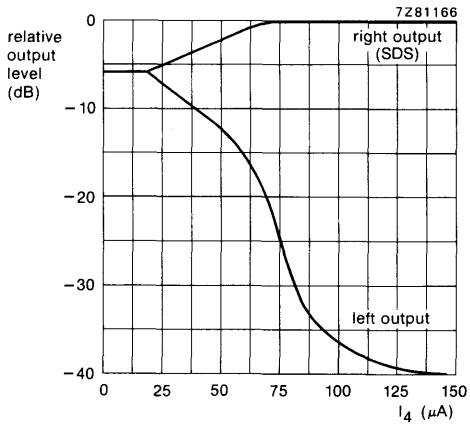
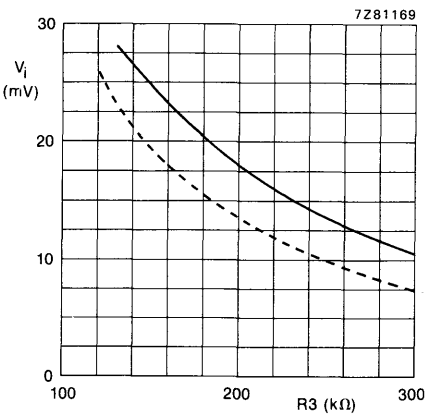


Fig. 6 Relative output level as a function of the signal dependent stereo (SDS) current (I_4); typical curves.



——— stereo "ON"
– – – stereo "OFF"

Fig. 7 Pilot sensitivity: pilot input voltage (V_i) as a function of pilot adjustment resistor R3; typical curves.

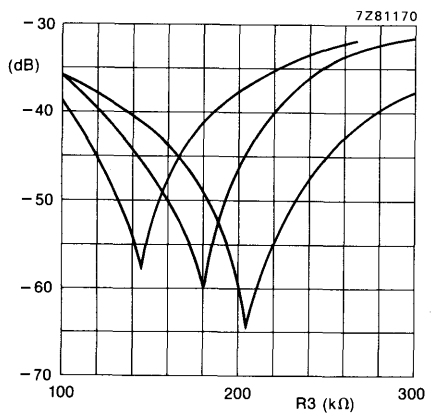


Fig. 8 Random samples of pilot cancelling: $\frac{V_o \text{ (at 19 kHz)}}{V_o \text{ (at 1 kHz)}}$ in dB as a function of R3; $V_{i(p\text{-}p)}$ = 1 V; V_{pilot} = 32 mV (9%).

PLL STEREO DECODER

GENERAL DESCRIPTION

The TEA5581 PLL stereo decoder is for car and medium-fi radios. It incorporates all the features provided by the TEA5580 together with a source selector, muting circuit and output amplifiers with adjustable gain. It also features a switch for radio or cassette function and a 228 kHz voltage-controlled oscillator (VCO) that is locked to the 19 kHz stereo pilot tone by a phase-locked loop (PLL) system. Subcarrier frequencies of 19, 38, 57 and 114 kHz are regenerated via I^2L logic from the VCO output.

The PLL phase detector suppresses phase distortion due to the 57 kHz pilot tone from the German 'Verkehrs Warnfunk' (VWF) traffic warning system. Typical suppression of the 19 kHz stereo pilot tone is 40 dB. Adjacent channel interference is prevented by the use of two demodulators, one driven by the 38 kHz decoding signal and the other at 114 kHz to suppress the third harmonic of the multiplexed input signal.

The gain of the input amplifier can be adjusted by an external resistor and the circuit includes compensation for an IF filter typical roll-off frequency of 50 kHz (2 dB down at 38 kHz).

The supply voltage range of the circuit is 7 V to 16 V.

Features

- Wide supply voltage range
- Automatic mono/stereo switching (pilot presence detector)
- Smooth stereo-to-mono change-over at weak signals (signal-dependent stereo channel separation)
- LED driver for stereo/mono indicator
- Suppresses:

  third harmonics (114 kHz) of multiplexed signal to prevent interference from strong adjacent channels;

  phase distortion due to the 57 kHz signal from VWF transmitters
- Pilot cancelling circuit to give added suppression of 19 kHz stereo pilot tone (up to 25 dB)
- IF filter roll-off compensation
- Source selector for radio or cassette input (typ. 90 dB)
- Mute circuit for 90 dB (typ.) muting of the output level
- Matrix and two output buffers with adjustable gain (max. 20 dB)

PACKAGE OUTLINES

TEA5581 : 16-lead DIL; plastic (SOT38).
TEA5581T: 16-lead mini-pack; plastic (SO16L; SOT162A).

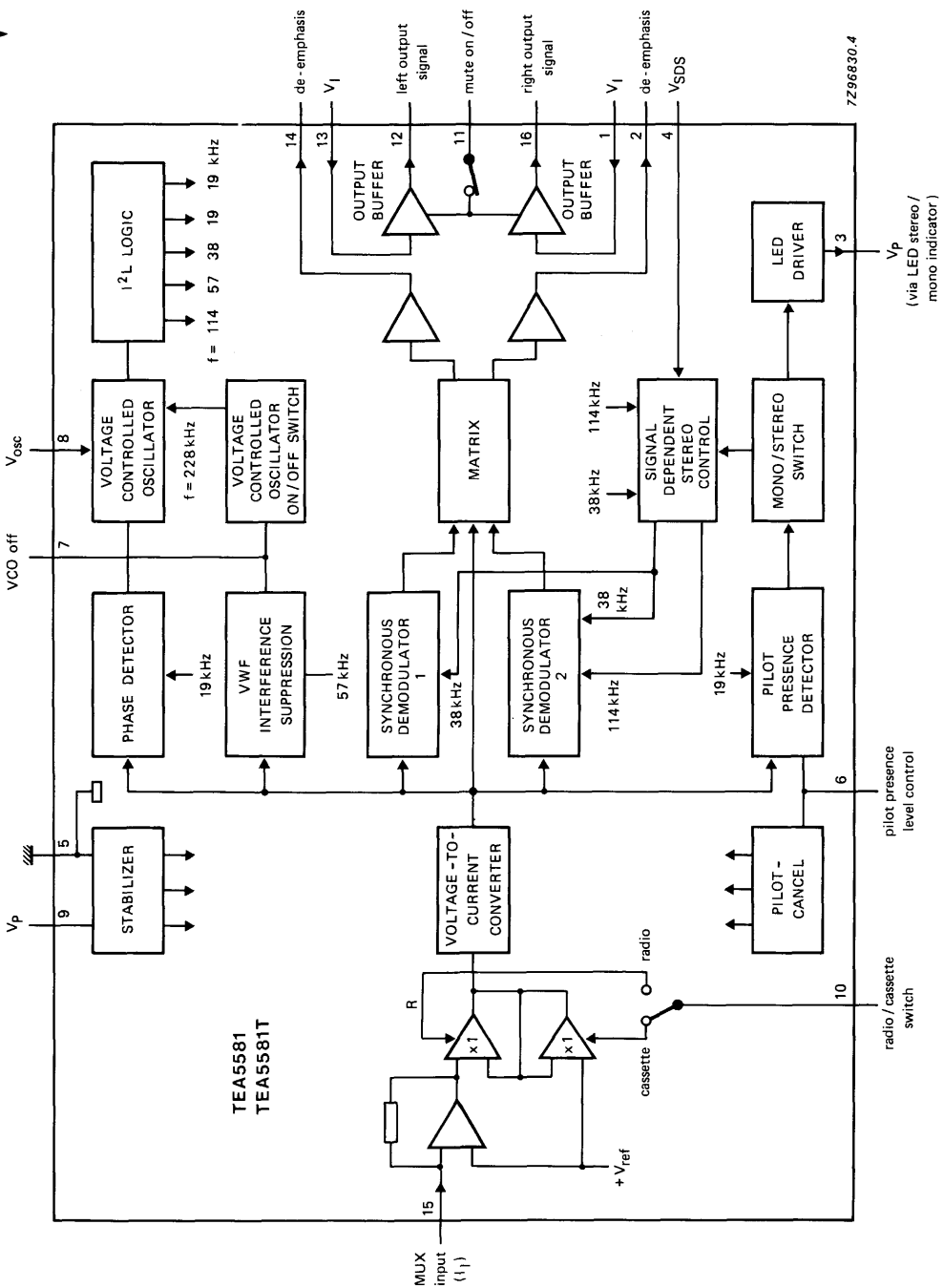


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{3-5}, V_{9-5}	–	18	V
LED-driver current (peak value)		$-I_{3M}$	–	75	mA
Total power dissipation		P_{tot}	see derating curve Fig. 2		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−30	+80	°C
Electrostatic handling *		V_{es}	−600	+600	V

From junction to ambient in free air

SOT38	$R_{th\ j-a}$	75 K/W
SOT162	$R_{th\ j-a}$	95 K/W

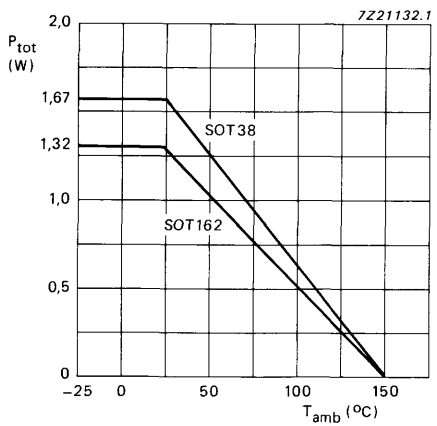


Fig. 2 Power derating curve.

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

DC CHARACTERISTICS

Measured in the circuit of Fig. 7; V_S = 8.5 V; T_{amb} = 25 °C; all DC voltages are with respect to pin 5; all currents are positive into the IC.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	R1 = 75 Ω	V_S	7.0	8.5	16	V
Total current consumption	without LED driver	I_{tot}	–	15	20	mA
Power dissipation		P_{tot}	–	125	–	mW
Voltage						
pin 15		V_{15}	–	2.1	–	V
pins 12 and 16		V_{12}, V_{16}	3.2	3.6	4.0	V
DC output current						
pins 2 and 14		$-I_{14}$, $-I_2$	225	320	450	μA
Output current						
pin 3		$-I_3$	–	–	20	mA
Switch "VCO-OFF"						
voltage		V_7	–	2.2	–	V
Switch "VCO-OFF"						
current		I_7	–	50	75	μA

AC CHARACTERISTICS

Measured in the circuit of Fig. 7; V_S = 8.5 V; T_{amb} = 25 °C; AC measurements have an input MUX-signal of 1 V (peak-to-peak); V_{pilot} = 32 mV (9%); f_m = 1 kHz; oscillator adjusted to 228 kHz at V_i = 0 V; values are measured with an external roll-off network of 50 kHz (2 dB down at 38 kHz) at the input (dashed components R_S and C_S in Fig. 7); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Transimpedance		V_O/I_I	0.13	0.15	0.17	V/μA
Input current (RMS value)		$I_{I(rms)}$	–	–	12	μA
Overall gain	mono; R3 = 47 kΩ	G_o (V_o/V_i)	9.0	10.0	11.0	dB
AF output voltage (RMS value)		$V_{12} = V_{16}$	0.95	1.14	1.33	V
AF output voltage (RMS value)		$V_2 = V_{14}$	–	–	500	mV
Total harmonic distortion	note 1; $V_{O(rms)}$ = 1 V	THD	–	0.1	0.5	%
Output voltage	THD = 1%	$V_{12} = V_{16}$	–	1.5	–	V
Output channel unbalanced		V_{12}/V_{16}	–	0.2	1.0	dB
Channel separation	IF roll-off frequency = 50 kHz L = 1; R = 0	α	26	40	–	dB
S/N ratio	bandwidth 20 Hz to 16 kHz	S/N	–	76	–	dB
	bandwidth IEC 79 (curve Din A)	S/N	–	82	–	dB
SDS control	see Fig. 6					
Channel separation	V_4 = 1.0 V	α	5	10	15	dB
Full stereo	channel separation ⩾ 26 dB	V_4	–	1.2	1.25	V
Full mono	channel separation ⩽ 1 dB	V_4	0.75	0.8	–	V
Stereo/mono switch	note 2; see Fig. 5; R4 = 180 kΩ					
Switching to:						
stereo		V_{pilot}	–	14	20	mV
mono		V_{pilot}	4	–	–	mV
Hysteresis		ΔV_I	–	4.5	–	mV

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Carrier and harmonic suppression at the output	note 3					
Pilot signal suppression	f = 19 kHz; R4 = 180 kΩ; note 2; see Figs 3 and 4	α_{19}	32	40	–	dB
Subcarrier suppression						
f = 38 kHz		α_{38}	–	50	–	dB
f = 57 kHz		α_{57}	–	50	–	dB
f = 228 kHz		α_{228}	–	75	–	dB
Intermodulation suppression	note 4					
f_m = 10 kHz	spurious signal f_s = 1 kHz	α_2	–	50	–	dB
f_m = 13 kHz	spurious signal f_s = 1 kHz	α_3	–	50	–	dB
VWF tone suppression f = 57 kHz	note 5	α_{57}	–	80	–	dB
SCA tone rejection f = 67 kHz	note 6	α_{67}	–	70	–	dB
ACI rejection	note 7					
f = 114 kHz		α_{114}	–	90	–	dB
f = 190 kHz		α_{190}	–	60	–	dB
Ripple rejection						
Ripple rejection	f = 100 Hz; V_{ripple} = 100 mV; mono	RR_{100}	–	50	–	dB
VCO						
Oscillator frequency adjustable with R5		f_{osc}	–	228	–	kHz
Capture range	deviation from 228 kHz centre frequency; V_{pilot} = 32 mV	$\Delta f/f$	–	6	–	%
Temperature coefficient	uncompensated	TC	–	-200×10^{-6}	–	K^{-1}

parameter	conditions	symbol	min.	typ.	max.	unit
Source selector						
Suppression of MPX signal	$V_{10} \geqslant 2$ V	α	80	90	–	dB
Switching level	cassette to radio					
voltage		V_{IL}	–	–	0.8	V
current		I_{IL}	–	10	25	μA
Switching level	radio to cassette					
voltage		V_{IH}	2.0	–	V_S	V
current		I_{IH}	–	–	1	μA
Output amplifiers						
Gain	note 8; R_6/R_7	G_v	–	–	20	dB
Output impedance		Z_o	–	200	500	Ω
External load impedance		$\|Z_l\|$	5	–	–	kΩ
Suppression (mute)	$V_{11} = \leqslant 0{,}8$ V	α	84	90	–	dB
DC offset voltage at outputs during mute switching	mute OFF-to-ON	ΔV_{12}, ΔV_{16}	–	1.0	–	mV
	mute ON-to-OFF	ΔV_{12}, ΔV_{16}	–	2.0	–	mV
Muting circuit						
Input voltage	mute ON	V_{IL}	–	–	0.8	V
	mute OFF	V_{IH}	2.0	–	V_S	V
Input current	mute ON	I_{IL}	–	10	25	μA
	mute OFF	I_{IH}	–	–	1	μA

Notes to the characteristics

1. Guaranteed for mono, mono + pilot and stereo.
2. Also adjustable.
3. Reference output voltage at 1 kHz (measured channel R, pin 16).
4. Intermodulation suppression (Beat-Frequency Components):

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (2 \times 10\text{ kHz}) - 19\text{ kHz}$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (3 \times 13\text{ kHz}) - 38\text{ kHz}$$

   measured with 91% mono signal; f_m = 10 or 13 kHz; 9% pilot signal.

5. Traffic radio (VWF) tone suppression:

$$\alpha_{57} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz} \pm 23\text{ Hz})}$$

   measured with 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 kHz; 60% AM modulated with f_{mod} = 23 Hz).

6. SCA (Subsidiary Communication Authorization) tone rejection:

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 9\text{ kHz})};\ f_s = (2 \times 38\text{ kHz}) - 67\text{ kHz}$$

   measured with 81% mono signal; f_m = 1 kHz; 9% pilot signal; 10% SCA-subcarrier (f_s = 67 kHz, unmodulated).

7. ACI (Adjacent Channel Interference) rejection at:

$$\alpha 114 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 4\text{ kHz})};\ f_s = (3 \times 38\text{ kHz}) - 110\text{ kHz}$$

$$\alpha 190 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 4\text{ kHz})};\ f_s = (5 \times 38\text{ kHz}) - 186\text{ kHz}$$

   measured with 90% mono signal; f_s = 1 kHz; 9% pilot signal; 1% spurious signal (f_s = 110 or 186 kHz, unmodulated).

8. Maximum permitted value of feedback resistor = 220 kΩ.

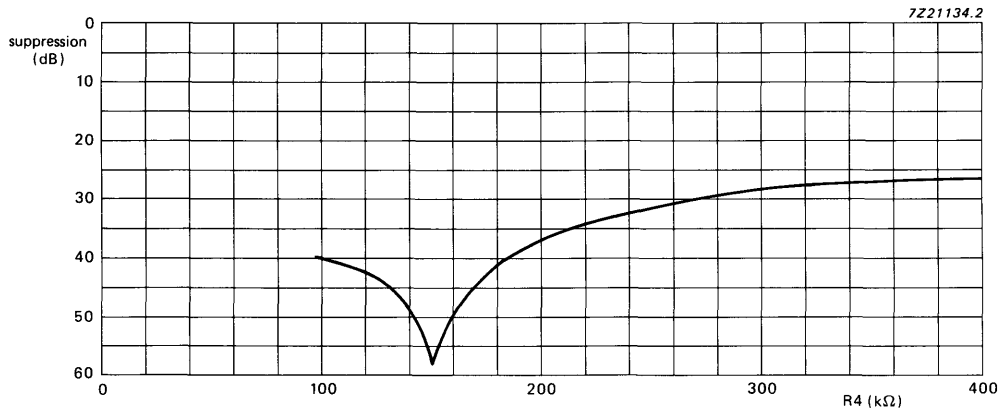
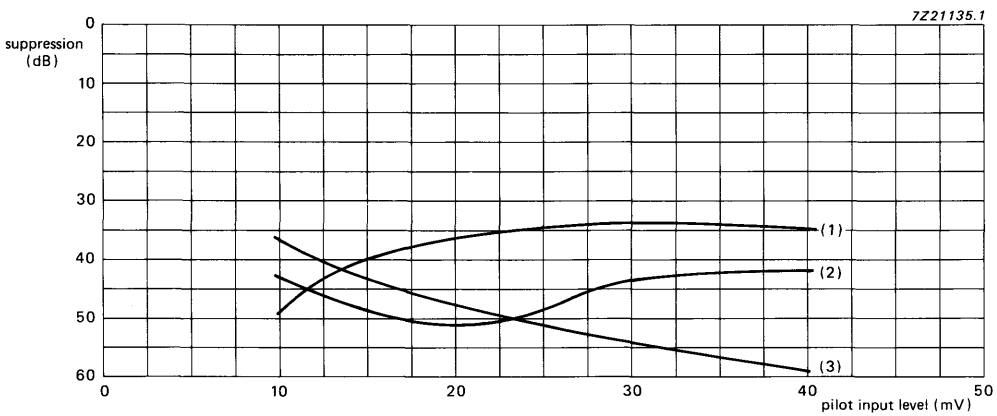
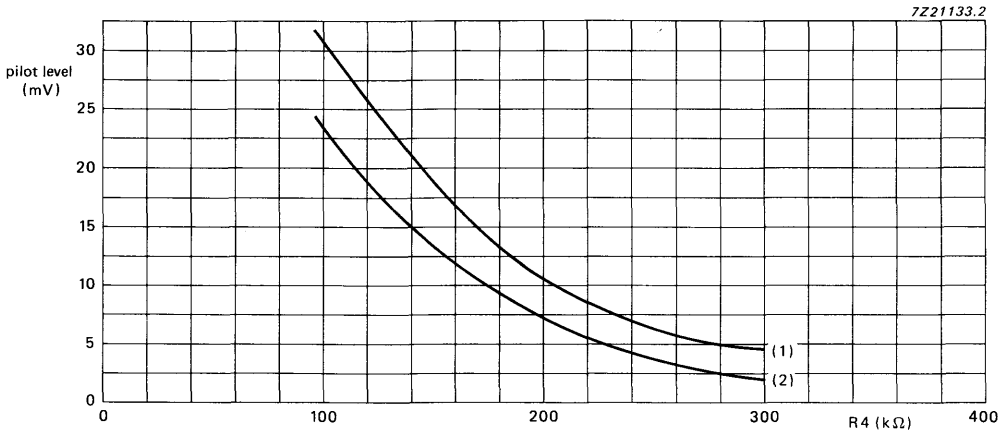


Fig. 3 Pilot suppression plotted against resistance (R4).



(1) 220 kΩ
(2) 180 kΩ
(3) 150 kΩ

Fig. 4 Pilot suppression plotted against pilot input voltage level.



(1) Switching from mono to stereo.
(2) Switching from stereo to mono.

Fig. 5 Pilot sensitivity against resistance (R4).

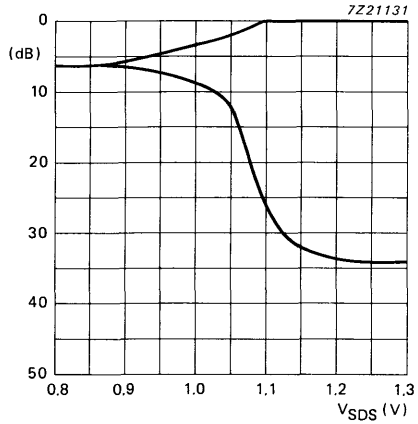
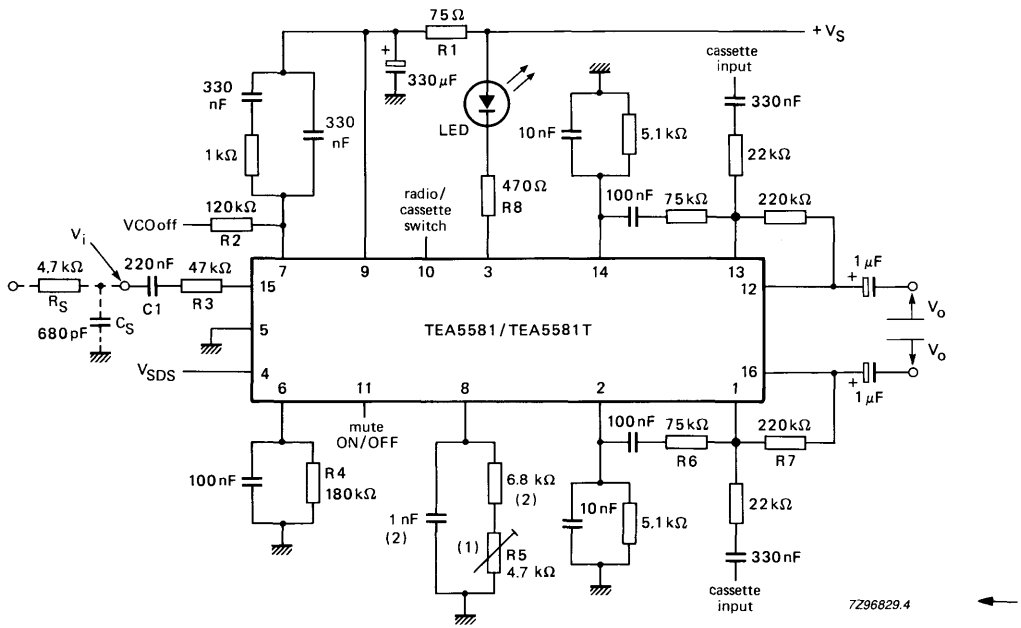


Fig. 6 Channel separation against V_{SDS}.

APPLICATION INFORMATION



(1) 25% tolerance (all other resistors have a 5% tolerance).
(2) 1% tolerance (NP0).

Fig. 7 Application diagram.

AM/FM RADIO RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TEA5591 is an integrated radio circuit which is designed for use in portable receivers and clock radios. The IC is also applicable to mains-fed AM and AM/FM receivers and car radio-receivers. The main advantage of this IC is its ability to operate over a wide range of supply voltages without loss of performance. The AM circuit incorporates a balanced mixer and a 'one-pin' oscillator, which operates in the 0.6 MHz to 30 MHz frequency range, with amplitude control. The circuit also includes an IF amplifier, a detector and an AGC circuit which controls the IF amplifier and the mixer. The FM circuit incorporates an RF amplifier, a balanced mixer and a 'one-pin' oscillator together with two AC coupled IF amplifiers (with distributed selectivity), a quadrature demodulator for the ceramic filter and internal AFC.

Features

- DC AM/FM switch facility
- Three internal separate stabilizers to enable operation over a wide range of supply voltages (1.8 to 15 V)
- All pins (except pin 9) are ESD protected

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 8)		V_P	1.8	3.0	15	V
Supply current						
AM part		$I_{P(AM)}$	–	14	19	mA
FM part		$I_{P(FM)}$	–	17	23	mA
Operating ambient temperature range		T_{amb}	−15	–	+60	°C
AM performance (pin 13)	m = 0.3					
RF sensitivity						
RF input voltage	V_o = 10 mV	V_i	–	3.5	–	μV
RF input voltage	(S+N)/N = 26 dB	V_i	–	17	–	μV
Signal plus noise-to-noise ratio	V_i = 1 mV	(S+N)/N	–	48	–	dB
AF output voltage		V_o	–	50	–	mV
Total harmonic distortion		THD	–	0.7	–	%
FM performance (pin 1)	Δf = 22.5 kHz					
RF sensitivity						
RF input voltage						
−3 dB before limiting		V_i	–	2.3	4.0	μV
Signal plus noise-to-noise ratio for:						
RF input signal voltage (V_i)	V_i = 3.0 μV	(S+N)/N	23	26	–	dB
	V_i = 1 mV	(S+N)/N	–	60	–	dB
AF output voltage	V_i = 100 μV	V_o	75	90	–	mV
Total harmonic distortion		THD	–	0.8	–	%

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

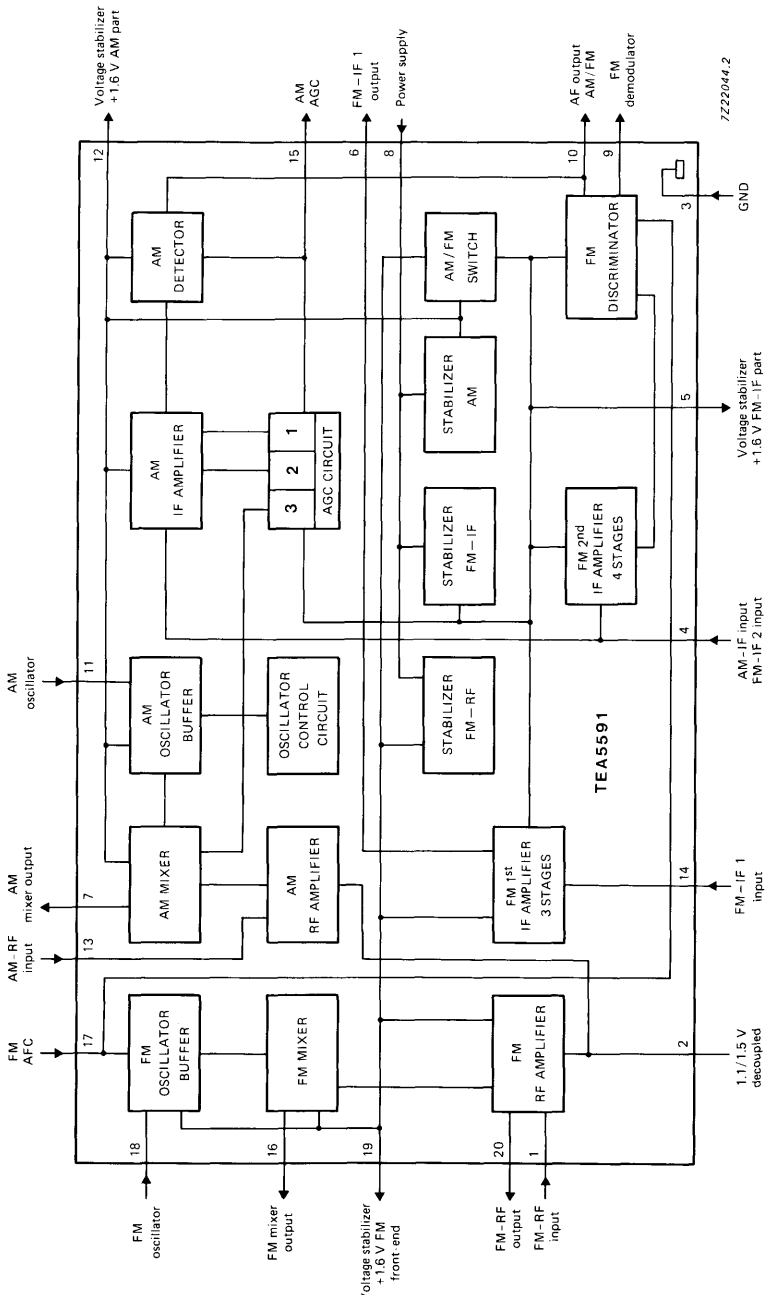


Fig.1 Block diagram.

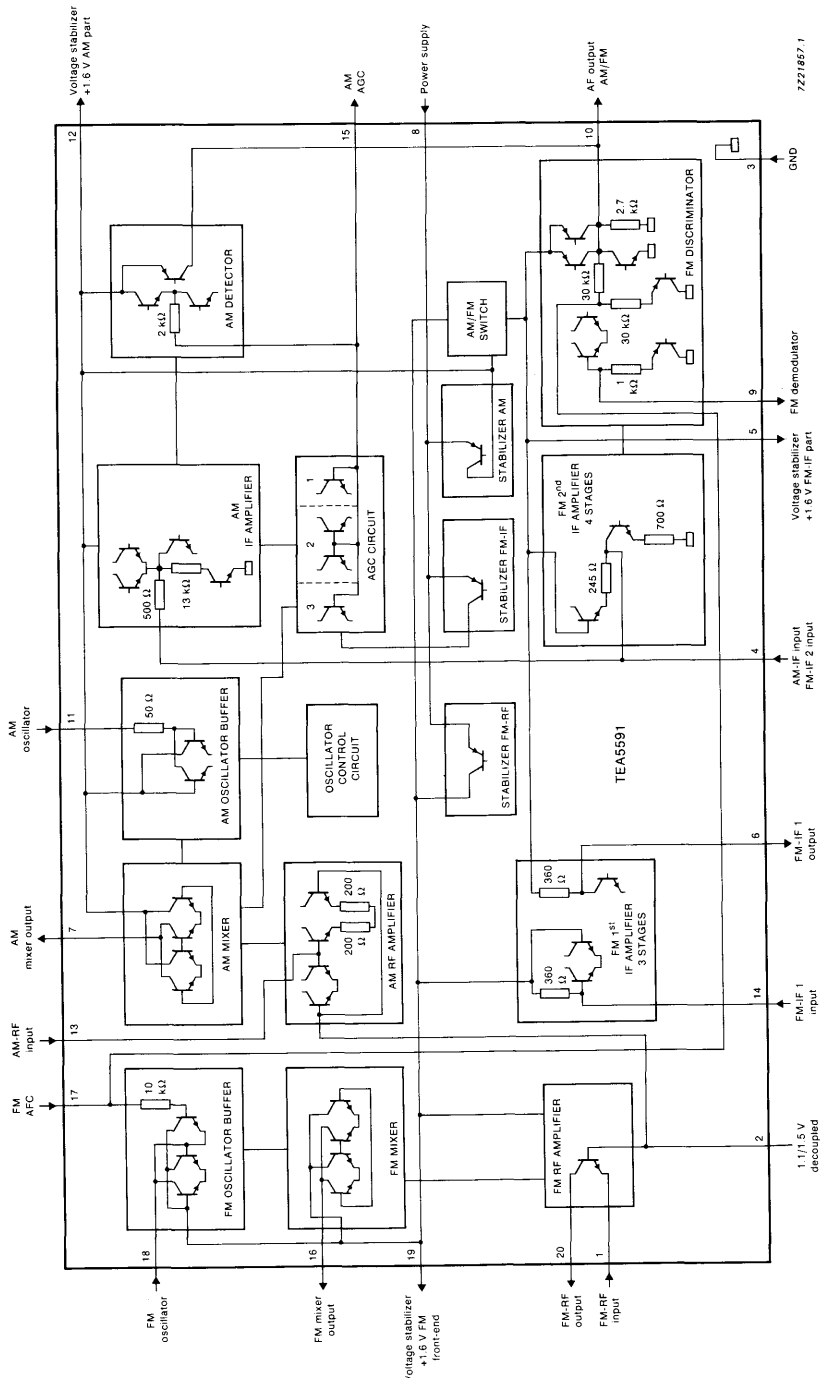


Fig.2 Equivalent circuit diagram.

PINNING

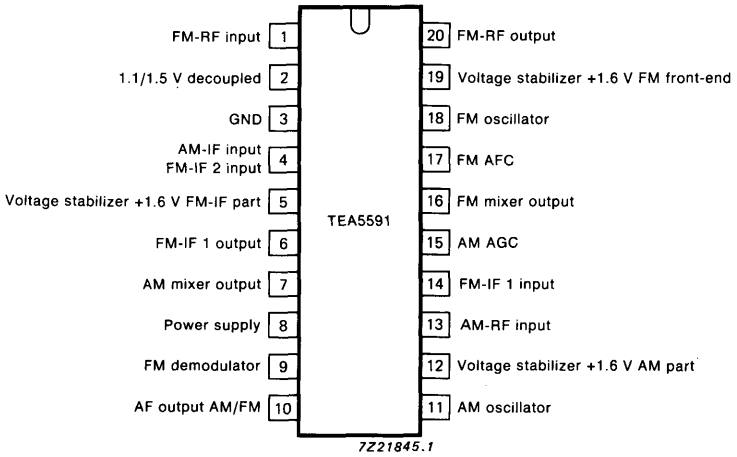


Fig.3 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 8)		V_P	–	18	V
Storage temperature range		T_{stg}	–65	+ 150	°C
Operating ambient temperature range		T_{amb}	–15	+ 60	°C
Total power dissipation		P_{tot}	see Fig.4		

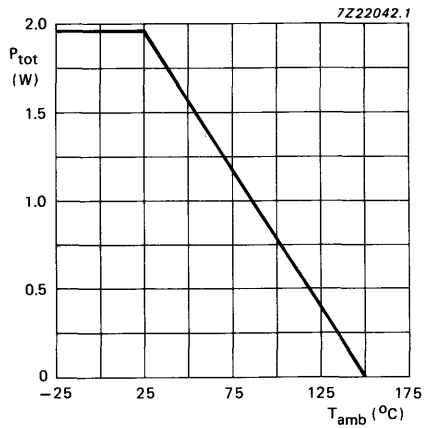


Fig.4 Power derating curve.

DC CHARACTERISTICS

All voltages are referenced to pin 3; all input currents are positive; all parameters are measured in Fig.5 at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	1.8	3.0	15	V
Voltages (FM)						
pin 1		V_1	–	0.90	–	V
pin 2		V_2	–	1.60	–	V
pin 4		V_4	–	0.85	–	V
pin 5		V_5	1.5	1.60	1.75	V
pin 6		V_6	–	1.48	–	V
pin 9		V_9	–	1.05	–	V
pin 14		V_{14}	–	1.63	–	V
pin 17		V_{17}	–	0.60	–	V
pin 19		V_{19}	–	1.60	–	V
Voltages (AM)						
pin 2		V_2	–	1.10	–	V
pin 12		V_{12}	–	1.60	–	V
pin 15		V_{15}	–	1.54	–	V
Supply current						
AM part		$I_{P(AM)}$	–	14	19	mA
FM part		$I_{P(FM)}$	–	17	23	mA

AC CHARACTERISTICS

V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
AM PART						
Input conductance pin 4	f = 0.5 MHz	g_{ie}	–	1.7	–	ms
Input capacitance pin 4	f = 0.5 MHz	C_{ie}	–	5	–	pF
Input conductance pin 13	f = 1.0 MHz	g_{ie}	–	230	–	μs
Input capacitance pin 13	f = 1.0 MHz	C_{ie}	–	13	–	pF
Output conductance pin 7	f = 0.5 MHz	g_{oe}	–	4	–	μs
Output capacitance pin 7	f = 0.5 MHz	C_{oe}	–	4.7	–	pF
Conductance pin 11	f = 1.5 MHz	g_e	–	−6.8	–	ms
Capacitance pin 11	f = 1.5 MHz	C_e	–	25	–	pF
FM PART						
Input conductance pin 4	f = 10.7 MHz	g_{ie}	–	2.7	–	ms
Input capacitance pin 4	f = 10.7 MHz	C_{ie}	–	6	–	pF
Input conductance pin 14	f = 10.7 MHz	g_{ie}	–	2.8	–	ms
Input capacitance pin 14	f = 10.7 MHz	C_{ie}	–	2.5	–	pF
Output conductance pin 6	f = 10.7 MHz	g_{oe}	–	2.8	–	ms
Output capacitance pin 6	f = 10.7 MHz	C_{oe}	–	3.0	–	pF
Output conductance pin 16	f = 10.7 MHz	g_{oe}	–	1.6	–	μs
Output capacitance pin 16	f = 10.7 MHz	C_{oe}	–	4.5	–	pF
Conductance pin 9	f = 10.7 MHz	g_e	–	880	–	μs
Capacitance pin 9	f = 10.7 MHz	C_e	–	3.6	–	pF
Conductance pin 18	f = 100 MHz	g_e	–	−4	–	ms
Capacitance pin 18	f = 100 MHz	C_e	–	10	–	pF

AC CHARACTERISTICS

All parameters are measured in Fig.5 at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified.
RF conditions: Input frequency 1 MHz; 30% modulation where f_{mod} = 1 kHz; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
AM PERFORMANCE						
RF sensitivity						
AF output voltage for: V_i = 7.5 μV	no AGC	V_o	16	30	40	mV
Noise						
Signal plus noise-to-noise ratio for:						
RF input signal voltage of V_i = 17 μV		(S + N)/N	23	26	–	dB
V_i = 1 mV		(S + N)/N	–	48	–	dB
Optimum source impedance		Z_S	–	1.8	–	kΩ
Noise factor	optimum noise impedance	NF	–	4	–	dB
AGC						
Change in RF input voltage for 10 dB change in output voltage	V_{i1} = 100 mV	V_{i1}/V_{i2}	80	86	–	dB
AF output voltage	V_i = 100 μV	V_o	40	50	60	mV
Total harmonic distortion	V_i = 100 μV to 10 mV	THD	–	0.7	1.5	%
	V_i = 100 μV to 10 mV; m = 0.8	THD	–	3	5	%
	V_i = 80 mV; m = 0.8	THD	–	–	8	%

Transimpedance (Z_{tr}) = v_4/i_7 = 900Ω.

parameter	conditions	symbol	min.	typ.	max.	unit
IF suppression (note 1)	V_o = 30 mV	α	–	20	–	dB
Oscillator (pin 11)						
Input voltage	f_{osc} = 1.5 MHz	V_{osc}	–	150	190	mV
	f_{osc} = 30.5 MHz	V_{osc}	–	150	–	mV
	V_P = 1.5 V	V_{osc}	100	–	–	mV
Temperature behaviour	−15 to + 60 °C (only the IC)					
Sensitivity		ΔV_i	–	−2	–	dB
Output voltage	V_i = 1 mV	ΔV_o	–	1	–	dB
Oscillator frequency						
LW		Δf_{osc}	–	500	–	Hz
MW		Δf_{osc}	–	300	–	Hz
SW		Δf_{osc}	–	100	–	kHz
Supply voltage behaviour	V_P = 1.8 to 15 V					
Sensitivity		ΔV_i	–	0	–	dB
Output voltage	V_i = 1 mV	ΔV_o	–	0.5	–	dB
Oscillator frequency						
LW		Δf_{osc}	–	6	–	kHz
MW		Δf_{osc}	–	0.1	–	kHz
SW		Δf_{osc}	–	30	–	kHz

AC CHARACTERISTICS

All parameters are measured in Fig.5 at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

RF conditions: Input frequency 100 MHz; frequency deviation f = ± 22,5 kHz and f_{mod} = 1 kHz

parameter	conditions	symbol	min.	typ.	max.	unit
FM PERFORMANCE						
RF sensitivity						
RF input voltage	−3 dB before limiting	V_{iFM}	–	2.3	4.0	μV
Noise						
Signal plus noise-to-noise ratio for:						
RF input signal voltage (V_i)						
V_i = 3.0 μV		(S + N)/N	23	26	–	dB
V_i = 1 mV		(S + N)/N	–	60	–	dB
Optimum source impedance		Z_{source}	–	50	–	Ω
Noise factor	optimum source impedance	NF	–	6	–	dB
AF output voltage	V_i = 100 μV	V_o	75	90	–	mV
Total harmonic distortion	V_i = 30 μV to 50 mV	THD	–	0.8	–	%
	V_i = 1 mV; Δf = 75 kHz	THD	–	3	–	%
	V_i = 100 mV; Δf = 75 kHz	THD	–	3	–	%
AM suppression	note 2					
RF input signal	V_i = 100 μV to 10 mV	AMS	–	50	–	dB
Oscillator voltage (pin 18)	f_{osc} = 100 MHz	V_{osc}	–	220	–	mV
	V_P = 1.5 V	V_{osc}	100	–	–	mV
IF rejection ratio		IF_{rr}	–	60	–	dB
AFC	f_{osc} = 111.2 MHz					
	V_{17} = 1.4 V	Δf	–	−620	–	kHz
	V_{17} = 0.2 V	Δf	–	+420	–	kHz

parameter	conditions	symbol	min.	typ.	max.	unit
Temperature behaviour	−15 to +60 °C (only the IC)					
RF sensitivity	−3 dB limiting	ΔV_i	–	−6	–	dB
Output voltage	V_i = 100 μV	ΔV_o	–	−2	–	dB
Oscillator frequency		Δf_{osc}	–	−0.3	–	%
Supply voltage behaviour	V_P = 1.8 to 15 V					
RF sensitivity	−3 dB limiting	ΔV_i	–	6	–	dB
Output voltage	V_i = 100 μV	ΔV_o	–	0.5	–	dB
Oscillator frequency		Δf_{osc}	–	100	–	kHz
Oscillator voltage		ΔV_{osc}	–	1.0	–	dB

Notes to the AC characteristics

1. $\alpha = \dfrac{V_i \text{ at } f_i = 455 \text{ kHz}}{V_i \text{ at } f_i = 1 \text{ MHz}}$.
2. AM suppression is measured at f_{mod} = 400 Hz, m = 0.3 for AM; f_{mod} = 1 kHz, Δf = 75 kHz for FM.

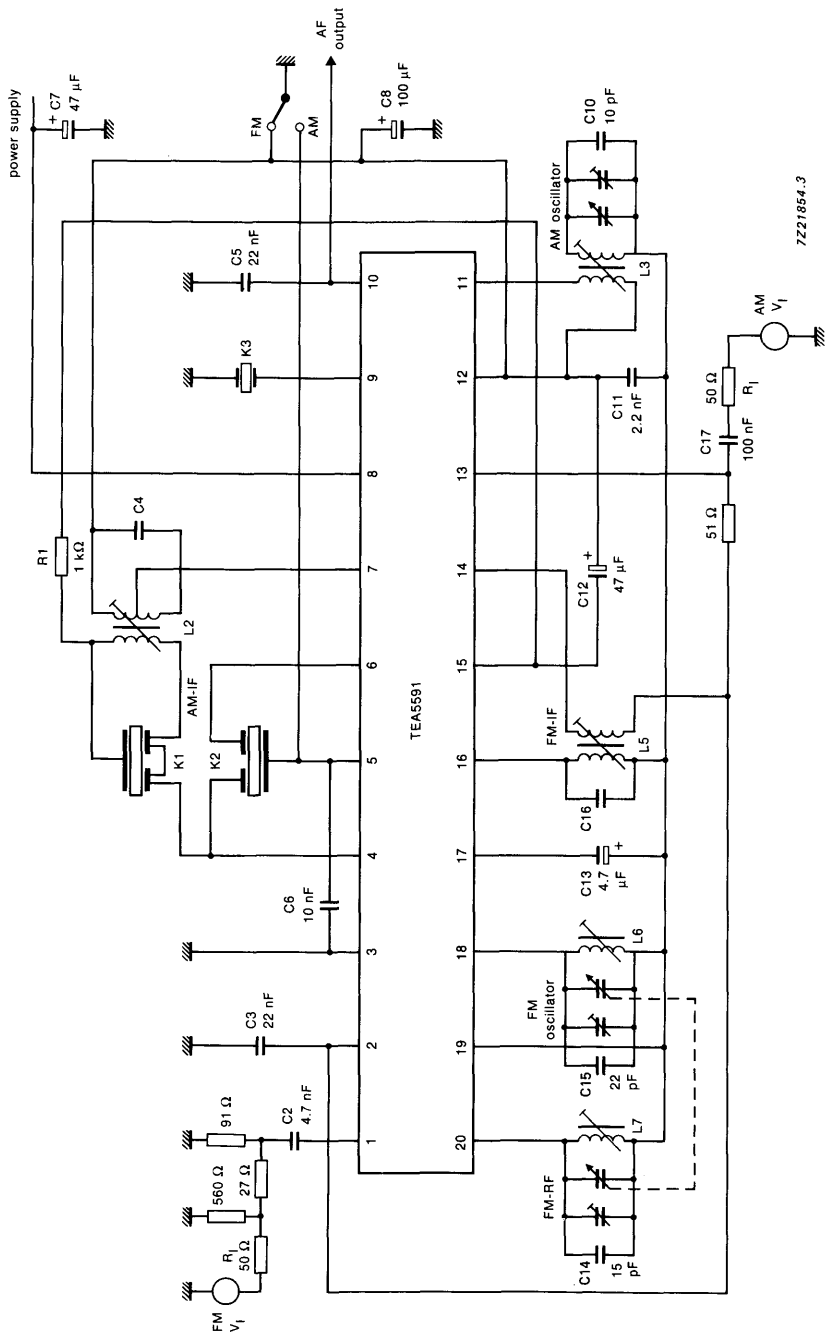


Fig.5 Test circuit.

APPLICATION INFORMATION

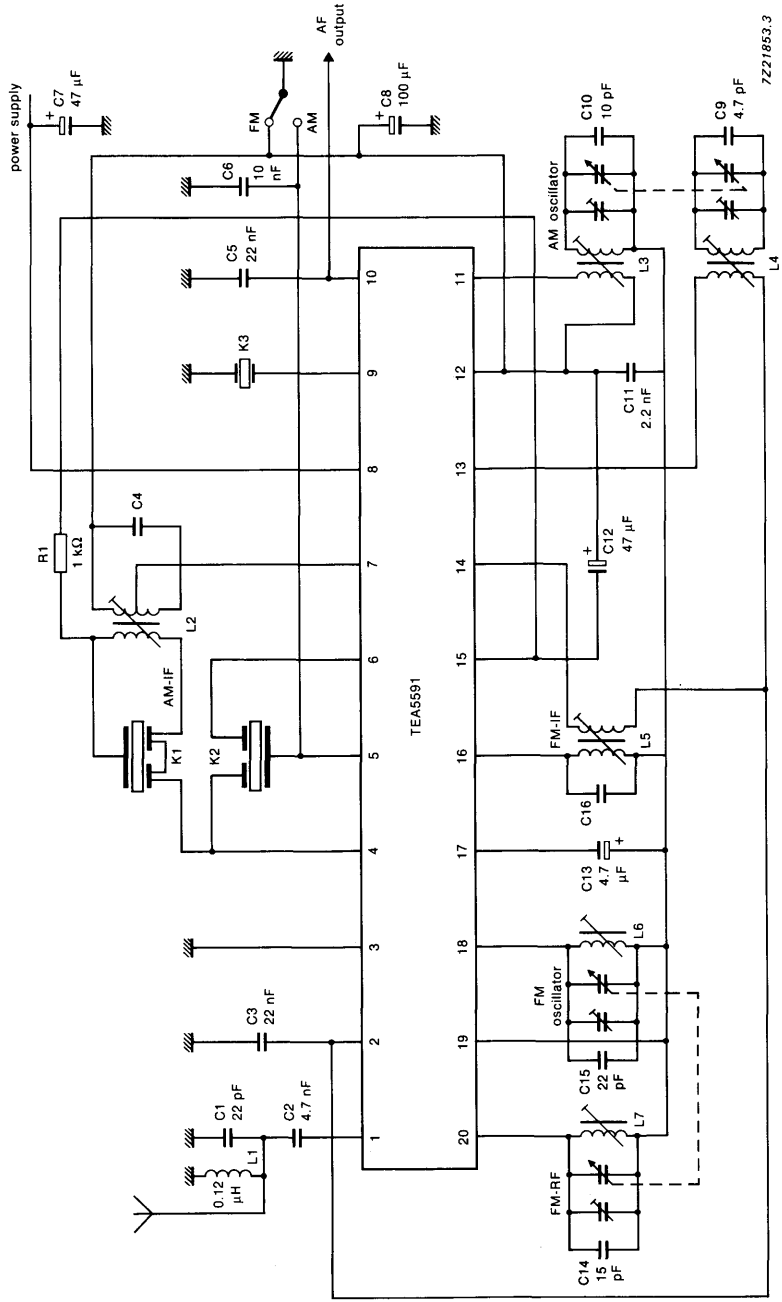
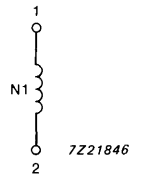


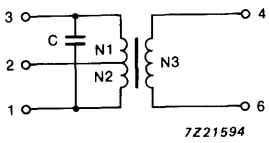
Fig.6 Application diagram.

Component data



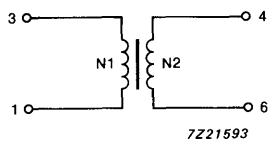
N1 = 4.5
L = 0.12 μH
Wire = 0.8 mm diameter
diameter = 4.5 mm

Fig.7 FM BFP coil (L1).



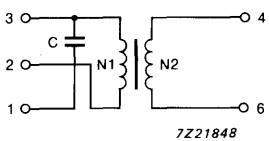
N1 = 132
N2 = 14
N3 = 9
C = 180 pF (internal)
Lprim = 660 μH
fo = 468 kHz
Wire = 0.07 mm diameter
Coil type 7P-TOKO
Material 7MCS

Fig.8 AM IF coil (L2). TOKO sample no. 7MCS-7P.



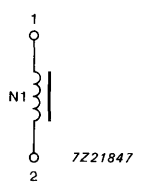
N1 = 86
N2 = 11
Lprim = 270 μH
Wire = 0.07 mm diameter
Coil type 7P-TOKO
Material 7BRS

Fig.9 Oscillator coil (L3). TOKO sample no. 7BRS-7P.



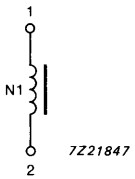
N1 = 11
N2 = 2
C = 85 pF (internal)
fo = 10.7 MHz

Fig.10 FM IF coil (L5). TOKO equivalent no. 119ACS-30120M.



N1 = 1.5
L = 0.03 μH

Fig.11 Oscillator coil (L6). TOKO equivalent no. 301SN-0100.



N1 = 2.5
L = 0.05 μH

Fig. 12 FM RF coil (L7). TOKO equivalent no. 301SN-0200.

Ferroceptor coil

L4: N1 = 105; N2 = 10; L = 625 μH

Ceramic Filters

AM IF (K1). SFZ468 HL.
FM IF (K2). SFE10 . 7 MS2.
FM detector (K3). CDA10 . 7 MC1.

Tuning capacitors

AM 140/82 pF
FM 2 x 20 pF

APPLICATION INFORMATION (continued)

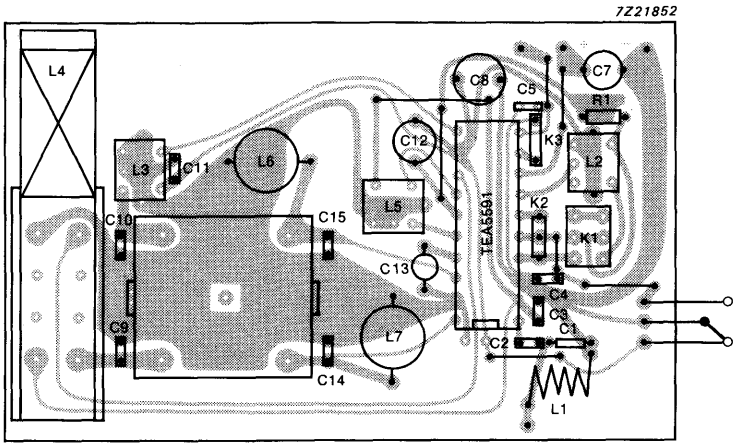


Fig.13 Printed-circuit board component side, showing component layout. For circuit diagram see Fig.6.

Physical dimensions of the printed circuit board = 5.0 x 8.1 cm.

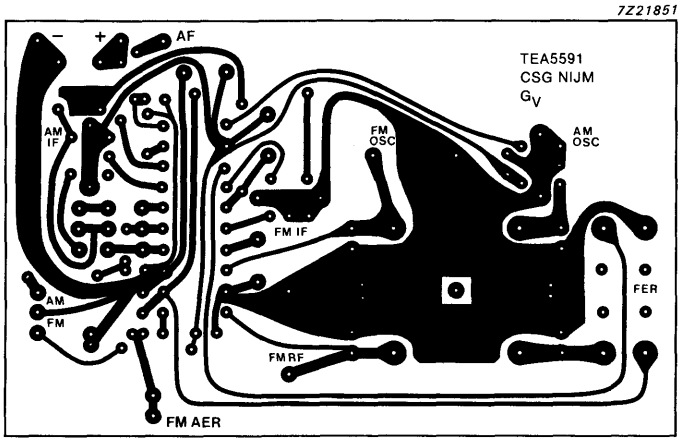


Fig.14 Printed-circuit board showing track side.

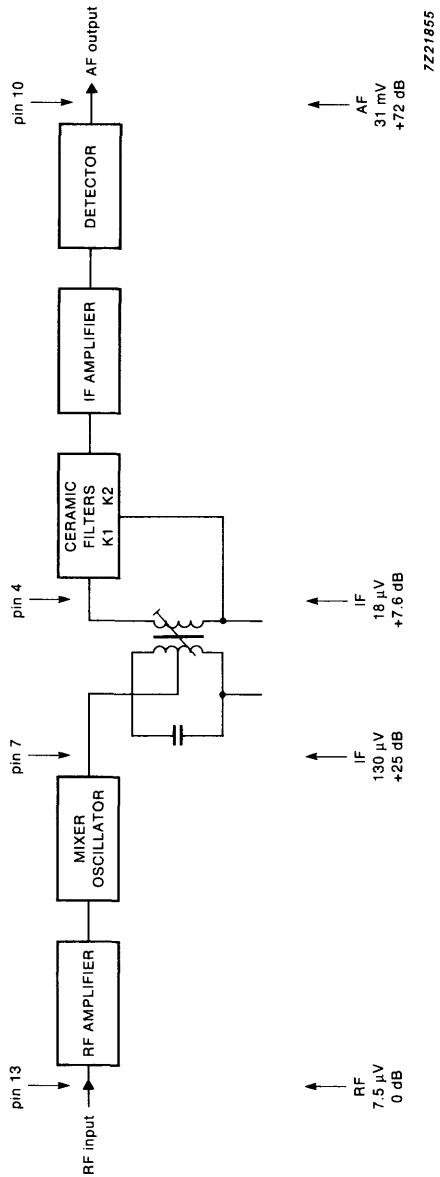


Fig.15 AM signal levels.

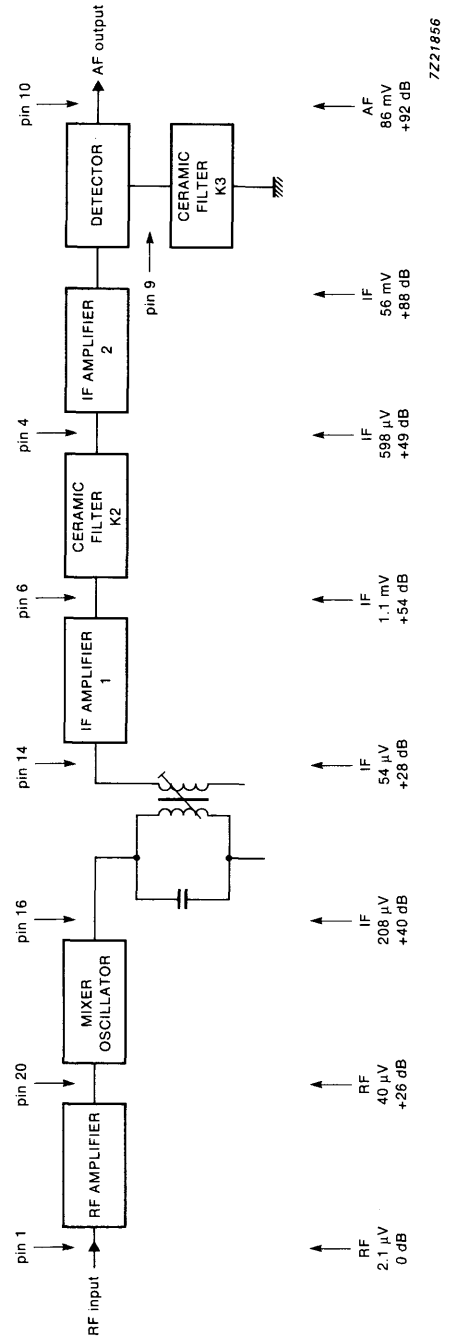


Fig.16 FM signal levels.

APPLICATION INFORMATION (continued)

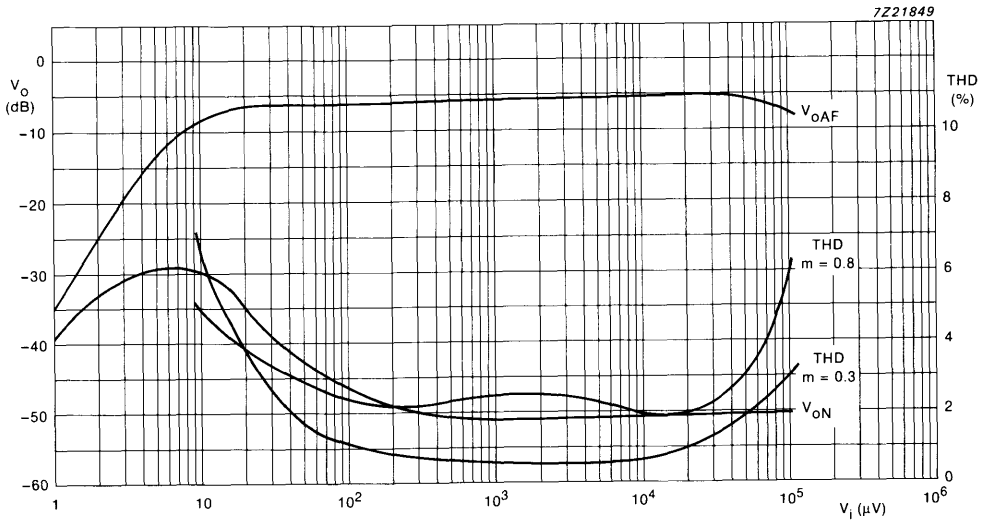


Fig.17 Signal and noise (V_{oAF}), noise (V_{oN}); reference level 0 dB = 100 mV, and total harmonic distortion (THD) as a function of input voltage (V_i) at pin 13. Measured in test circuit Fig.5. AM AGC is measured at f_i = 1 MHz; f_{mod} = 1 kHz; m = 0.3. AM distortion is measured at f_i = 1 MHz; f_{mod} = 1 kHz.

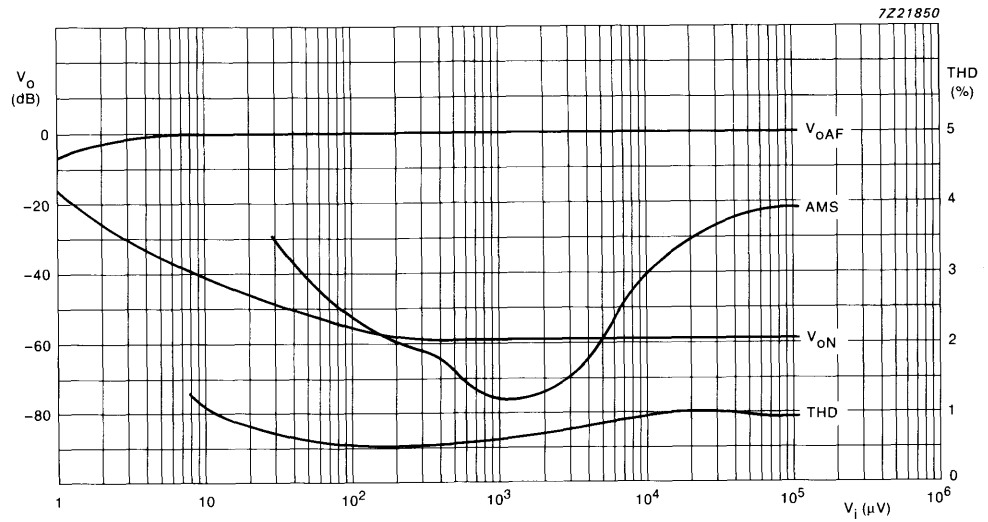


Fig.18 Signal and noise (V_{oAF}), noise (V_{oN}); reference level 0 dB = 100 mV; AM suppression (AMS) and total harmonic distortion (THD) as a function of input voltage (V) at pin 1. Measured in test circuit Fig.5 at f_i = 98 MHz; f_{mod} = 1 kHz; Δf 22.5 kHz. AM suppression is measured at f_{mod} = 400 Hz, m = 0.3 for AM; f_{mod} = 1 kHz, Δf = 75 kHz for FM.

FM/IF SYSTEM AND MICROCOMPUTER-BASED TUNING INTERFACE

GENERAL DESCRIPTION

The TEA6100 is a FM/IF system circuit intended for microcomputer controlled radio receivers. The circuit includes highly sensitive analogue circuitry. The digital circuitry, including an I²C bus, controls the analogue circuitry and the AM/FM tuning and stop information for the microcomputer.

Features

- 4-stage symmetrical IF limiting amplifier
- Software selectable AM or FM input
- Symmetrical quadrature demodulator
- Single-ended LF output stage
- D.C. output level determined by the input signal
- Semi-adjustable AM and FM level voltage
- Multi-path detector/rectifier/amplifier circuitry
- 3-bit level information and 3-bit multi-path information
- Signal dependent 'soft' muting circuit; externally adjustable
- Reference voltage output (FM mode only)
- 8-bit AM/FM frequency counter with selectable counter resolution
- Possibility to measure the AM IF frequency at 460 kHz (250 Hz resolution) and 10,7 MHz (500 Hz resolution)
- Reference frequency can be directly connected to the reference frequency output of a frequency synthesizer (TSA6057, 40 kHz)

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{P1}, V_{P2}	–	8,5	–	V
Supply current		$I_{P1} + I_{P2}$	–	35	–	mA
FM/IF sensitivity	–3 dB before limiting	V_i	–	15	–	μV
Signal plus noise to noise ratio	Δf = 75 kHz; V_I = 10 mV	(S + N)/N	–	85	–	dB
Audio output voltage after limiting	Δf = 22,5 kHz	V_o	–	200	–	mV
AM suppression	V_{IFM} = 600 μV to 600 mV; m = 0,3	AMS	–	60	–	dB
Frequency counter sensitivity						
AM	pin 19, f = 10,7 MHz	$V_{i(AM)}$	–	45	–	μV
	f = 460 kHz	$V_{i(AM)}$	–	20	–	μV
FM	pin 18, f = 10,7 MHz	$V_{i(FM)}$	–	45	–	μV
Resolution of the frequency counter	reference frequency of 40 kHz;					
AM	IF = 460 kHz	f_s (AM)	–	250	–	Hz
	IF = 10,7 MHz	f_s (AM)	–	500	–	Hz
FM		f_s (FM)	–	6,4	–	kHz

DEVELOPMENT DATA

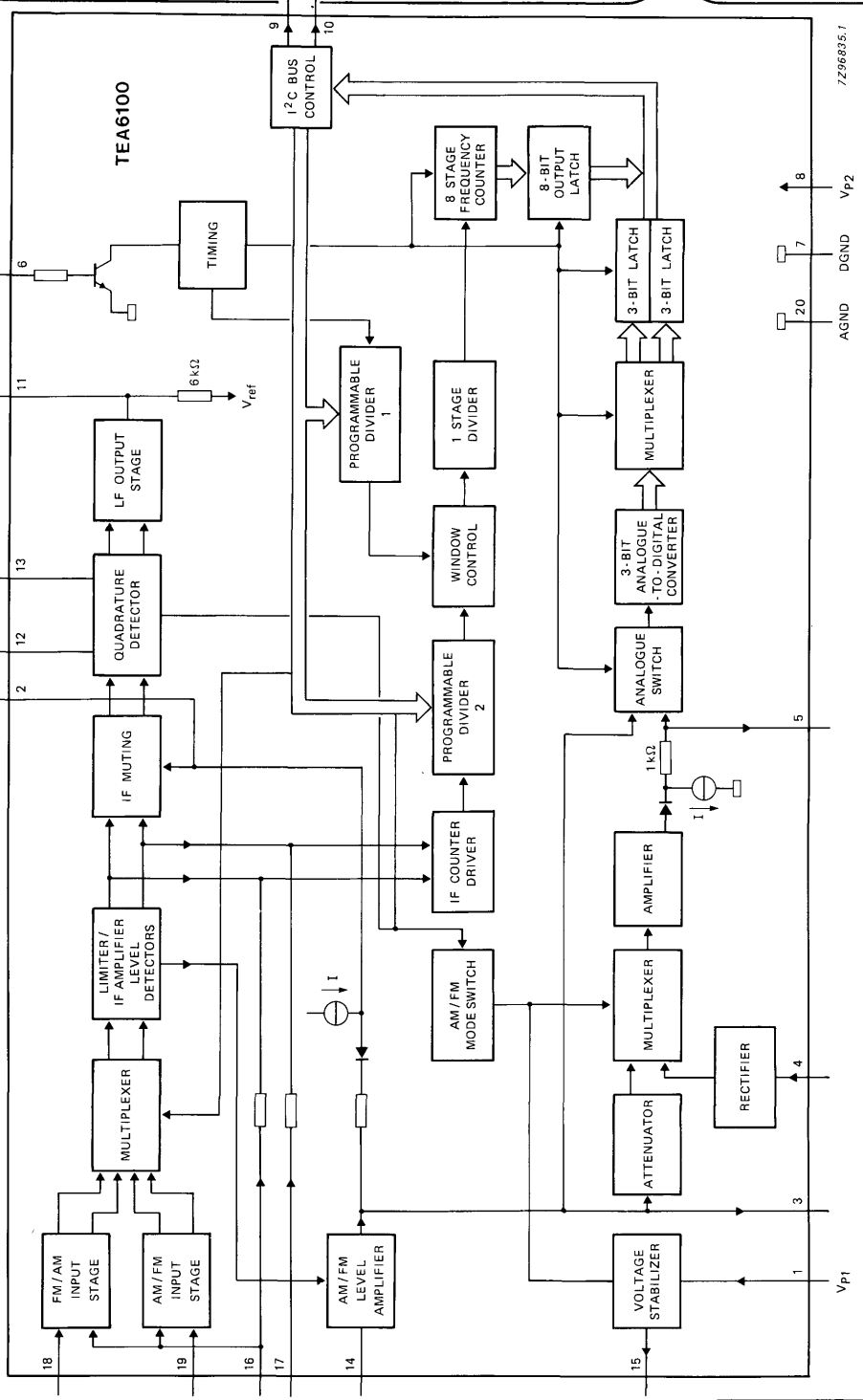


Fig. 1 Block diagram.

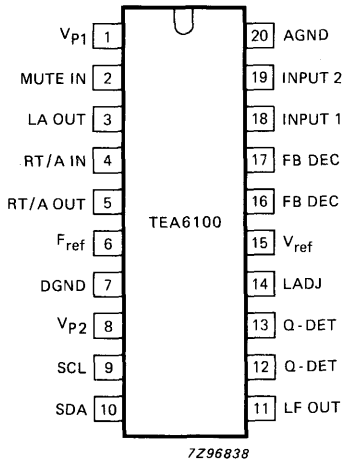


Fig. 2 Pinning diagram.

PINNING

1	V_{P1}	analogue supply voltage
2	MUTE IN	mute input
3	LA OUT	level amplifier output
4	RT/A IN	rectifier/amplifier input
5	RT/A OUT	rectifier/amplifier output
6	F_{ref}	reference frequency input
7	DGND	digital ground
8	V_{P2}	digital supply voltage
9	SCL	serial clock line | I^2C bus
10	SDA	serial data line | I^2C bus
11	LF OUT	audio output signal
12	Q-DET	phase shift for quadrature detector
13	Q-DET	phase shift for quadrature detector
14	LADJ	level amplifier adjustment
15	V_{ref}	reference voltage
16	FB DEC	decoupled feedback
17	FB DEC	decoupled feedback
18	INPUT 1	FM/AM IF input
19	INPUT 2	AM/FM IF input
20	AGND	analogue ground

FUNCTIONAL DESCRIPTION (see Figs 1 and 13)

The IF amplifier consists of four balanced limiting amplifier stages, two separate inputs (AM and FM) and one output. Software programming (see Table 2; Figs 4 and 5) allows the input signals (AM/FM) to be inserted on either input (pin 18 or 19). The output drives the frequency counter and via the mute stage, drives the quadrature detector. The output of the quadrature detector is applied to an audio stage (which has a single-ended output). The AM/FM level amplifier, which is driven by 5 IF level detectors, generates a signal dependent d.c. voltage. The level output voltage is used internally to control the mute stage and, if required, the signal can be used externally to control the stereo channel separation and frequency response of a stereo decoder. The signal is also feed to the analogue-to-digital converter (ADC). Due to the front-end spread in the amplification, the level voltage is made adjustable (LADJ, pin 14). The level voltage amplifier controls the mute stage and this insures the –3 dB limiting point remains constant, independent of the front-end spread. AM and FM mode have different front-end circuitry, therefore LADJ must be adjustable for both inputs.

The output voltage of the level amplifier is dependent upon the field strength of the input signal. The multi-path of the FM signal exists in the AM modulation of the input signal. The following method is used to determine the level information and the amount of multi-path (as a DC voltage):

- the IF level detector detects the multi-path and feds the signal, via the level amplifiers, to the external bandpass filter (pin 3) and ADC1
- the signal is then fed to an internal rectifier
- the rectified signal is then fed to an amplifier, so at pin 5 the DC level information is externally available and internally used by ADC2

In the FM mode, the DC information concerning the multi-path is available at pin 5 and the level information is available at pin 3.

In the AM mode, the level information at pin 3 cannot be directly used owing to AM modulation on the output signal of the level amplifier. This signal requires filtering, which is achieved by the following method:

- the multiplexer is switched to a position which causes the signal to be applied to the attenuator
- after attenuation the signal is fed to an amplifier (the resultant gain of attenuator and amplifier is unity), after amplification the signal is filtered by an internal resistor and external capacitor
- after filtering the signal is applied to ADC2 and is externally available

In AM mode pin 5 contains the level information.

The voltages on pin 3 and 5 are converted into two 3-bit digital words by the ADC, which can then be read out by the I^2C bus. The meaning of the 3-bit words is shown in Table 1.

Table 1 3-bit words

	position	
word	FM	AM
1	multipath	level without modulation
2	level	level with modulation

The FM modulated signal is converted into an audio signal by the symmetrical quadrature detector. The main advantage of such a detector is that it requires few external components.

An FM signal requires good AM suppression, and as a result, the IF amplifiers must act as limiters. To achieve good suppression on small input signals the IF amplifiers must have a high gain and thus a high sensitivity. High sensitivity is an undesirable property when used in car radio applications, this problem is solved by having an externally adjustable mute stage to control the overall sensitivity of the device.

The IF mute stage is controlled by the level amplifier (soft muting) and is only active in FM mode. If the input falls below a predetermined level, the mute stage becomes active. To avoid the 'ON/OFF' effect of the audio signal due to fluctuations of the input signal, the mute stage is activated rapidly but de-activated slowly. The mute stage is de-activated slowly, via a current source and an external capacitor at pin 2, to avoid aggressive behaviour of the audio signal. It is possible to adjust the '–3 dB limiting point' of the audio output via the level voltage due to the level signal being externally adjustable. If hard muting is required then pin 2 must be switched to ground.

The 8-bit counter allows accurate stop information to be obtained, because exact tuning is achieved when the measured frequency is equal to the centre frequency of the IF filter.

To measure the input frequency, the number of pulses which occur in a defined time must be counted. This defined time is refered to as 'window'. A wide window indicates a long measuring time and therefore a high accuracy. The counter resolution is defined as Hertz per count. Due to the TEA6100 having to measure the IF frequencies of AM and FM, the counter resolution must be adjustable (different channel spacing). The counter resolution depends on the setting of dividers 1 (N1), divider 2 (N2) and the reference frequency (F_{ref}). The divider ratios of N1 and N2 are controlled by software (see section PROGRAMMING INFORMATION). In Table 3 the window and counter resolution has been calculated for a reference frequency of 40 kHz. The accuracy is controlled by bit 7 of the input word. Although the resolution is the same for bit 7 = logic 0 and bit 7 = logic 1, the width of the window doubles when bit 7 = logic 1.

- bit 7 = 0, accuracy = ± counter resolution
- bit 7 = 1, accuracy = $\pm \frac{1}{2}$ counter resolution

Communication between TEA6100 and the microcomputer is via a two wire bidirectional I^2C bus. The power supply lines are fully isolated to avoid cross talk between the digital and analogue parts of the circuit.

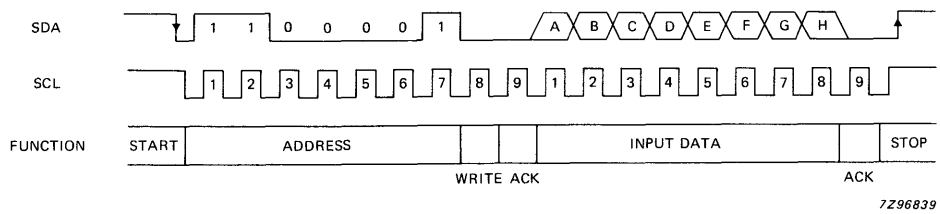


Fig. 3 Input data format waveforms.

Table 2 Input bits

bit	function	logic 0	logic 1	see Figs. 5 and 6
1	reference frequency	32 kHz	40 kHz	A
2	IF mode	AM	FM	B
3	IF input	pin 19	pin 18	C
4	counter input	460 kHz	10,7 MHz	D
5	counter mode	AM	FM	E
6	resolution	divide by 8	divide by 1	F
7	accuracy	LOW	HIGH	G
8	test mode	OFF	ON	H

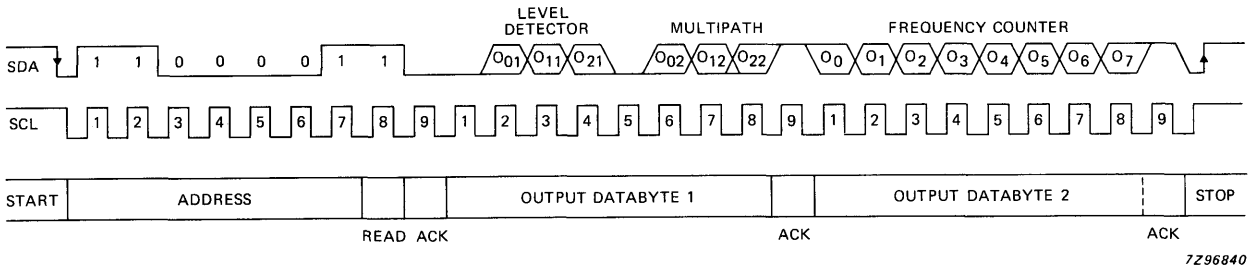


Fig. 4 Output data format waveforms.

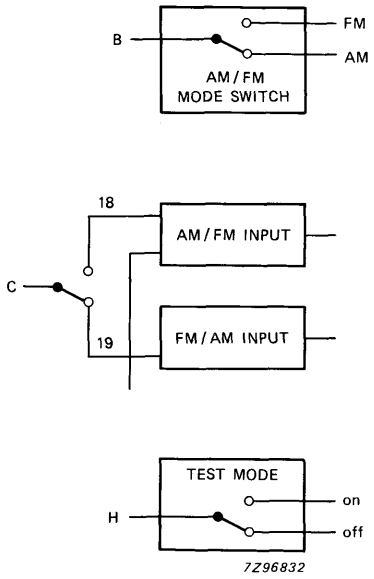


Fig. 5 Switch positions, analogue part (switches drawn in logic 0 state).

DEVELOPMENT DATA

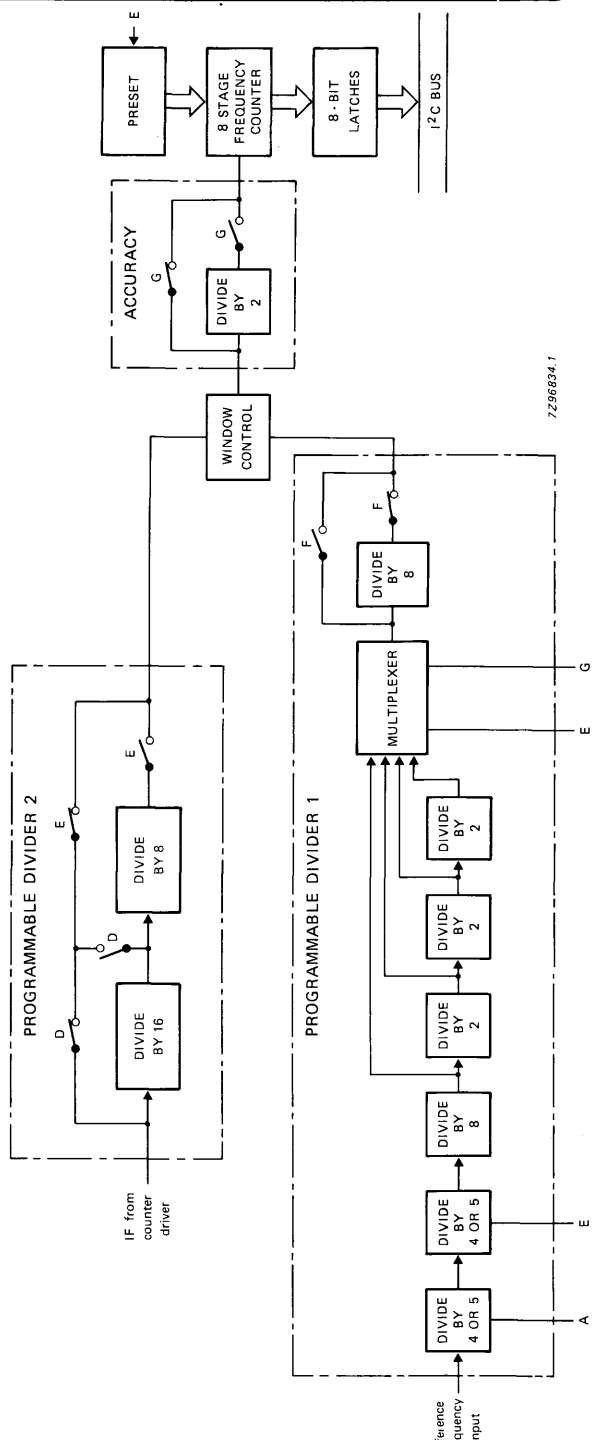


Fig. 6 Switch positions, digital part (switches drawn in logic 0 state, see Tables 2 and 3).

Table 3 Possible window settings and counter resolutions with a 40 kHz reference frequency (see Figs. 5 and 6)

position of switch ADEFG	window (ms)	counter resolution Hz/count	IF frequency (kHz)	read out by IF frequency (hex)	range (kHz)	
					min.	max.
00000	25,6	39,1	460,0	4F	456,914	466,875
10000	32,0	31,3	460,0	CF	453,531	461,500
00001	51,2	39,1	460,0	4F	456,914	466,875
10001	64,0	31,3	460,0	CF	453,531	461,500
00100	128,0	1000,0	460,0	C3	265,000	520,000
10100	160,0	800,0	460,0	36	416,800	620,800
00101	256,0	1000,0	460,0	C3	256,000	520,000
10101	320,0	800,0	460,0	36	416,800	620,800
00010	3,2	312,5	460,0	0F	455,312	535,000
10010	4,0	250,0	460,0	7F	428,250	492,000
00011	6,1	312,5	460,0	0F	455,312	535,000
10011	8,0	250,0	460,0	7F	428,250	492,000
00110	16,0	8000,0	460,0	30	76,000	2116,000
10110	20,0	6400,0	460,0	3F	56,800	1688,800
00111	32,0	8000,0	460,0	30	76,800	2116,000
10111	40,0	6400,0	460,0	3F	56,800	1688,800
01000	25,6	625,0	10700,0	2F	10670,625	10830,000
11000	32,0	500,0	10700,0	E7	10584,500	10712,000
01001	51,2	625,0	10700,0	2F	10670,625	10830,000
11001	64,0	500,0	10700,0	E7	10584,000	10712,000
01100	128,0	1000,0	10700,0	C3	10505,000	10760,000
11100	160,0	800,0	10700,0	36	10656,800	10860,800
01101	256,0	1000,0	10700,0	C3	10505,000	10760,000
11101	320,0	800,0	10700,0	36	10656,800	10860,000
01010	3,2	5000,0	10700,0	AB	9845,000	11120,000
11010	4,0	4000,0	10700,0	C2	9924,000	10944,000
01011	6,4	5000,0	10700,0	AB	9845,000	11120,000
11011	8,0	4000,0	10700,0	C2	9924,000	10944,000
01110	16,0	8000,0	10700,0	30	10316,000	12356,000
11110	20,0	6400,0	10700,0	7F	9887,200	11519,200
01111	32,0	8000,0	10700,0	30	10316,000	12356,000
11111	40,0	6400,0	10700,0	7F	9887,200	11519,200

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pins 1 and 8	V_{P1}, V_{P2}	0	13,2	V
Total power dissipation		P_{tot}	see Fig. 7		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−30	+85	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 70 K/W

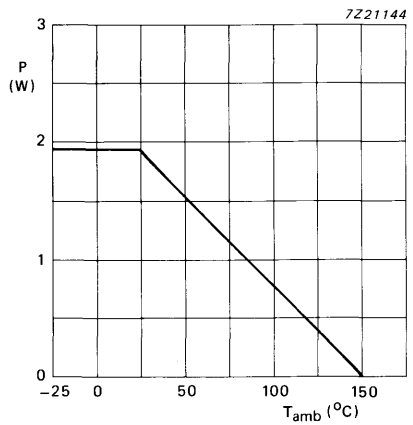


Fig. 7 Power derating curve.

DC CHARACTERISTICS (note)

$V_{P1} = V_{P2} = 8{,}5$ V; $T_{amb} = 25$ °C; all currents positive into the IC; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pins 1 and 8	V_{P1}, V_{P2}	7,5	8,5	12	V
Supply current						
FM mode	$V_{ADJ} > 2{,}4$ V	I_{P1}	–	19	25	mA
AM mode	$V_{ADJ} > 2{,}4$ V	I_{P1}	–	15	25	mA
digital part		I_{P2}	–	16	23	mA
Power dissipation		P_d	–	280	–	mW

DEVELOPMENT DATA

AC CHARACTERISTICS (note 1)

V_P = 8,5 V; $V_{i(FM)}$ = 1 mV; f = 10,7 MHz; Δf = 22,5 kHz; f_m = 1 kHz; FM mode; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
IF amplifier, quadrature detector and LF amplifier output	pin 11					
Sensitivity	−3 dB before limiting; inactive mute	$V_{i(FM)}$	–	15	30	μV
Sensitivity	S/N = 26 dB; inactive mute	$V_{i(FM)}$	–	12	–	μV
Signal plus noise to noise ratio	$V_{i(FM)}$ = 10 mV; bandwith = 0,3 to 15 kHz; Δf = 75 kHz	(S + N)/N	–	85	–	dB
IF input range	AM suppression > 40 dB	$V_{i(FM)}$	–	0,09 to 1000	–	mV
Audio output voltage after limiting	Δf = 22,5 kHz	V_o	160	200	240	mV
Total harmonic distortion for single tuned circuit	Δf = 75 kHz	THD	–	0,65	–	%
AM suppression	note 2; see Fig. 8;					
	$V_{i(AM)}$ range = 200 μV to 600 mV	AMS	–	60	–	dB
	$V_{i(AM)}$ range = 200 μV to 600 μV	AMS	–	55	–	dB
Supply voltage ripple rejection	200 Hz; 20 log (V_i/V_o)	SVRR	38	40	–	dB
IF counter inputs						
Frequency counter sensitivity	minimum input voltage for a readout ± 1 bit;					
FM mode	10,7 MHz	$V_{i(FM)}$	–	–	60	μV
AM mode	10,7 MHz	$V_{i(AM)}$	–	–	60	μV
AM mode	460 kHz	$V_{i(AM)}$	–	–	45	μV
Maximum input voltage		V_i	–	–	1	V

parameter	conditions	symbol	min.	typ.	max.	unit
FM level performance	see Fig. 9					
Output voltage adjustment range	$V_{i(FM)}$ = 0 V; pins 3 and 14	V_{LFM}	–	0,1 to 4,6	–	V
Maximum output voltage	pins 3 and 14	V_{LFM}	V_P–1,5	–	–	V
Adjustable gain	$V_{i(FM)}/V_{ADJ}$	G_{ADJ}	–	–2	–	dB
Level voltage slope	V_{ADJ} = 2,4 V; $V_{i(FM)}$ = 100 to 10 mV	$S_{i(FM)}$	1,4	1,6	1,8	V/dec *
Output impedance of level amplifier	$V_{LFM} > 1$ V	$\|Z_o\|$	–	100	–	Ω
AM level performance	see Fig. 10					
Output voltage adjustment range	$V_{i(AM)}$ = 0 V; pins 5 and 14	V_{LFM}	–	0,1 to 4,6	–	V
	$V_{i(AM)}$ = 10 mV; pins 5 and 14	V_{LAM}	6	–	–	V
Adjustable gain	$V_{i(AM)}/V_{ADJ}$	G_{ADJ}	–	–2	–	dB
Level voltage slope	V_{ADJ} = 2,4 V; $V_{i(FM)}$ = 100 to 10 mV	$S_{i(AM)}$	1,3	1,5	1,7	V/dec *
IF soft muting	V_{LFM}; pin 3; see Fig. 11					
Mute operating range		V_{LFM}	–	0,1 to 2,5	–	V
Mute voltage	–3 dB output attenuation	V_{LFM}	1,20	1,45	1,75	V
Maximum muting	V_{LFM} = 0,1 V	V_{MUTE}	–	19	–	dB
IF hard muting	V_{MUTE}; pin 2					
Mute voltage	–60 dB output attenuation	V_{MUTE}	–	460	–	mV
Mute discharge current	V_{MUTE} = 1 V; V_{LEVEL} = 0 V; mute ON; pin 2	$+I_2$	–	270	–	μA
Mute charging current	V_{MUTE} = 0 V; mute OFF	$-I_2$	–	1,5	–	μA

* V/dec = voltage per decade.

DEVELOPMENT DATA

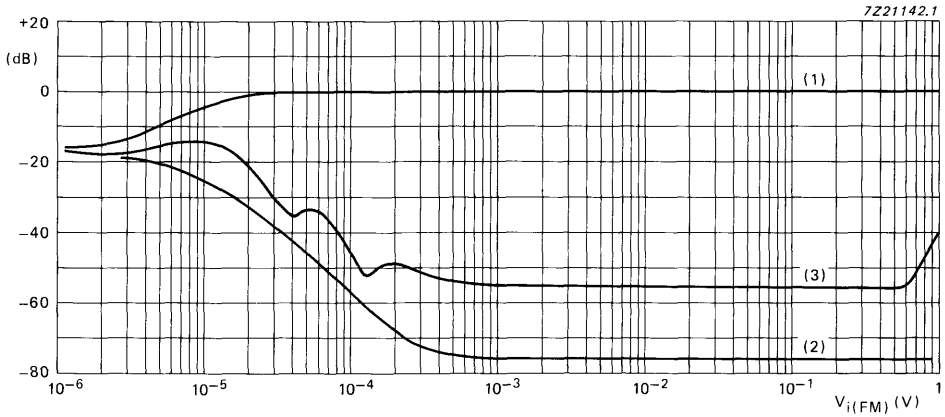
AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Rectifier/amplifier						
Input impedance	pin 4	$\|Z_i\|$	7	10	13	kΩ
Conversion gain AC to DC	pins 4 and 5; bandwith = 100 Hz to 120 kHz; 20 log $V_{O(MP)}$ (d.c.)/ $V_{i(MP)}$ (a.c.)	G_A	–	30	–	dB
DC output voltage range		$V_{O(MP)}$	–	0,2 to 6	–	V
Output characteristics	see Fig. 13; note 3					
Discharge current		I_o	–	200	–	μA
Output ripple in AM mode (peak-to-peak value)	f_m = 200 Hz; m = 0,8; $V_{i(AM)}$ range = 100 μV to 30 mV	V_{ripple}	–	300	400	mV
Multi-path output	see Fig. 12; note 4					
Reference voltage output	pin 15, FM only					
Output voltage		V_{ref}	–	4,4	–	V
Output sink current		$+I_{15}$	–	–	1,5	mA
Output impedance		$\|Z_O\|$	–	–	10	Ω
Output charge current		$-I_{15}$	5	–	–	mA
Output voltage	AM mode	V_{ref}	–	0	–	V
Output impedance	AM mode	$\|Z_O\|$	–	14	–	kΩ
I²C bus data format	see Figs 3 and 4; Table 2					
3-bit ADC	multi-path and level information, note 5					
Trip level LOW		V_{TL}	1,20	1,45	1,75	V
Trip level HIGH		V_{TH}	4,25	4,50	4,75	V
Reference frequency input	pin 6					
Reference range		F_{ref}	–	–	40	kHz
Input voltage LOW		V_{IL}	–	–	0,4	V
Input current HIGH		I_{IH}	5	–	–	μA

Notes to the characteristics

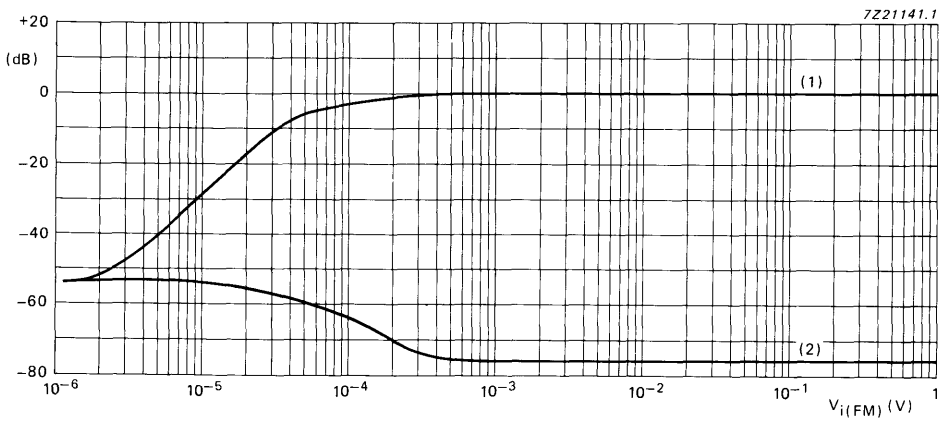
1. All characteristics are measured from the circuit shown in Fig. 13.
2. Conditions for this parameter are:
   20 log $V_{o(FM)}$; m = 0,3 or 20 log $V_{o(AM)}$; m = 0,3.
3. Voltage source followed by diode and resistor.
4. A DC shift can be achieved by connecting a 1,8 MΩ resistor between pin 4 and pin 15.
5. Step size between trip levels:
   $(V_{TH} - V_{TL})/6 \pm 0{,}07$ V.

DEVELOPMENT DATA



(1) Audio (Δf = 22,5 kHz and f_{mod} = 1 kHz) for V_{ADJ} = 0 V.
(2) Noise (with dBA filter) for V_{ADJ} = 0 V.
(3) AM suppression (m = 0,3 and f_{mod} = 1 kHz) for V_{ADJ} = 0 V.

Fig. 8(a) Audio output voltage performance plotted against input signal, $V_{i(FM)}$.



(1) Audio (Δf = 22,5 kHz and f_{mod} = 1 kHz) for V_{ADJ} = 2,4 V.
(2) Noise (with dBA filter) for V_{ADJ} = 2,4 V.

Fig. 8(b) Audio output voltage performance plotted against input signal, $V_{i(FM)}$.

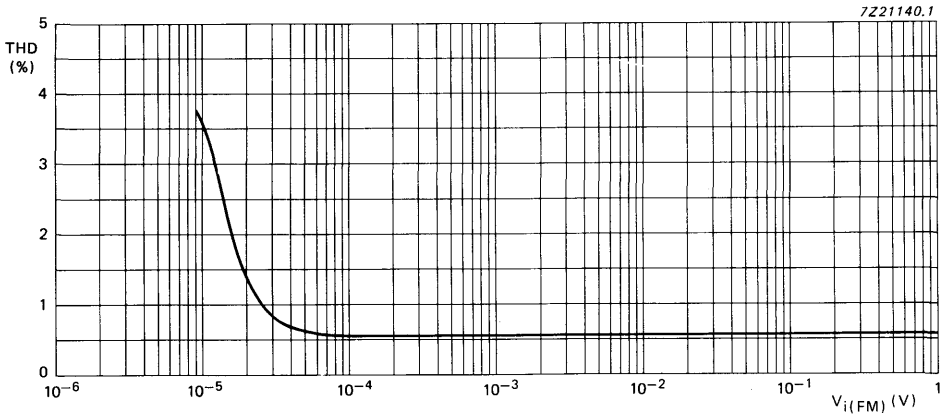
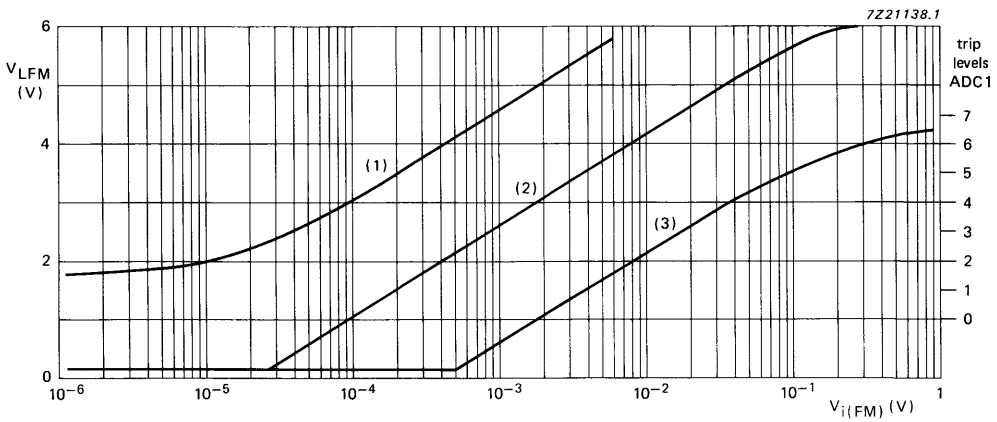
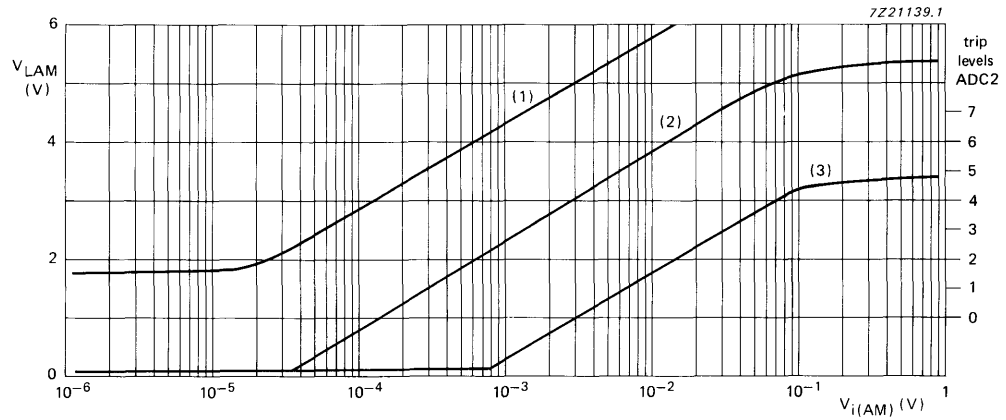


Fig. 8(c) Total harmonic distortion; Δf = 75 kHz, f_{mod} = 1 kHz and V_{ADJ} = 0 V.



(1) V_{ADJ} = 1,4 V.
(2) V_{ADJ} = 2,4 V.
(3) V_{ADJ} = 3,4 V.

Fig. 9 Level voltage output (V_{LFM}) plotted against IF input signal, $V_{i(FM)}$; IF = 10,7 MHz.



(1) V_{ADJ} = 1,4 V.
(2) V_{ADJ} = 2,4 V.
(3) V_{ADJ} = 3,4 V.

Fig. 10 Level voltage output (V_{LAM}) plotted against IF input signal, $V_{i(AM)}$; IF = 10,7 MHz or 460 kHz.

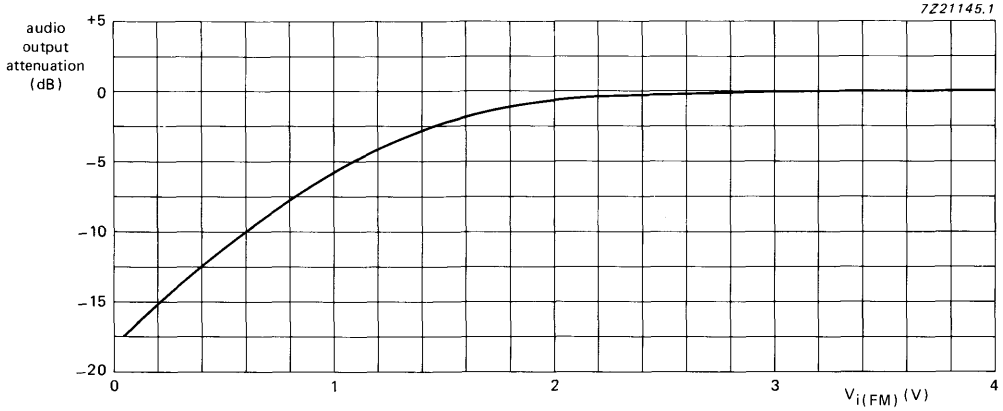
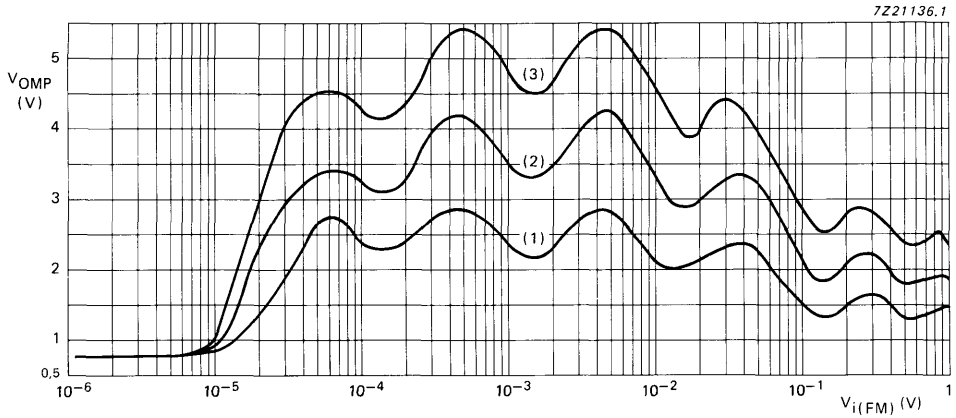


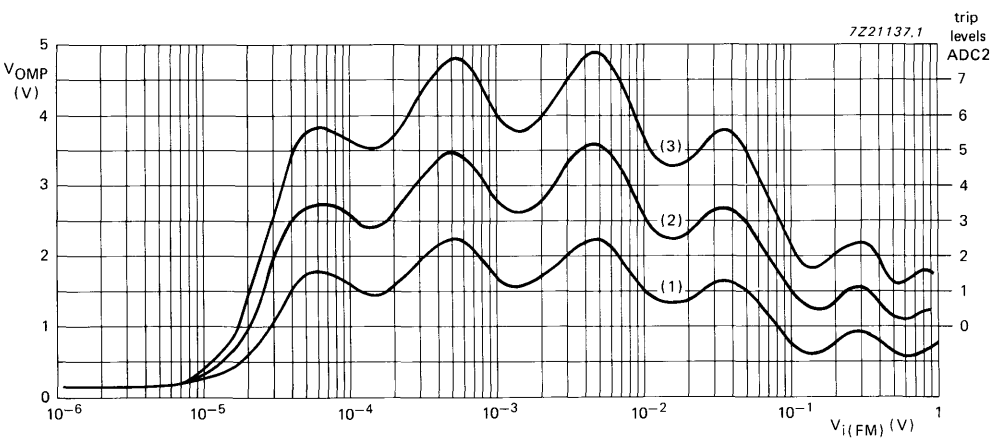
Fig. 11 Soft muting plotted against level output voltage; $V_{i(FM)}$ = 1 mV and Δf = 22,5 kHz.



(1) mod = 0,2
(2) mod = 0,3
(3) mod = 0,4

Fig. 12(a) Multi-path output plotted against IF input signal, $V_{i(FM)}$; f_{mod} = 3 kHz (AM, no FM modulation), V_{ADJ} = 2,4 V and 1,8 MΩ resistor connected between pin 4 and pin 15.

DEVELOPMENT DATA



(1) mod = 0,2
(2) mod = 0,3
(3) mod = 0,4

Fig. 12(b) Multi-path output plotted against IF input signal, $V_{i(FM)}$; f_{mod} = 3 kHz (AM, no FM modulation), V_{ADJ} = 2,4 V.

APPLICATION INFORMATION

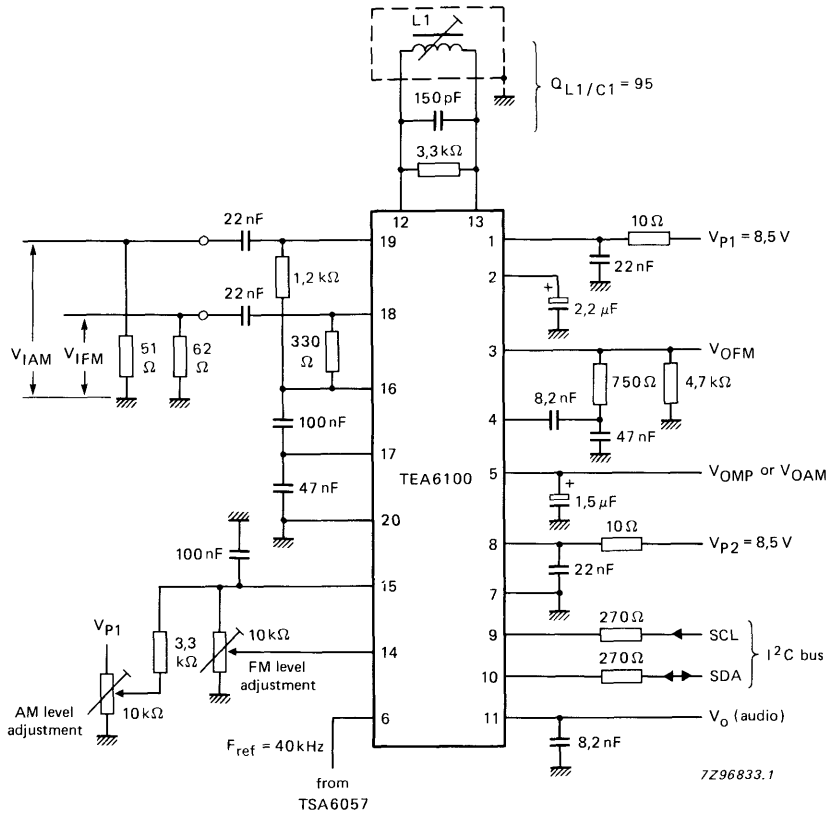


Fig. 13 Application diagram.

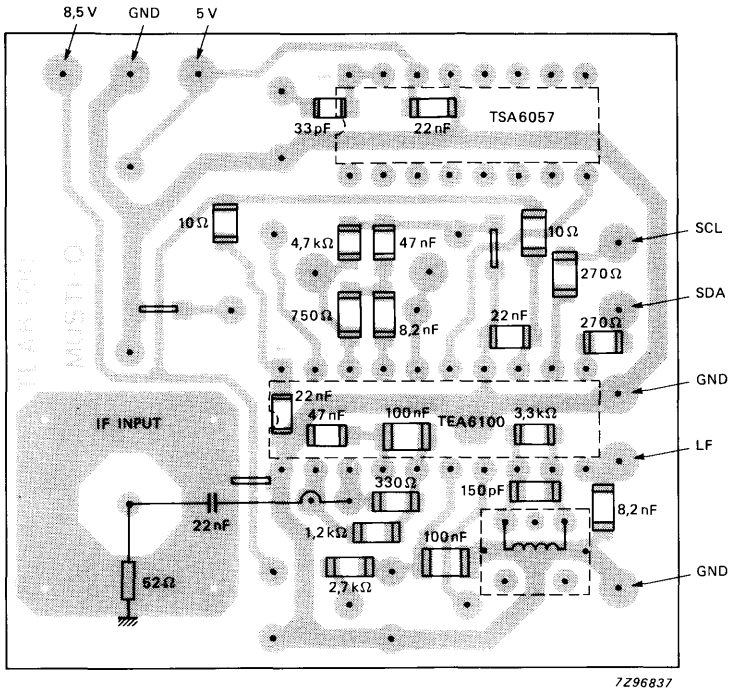


Fig. 14 Track side of printed circuit board.

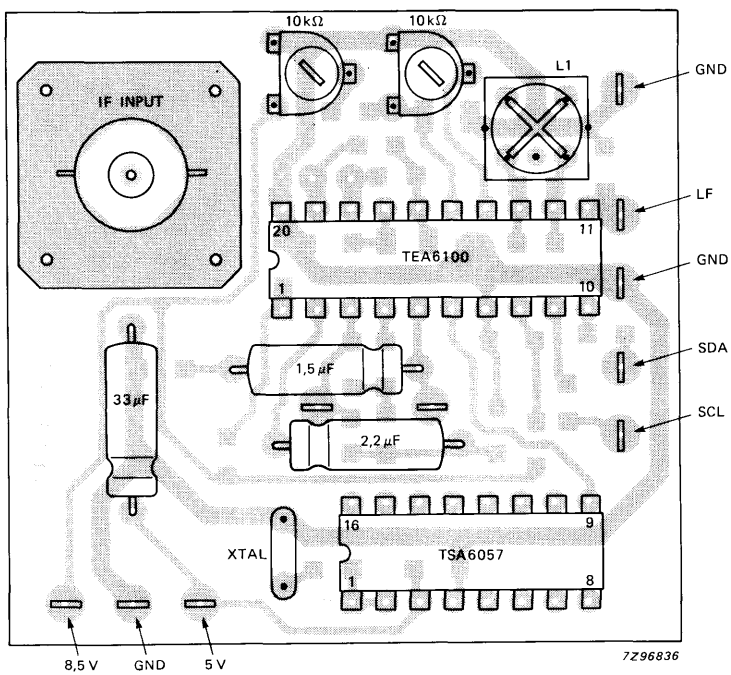
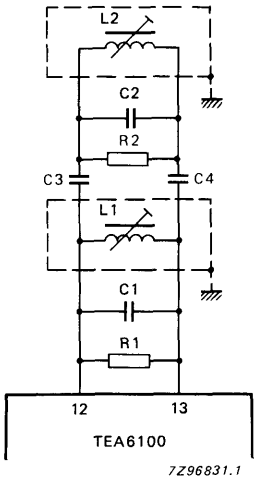


Fig. 15 Component side of printed circuit board.

Double tuned circuit



R1 = 5,1 kΩ, R2 = 1,5 kΩ
C1 = C2 = 150 pF (n = 220)
C3 = C4 = 10 pF
L1 = L2 = 1,6 μH

Fig. 16 Double tuned demodulator circuit.

Alignment of the circuit is obtained with an IF input signal > 200 μV. Tuning the circuit is performed by, detuning L2, adjusting L1 to obtain a minimum distortion level and then adjusting L2 to obtain a minimum distortion level.

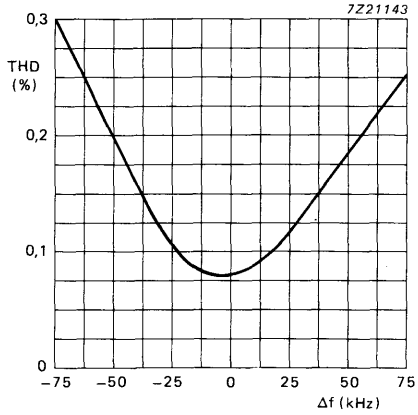


Fig. 17 Total harmonic distortion plotted against IF detuning; for $\Delta f = \pm 75$ kHz, $f_{mod} = 1$ kHz and $V_O = 500$ mV.

PROGRAMMING INFORMATION

Converting the read out of the counters into frequency

The counter resolution at the input is defined as:

- resolution = divider ratio of N2/window

For every increment of the counter the counted frequency increases relative to the resolution in Hertz, as shown in example:

- window = 20 ms; N2 = 128; IF frequency = 10,7 MHz; resolution = 128/0,02 = 6,4 kHz per count

The counter consists of 8 bits. Therefore, the maximum frequency range that can be counted is 256 x resolution = 1,6384 MHz. In the example the frequency to be counted is 10,7 MHz, therefore, the counter will overflow (in the example above, 7 times). The real measured frequency is:

- f_{real} = (read out + overflow x 256) x resolution

The overflow indicates the off-set on the frequency scale which must be added to the read out. Due to the bandwidth of the IF filter, the frequencies at the input to the TEA6100 are known, for example:

- IF filter for FM has a center frequency of 10,7 MHz and −3 dB bandwidth of 300 kHz. Only the frequencies of 10,7 MHz ± 150 kHz occur at the input of the TEA6100. For this reason it is not necessary to count the overflow.

The read out of the counter has to be translated into frequency. This translation depends upon the counter resolution. The preferred way to calculate the input frequency is to:

- calculate the read out of the target IF frequency. Compare this value with that of the measured read out and multiply the difference by the resolution.

The formulae for calculating the target IF read out and the resolution are as follows (A, D, E, F and G refer to the bits of the I^2C bus input data as shown in Figs 3 and 4 and to the counter/timer block diagram shown in Fig. 6. An, Dn, En, Fn and Gn are inverted values of the variables A, D, E, F and G. Table 3 shows the following formulae calculated for a reference frequency of 40 kHz):

- N1 = (An x 4 + A x 5) x (En x 4 + E x 5) x 8 x ($2^{[E \times 2 + G \times 1]}$) x (F x 1 + Fn x 8)
- Window (T) = $N1/F_{ref}$
- N2 = (E x 16 x 8 + En x [Dn x 1 + D x 16]) x (G x 2 + Gn x 1)
- Target decimal read out (TDEC) = T x (TIFF/N2 + (E x 247 + En x 79). TIFF is the symbol for target IF frequency
- Target read out hexadecimal (THEX), convert the target decimal read out to hexadecimal and use the 2 least significant digits (Do not use overflow value). The symbol for measured hexadecimal is MHEX
- Resolution (R) = N2/T
- Measured frequency (F_I) = (TIFF) + R x (MHEX − THEX)

Note

Care should be taken if TIFF + $\frac{1}{2}$ filter bandwidth is greater than the frequency for the read out of hexadecimal value FF, or if TIFF − $\frac{1}{2}$ filter bandwith is less than the frequency at read out for hexadecimal value 00.

- Counter accuracy (AW and AN), with bit 7 (G) the accuracy can be chosen with the same resolution. If bit 7 is logic 1 the accuracy is HIGH and if bit 7 is logic 0 then the accuracy is LOW.

  bit 7 = 0, AN = ± (N2/T)
  bit 7 = 1, AW = ± ($\frac{1}{2}$ x N2/T)

DEVELOPMENT DATA

Example

The example uses the following values:

TIFF = 10,7 MHz; accuracy = LOW (G = 0); F_{ref} = 40 kHz (A = 1); IF frequency = 10, 7 MHz (D = 1); resolution = N1 (F = 1) and counter mode = FM (E = 1)

N1 = (0 x 4 + 1 x 5) x (0 x 4 + 1 x 5) x 8 x ($2^{[1 \times 2 + 0 \times 1]}$) x (1 x 1 + 0 x 8) = 800

T = 800/40 = 20 ms

N2 = (1 x 16 x 8 + 0 x [1 x 1 + 0 x 16]) x (0 x 2 + 1 x 1) = 128

TDEC = 20 x 10,7/128 + (1 x 247 + 0 x 79) = 1919

THEX; 1919 is hexadecimal 77F and the least significant 2 digits are 7F, so THEX = 7 F

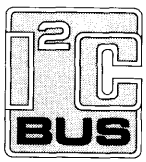
R = 128/20 = 6400 Hz/count

Assume the readout is '6E', the measured frequency will be:

- F_I = 10,7 + (6E − 7F) x 6400 = 10,59 MHz

Assume the readout is '83', the measured frequency will be:

- F_I = 10,7 + (83 − 7F) x 6400 = 10,726



INTEGRATED AM UPCONVERSION RECEIVER

GENERAL DESCRIPTION

The TEA6200 is an integrated AM upconversion receiver circuit with an IF of 10.7 MHz. Because of the high dynamic range of the RF prestage there is no tuned prestage. The whole selectivity is provided by crystal filters. The circuit is intended for use in AM radios with synthesizer tuning.
The TEA6200 can handle RF signals up to 2 V RMS.

Features

- No pre-tuned selection is required
- No LW/MW switching
- RF input is protected from static discharge from the aerial
- Electronic standby switch
- Voltage controlled oscillator for synthesizer tuning
- IF output providing level information for search tuning.
- No alignment required.

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	7.6	8.5	9.4	V
Supply current range	I_P	–	50	70	mA
AF output voltage with: RF at 1 MHz and 10 mV f_m at 400 Hz and 30%	V_{af}	–	350	–	mV
AGC start	V_{rf}	30	50	80	μV
AGC range	ΔV_{rf}	–	95	–	dB

PACKAGE OUTLINE

20-lead dual in line; plastic (SOT146).

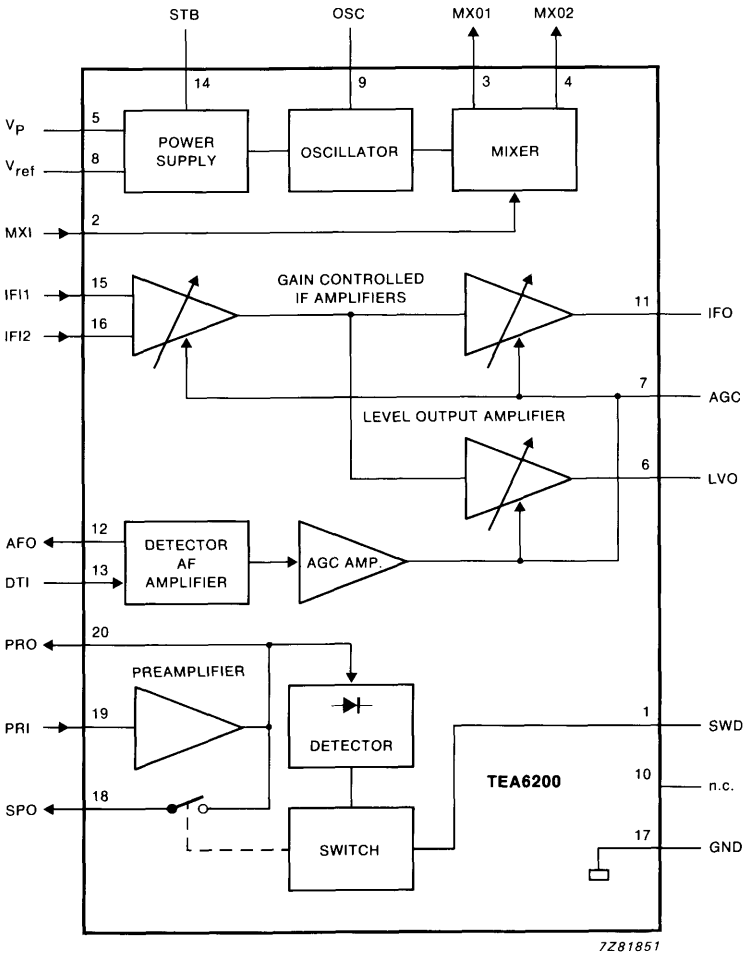


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

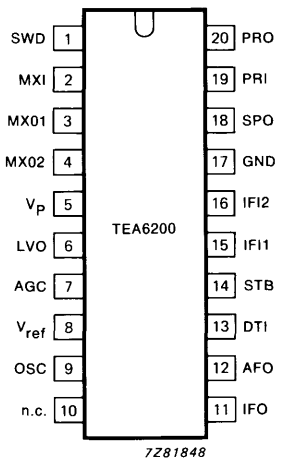


Fig. 2 Pinning diagram.

1	SWD	switching delay
2	MXI	mixer input
3	MXO1	mixer output 1
4	MXO2	mixer output 2
5	V_P	supply voltage
6	LVO	level output
7	AGC	AGC time constant
8	V_{ref}	reference voltage
9	OSC	oscillator
10	n.c.	not internally connected*
11	IFO	IF output
12	AFO	AF output
13	DTI	detector input
14	STB	standby switch
15	IFI1	IF input 1
16	IFI2	IF input 2
17	GND	ground
18	SPO	switched prestage output
19	PRI	prestage input
20	PRO	prestage output

* Pin 10 must be connected to pin 5, 8 or 17.

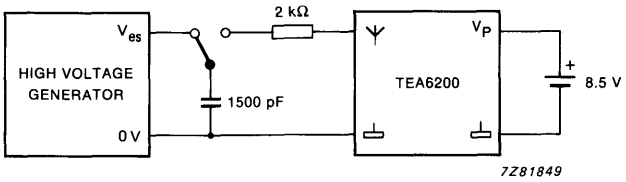
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	12	V
Supply current	I_P	–	70	mA
Total power dissipation	P_{tot}	–	850	mW
Operating ambient temperature range	T_{amb}	−30	+ 85	°C
Storage temperature range	T_{stg}	−40	+ 150	°C
Electrostatic discharge voltage	$\pm V_{es}$	–	10	kV

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 80 K/W



Will tolerate discharge between −10 kV and + 10 kV.

Fig. 3. Test circuit in accordance with IEC 315-1 clause 25.

DC CHARACTERISTICS

V_P = 8.5 V; $V_{14} = V_P$; Signal in OFF condition; all voltages referenced to ground unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Mixer input		V_I	–	4.0	–	V
Mixer output 1		V_O	–	8.5	–	V
Mixer output 2		V_O	–	8.5	–	V
Level output		V_O	–	8.5	–	V
AGC voltage		V_{AGC}	–	0.65	–	V
Reference voltage		V_{ref}	–	4.0	–	V
Oscillator DC voltage		V_{OSC}	–	4.0	–	V
Prestage input		V_I	–	1.2	–	V
Prestage output		V_O	–	3.2	–	V

CHARACTERISTICS

V_P = 8.5 V; T_{amb} = 25 °C; f_{RF} = 1 MHz at 10 mV RMS; Q_{OSC} = 50; modulation = 400 Hz at 30%; insertion loss of filters: crystal filter = 1 dB; ceramic filter = 4 dB, all voltages referenced to ground unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	7.6	8.5	9.4	V
Supply current range		I_P	–	50	70	mA
Guaranteed operating voltage		V_P	7.0	–	10.0	V
Standby switch						
ON voltage		V_{14}	3.2	–	V_P	V
OFF voltage		V_{14}	0	–	1	V
ON current		$\|I_{14}\|$	–	–	10	μA
OFF current		$-I_{14}$	–	–	0.5	mA
Supply current	device OFF	I_P	–	–	10	mA
Prestage	note 1					
Switching threshold	modulation = 80%	V_{rf}	–	320	–	mV
Hysteresis		V_{rf}	1.5	3.5	5.5	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Frequency range		f_{osc}	10.8	–	17.8	MHz
Oscillator amplitude		V_{osc}	200	420	–	mV
Tuned circuit selectivity		Q_{OSC}	20	50	–	–
Mixer						
Input capacitance		C_{2-8}	–	5	10	pF
Input impedance		Z_{2-8}	10	40	–	kΩ
Conversion transconductance		I_{3-4}/V_{2-8}	–	3.8	–	S
IF amplifier						
Input impedance		R_{16-15}	10	–	–	kΩ
Input capacitance		C_{16-15}	–	–	5	pF
Output impedance		Z_{11}	230	330	430	Ω
Detector	note 2					
Input impedance		Z_{13}	265	380	500	Ω
Output impedance		Z_{12}	7	10	14	kΩ
Output level		V_{af}	250	350	500	mV
Reference voltage						
Voltage	V_P = 8.5 V	V_8	3.8	4.0	4.2	V
Output impedance		Z_8	–	20	–	Ω
Ripple rejection		$\frac{\Delta V_P}{\Delta V_8}$	40	–	–	dB
Level output pin 6	see Fig. 5					
Output impedance		Z_6	–	1	–	kΩ
Output voltage	V_{rf} = 70 μV	V_6	0.5	0.7	1.0	mV
Output voltage	V_{rf} = 2 mV	V_6	–	15	–	mV

parameter	conditions	symbol	min.	typ.	max.	unit
RF sensitivity						
RF input	(S + N)/N = 6 dB	V_{rf}	–	11	20	μV
	(S + N)/N = 26 dB	V_{rf}	–	110	150	μV
	(S + N)/N = 46 dB	V_{rf}	–	1100	2000	μV
	RF = 150 kHz (S + N)/N = 26 dB	V_{rf}	–	200	–	μV
Output signal						
AF output voltage	V_{rf} = 10 mV	V_{af}	250	350	500	mV
	V_{rf} = 20 μV	V_{af}	–	100	–	mV
Total distortion	V_{rf} = 1 mV; modulation = 80%	d_{tot}	–	3	5	%
Signal plus noise-to-noise ratio	RF = 10 mV to 1 V	(S+N)/N	53	57	–	dB
Ripple rejection	V_P = 8.5 V + V_r 20 Hz < fR < 20 kHz V_{rms} = 40 mV	$\frac{\Delta V_P}{\Delta V_{af}}$	20	–	–	dB
Large signal handling						
Aerial input voltage	THD = 10%; modulation = 80%	V_{rf}	2	3	–	V
AGC range of preamplifier switch			–	12	–	dB
Switching threshold	modulation = 80%	V_{rf}	–	320	–	mV
Hysteresis	modulation = 80%	V_{rf}	1.5	3.5	5.5	dB
Ripple rejection of preamplifier	20 Hz < f_R < 1.5 MHz	$\frac{\Delta V_P}{\Delta V_{20}}$	–	40	–	dB
AGC						
AGC range			–	95	–	dB
Change of V_{af}	100 μV < V_{rf} < 2 V		–	2	3	dB
AGC start		V_{rf}	30	50	80	μV
Intermodulation free dynamic range						
Long wave	350/250 kHz					
second order	input noise level = –99 dBm	IMFDR 2	72	82	–	dB
third order	input noise level = –99 dBm	IMFDR 3	–	86	–	dB
Medium wave	650/1550 kHz					
second order	input noise level = –104 dBm	IMFDR 2	74	84	–	dB
third order	1.25/1.4 MHz input noise level = –104 dBm	IMFDR 3	–	90	–	dB

DEVELOPMENT DATA

Notes to the characteristics

1. The prestage is connected to the aerial by a 6 MHz low-pass filter that decouples unwanted aerial cable resonance frequencies. The large dynamic range of the prestage is achieved by use of a transimpedance amplifier with a feedback loop consisting of an equivalent aerial capacitance and a feedback capacitor. When large RF signals are received the feedback capacitance in the loop is increased and the gain subsequently reduced, (see Fig. 4).

   Voltage gain for small signals $G_V = V_{rf} \times \frac{C_{ae}}{C_1}$

   Voltage gain for large signals $G_V = V_{rf} \times \frac{C_{ae}}{C_1 + C_2}$

2. To protect the demodulator and the AGC circuitry, against parasitic oscillation in the IF section, a ceramic filter is connected between the IF output and detector input.

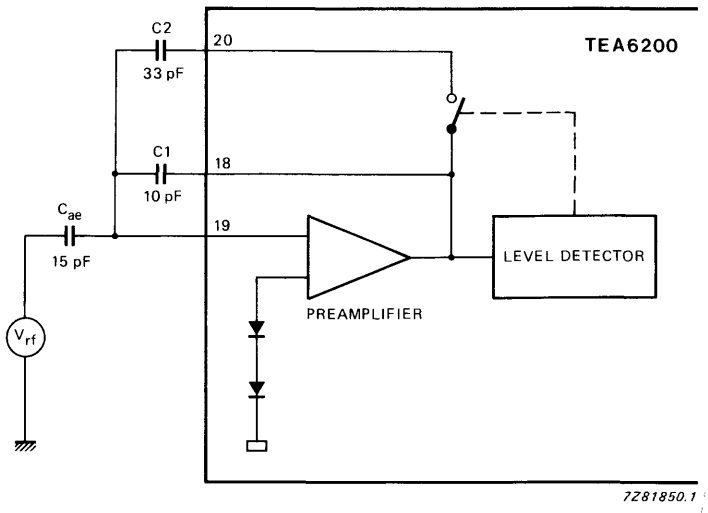


Fig. 4 Prestage circuit.

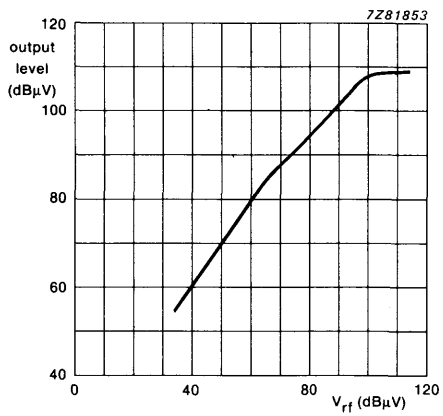


Fig. 5 IF output level.

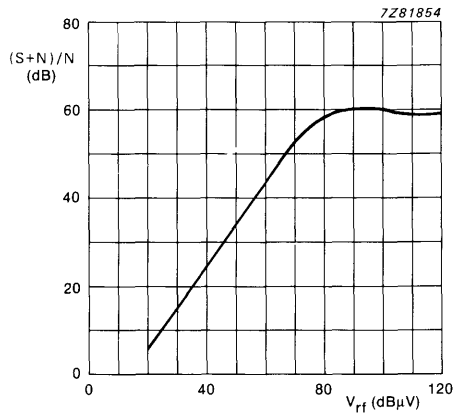


Fig. 6 Signal plus noise-to-noise ratio.

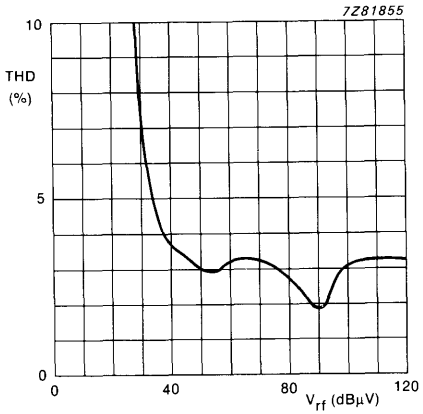


Fig. 7 Total harmonic distortion.

APPLICATION INFORMATION

Notes Fig. 8.

	Component	Circuit identity	Supplier reference
→	(1) Crystal filters	XTAL	NDK 10T 7 BA
	(2) Ceramic filter	SFE	Murata E 10 7 S
	(3) Transformer	T1	Toko 7PS-1078 JK
	(4) Variable capacitance diode.	D1	BB609, BB809 or BBY40
→	(5) Oscillator coil	L1	Toko 7PS-1077 X

DEVELOPMENT DATA

APPLICATION INFORMATION

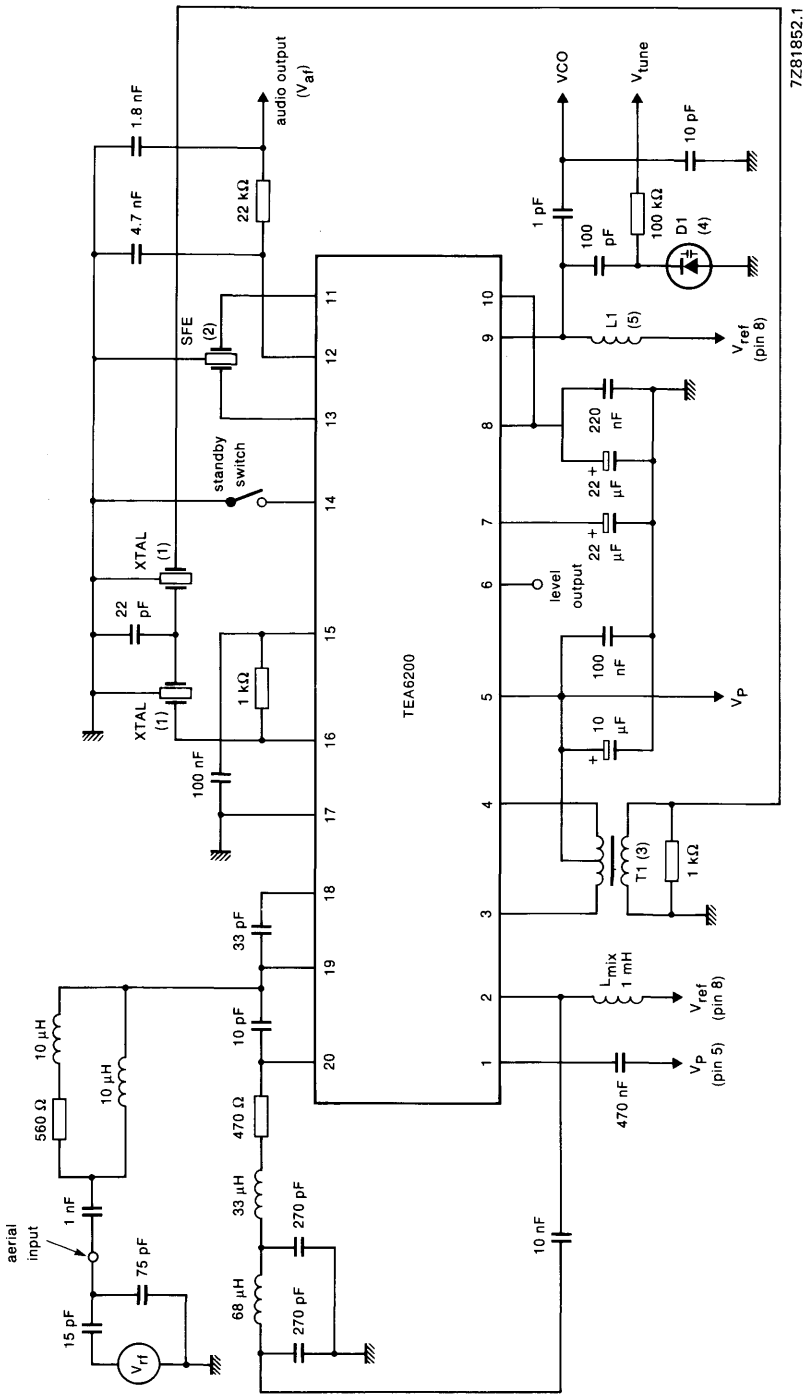


Fig. 8 Application diagram.

SOUND FADER CONTROL CIRCUIT

GENERAL DESCRIPTION

The Sound Fader Control circuit (SOFAC) is an I²C-bus controlled preamplifier for car radios.

Features

- Source selector for three stereo inputs
- Inputs and outputs for noise reduction circuits
- Volume and balance control; control range of 86 dB in steps of 2 dB
- Bass and treble control from + 15 dB (treble 12 dB) to −12 dB in steps of 3 dB
- Fader control from 0 dB to −30 dB in steps of 2 dB
- Fast muting
- Low noise suitable for DOLBY* B and C NR (noise reduction)
- Signal handling suitable for compact disc
- I²C-bus control for all functions
- ESD protected

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Input sensitivity for full power at the output stage	$V_{i(rms)}$	–	50	–	mV
Input signal handling	$V_{i(rms)}$	–	1,65	–	V
Frequency response	f_r	35	–	20 000	Hz
Channel separation f = 250 Hz to 10 kHz	α_{CS}	70	92	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Signal plus noise-to-noise ratio	(S+N)/N	–	80	–	dB
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

* Dolby is a registered trademark of Dolby Laboratories Licencing Corporation, San Fransisco, California (U.S.A.).

PACKAGE OUTLINES

28-lead dual in-line; plastic (SOT117).
28-lead mini-pack; plastic (SO28; SOT136A).

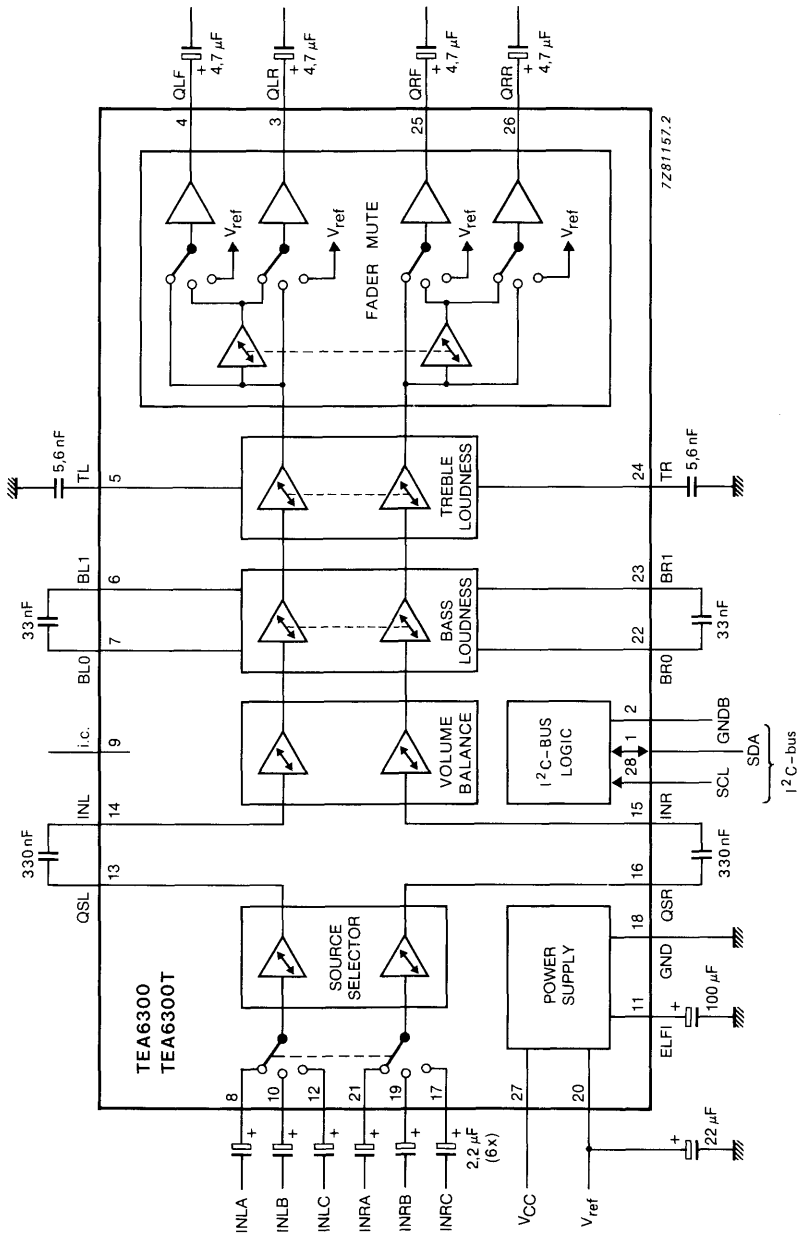


Fig. 1 Block diagram.

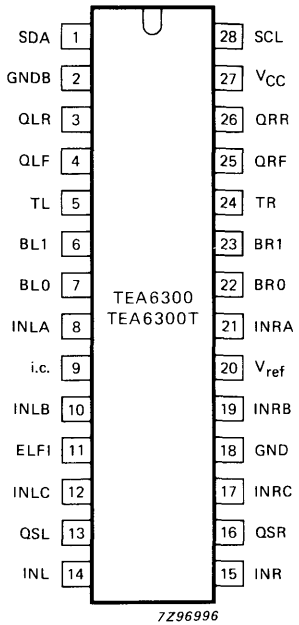


Fig. 2 Pinning diagram.

PINNING

1	SDA	serial data input/output (I^2C-bus)
2	GNDB	ground for I^2C-bus terminals
3	QLR	output left rear
4	QLF	output left front
5	TL	treble control capacitor; left channel
6	BL1	bass control capacitor; left channel
7	BL0	bass control capacitor; left channel
8	INLA	input left source A
9	i.c.	internally connected
10	INLB	input left source B
11	ELFI	electronic filtering for supply
12	INLC	input left source C
13	QSL	output source selector left
14	INL	input left control part
15	INR	input right control part
16	QSR	output source selector right
17	INRC	input right source C
18	GND	ground
19	INRB	input right source B
20	V_{ref}	reference voltage (1/2 V_{CC})
21	INRA	input right source A
22	BR0	bass control capacitor; right channel
23	BR1	bass control capacitor; right channel
24	TR	treble control capacitor; right channel
25	QRF	output right front
26	QRR	output right rear
27	V_{CC}	supply voltage
28	SCL	serial clock input (I^2C-bus)

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The source selector selects three stereo channels —RF part (AM/FM), recorder and compact disc. As the outputs of the source selector and the inputs of the main control part are available, additional circuits such as compander and equalizer systems may be inserted into the signal path. The AC signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantage of this principle is the combination of low noise, low distortion and a high dynamic range for the circuit.

The separate volume controls of the left and the right channel facilitate correct balance control. The range and balance control is software programmable.

Because the TEA6300 has four outputs a low-level fader is included. The fader control is independent of the volume control and an extra mute position is built in for the front, the rear or for all channels. The last function may be used for muting during preset selection. An extra pop suppression circuit is built in for pop-free switching on and off. As all switching and control functions are controllable via the two-wire I^2C-bus, no external interface between the microcomputer and the TEA6300 is required.

The on-chip power-on-reset sets the TEA6300 to the general mute mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 27-18)	V_{CC}	–	16	V
Maximum power dissipation	P_{tot}	–	1	W
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{CC} = 8,5 V; R_S = 600 Ω; R_L = 10 kΩ; f = 1 kHz; T_{amb} = 25 °C; test circuit Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Supply current	I_{CC}	–	26	–	mA
Supply current at 8,5 V	I_{CC}	–	–	30	mA
Supply current at 13,2 V	I_{CC}	–	–	44	mA
DC voltage inputs, outputs and reference	V_{DC}	0,45	0,5	0,55	V
Internal reference voltage (pin 20) V_{ref} = 0,5 V_{CC}	V_{REF}	–	4,25	–	V
Maximum voltage gain bass and treble linear, fader off	G_v	19	20	21	dB
Output voltage level for P_{max} at the output stage for start of clipping	$V_{o(rms)}$ $V_{o(rms)}$	– –	500 1000	– –	mV mV
Input sensitivity at V_o = 500 mV	$V_{i(rms)}$	–	50	–	mV
Frequency response bass and treble linear; roll-off frequency −1 dB	f_r	35	–	20 000	Hz
Channel separation G_v = 0 dB; bass and treble linear; frequency range 250 Hz to 10 kHz	α_{CS}	70	92	–	dB
Total harmonic distortion frequency range 20 Hz to 12,5 kHz					
V_i = 50 mV; G_v = 20 dB	THD	–	0,1	0,3	%
V_i = 500 mV; G_v = 0 dB	THD	–	0,05	0,2	%
V_i = 1,6 V; G_v = −10 dB	THD	–	0,2	0,5	%
Ripple rejection $V_{r(rms)}$ < 200 mV; G_v = 0 dB; bass and treble linear;					
at f = 100 Hz	RR_{100}	–	70	–	dB
at f = 40 Hz to 12,5 kHz	RR_{range}	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal plus noise-to-noise ratio bass and treble linear; notes 1 and 2 CCIR 468-2 weighted; quasi peak					
V_i = 50 mV; V_o = 46 mV; P_o = 50 mW	(S + N)/N	–	65	–	dB
V_i = 500 mV; V_o = 45 mV; P_o = 50 mW	(S + N)/N	–	67	–	dB
V_i = 50 mV; V_o = 200 mV; P_o = 1 W	(S + N)/N	65	70	–	dB
V_i = 500 mV; V_o = 200 mV; P_o = 1 W	(S + N)/N	65	78	–	dB
V_i = 50 mV; V_o = 500 mV; P_o = 6 W	(S + N)/N	–	70	–	dB
V_i = 500 mV; V_o = 500 mV; P_o = 6 W	(S + N)/N	–	85	–	dB
Noise output power mute position, only contribution of TEA6300; power amplifier for 25 W	P_{no}	–	–	10	nW
Crosstalk (20 log $V_{bus(p-p)}/V_{o(rms)}$) between bus inputs and signal outputs G_V = 0 dB; bass and treble linear	α_B	–	110	–	dB
Source selector					
Input impedance	Z_i	20	30	40	kΩ
Output impedance	Z_o	–	–	100	Ω
Output load resistance	R_L	10	–	–	kΩ
Output load capacity	C_L	0	–	200	pF
Input isolation not selected source; frequency range 40 Hz to 12,5 kHz	α_S	–	80	–	dB
Voltage gain $R_L \geqslant 10$ kΩ	G_v	–	0	–	dB
Internal bias voltage ratio	$V_{b\,int}/V_{ref}$	–	1	–	
Maximum input voltage level (RMS value)					
THD < 0,5%	$V_{i(rms)}$	–	1,65	–	V
THD < 0,5%; V_{CC} = 7,5 V	$V_{i(rms)}$	–	1,5	–	V
Total harmonic distortion V_i = 500 mV; R_L = 10 kΩ	THD	–	–	0,1	%
Noise output voltage weighted CCIR 468-2, quasi peak	V_{no}	–	9	20	μV
DC offset voltage between any inputs	V_o	–	–	10	mV
Control part					
Source selector disconnected, source resistance 600 Ω					
Input impedance	Z_i	35	50	65	kΩ
Output impedance	Z_o	–	100	150	Ω
Output load resistance	R_L	5	–	–	kΩ
Output load capacity	C_L	0	–	2500	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Maximum input voltage THD < 0,5%; G_v = −10 dB; bass and treble linear	$V_{i(rms)}$	–	2,0	–	V
Noise output voltage weighted acc CCIR 468-2, quasi peak, bass and treble linear, fader off					
G_v = 20 dB	V_{no}	–	110	220	μV
G_v = 0 dB	V_{no}	–	25	50	μV
G_v = −66 dB	V_{no}	–	19	38	μV
mute position	V_{no}	–	11	22	μV
Volume control					
Continuous control range	G_c	–	86	–	dB
Step resolution		–	2	–	dB
Attenuator set error (G_v = + 20 to −50 dB)	ΔG_a	–	–	2	dB
Attenuator set error (G_v = + 20 to −66 dB)	ΔG_a	–	–	3	dB
Gain tracking error balance in mid position, bass and treble linear	ΔG_t	–	–	2	dB
Mute attenuation	α_m	76	90	–	dB
DC step offset					
Between any adjoining step and any step to mute					
G_v = 0 to −66 dB		–	0,2	10	mV
G_v = 20 to 0 dB		–	2	15	mV
In any treble and fader position G_v = 0 to −66 dB		–	–	10	mV
In any bass position G_v = 0 to −66 dB		–	–	20	mV
Bass control					
Bass control range					
f = 40 Hz; maximum boost	G_b	14	15	16	dB
f = 40 Hz; maximum attenuation	G_b	11	12	13	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Treble control					
Treble control range					
f = 15 kHz; maximum boost	G_t	11	12	13	dB
f = 15 kHz; maximum attenuation	G_t	11	12	13	dB
f > 15 kHz; maximum boost	G_t	–	–	15	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Fader control					
Continuous attenuation fader control range	G_f	–	30	–	dB
Step resolution		–	2	–	dB
Attenuator set error		–	–	1,5	dB
Mute attenuation	α_m	74	84	–	dB
Digital part					
Bus terminals					
Input voltage					
HIGH	V_{IH}	3	–	12	V
LOW	V_{IL}	−0,3	–	+ 1,5	V
Input current					
HIGH	I_{IH}	−10	–	+ 10	μA
LOW	I_{IL}	−10	–	+ 10	μA
Output voltage LOW I_L = 3 mA	V_{OL}	–	–	0,4	V
AC characteristics					
in accordance with the I^2C-bus specification					
Power-on-Reset					
When RESET is active the GMU (general mute) bit is set and the I^2C-bus receiver is in RESET position					
Increasing supply voltage					
start of reset	V_{CC}	–	–	2,5	V
end of reset	V_{CC}	5,2	6,0	6,8	V
Decreasing supply voltage					
start of reset	V_{CC}	4,2	5,0	5,8	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier with 20 dB gain, connected to the output of the circuit. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. Signal-to-noise ratios on a CCIR 468-2 average meter reading are 4,5 dB better than on CCIR 468-2 quasi peak.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

S = start condition
SLAVE ADDRESS = 1000 0000
A = acknowledge, generated by the slave
SUBADDRESS = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; subaddress/data

function	subaddress	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
volume left	0 0 0 0 0 0 0 0	X	X	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0 0 0 0 0 0 0 1	X	X	VR5	VR4	VR3	VR2	VR1	VR0
bass	0 0 0 0 0 0 1 0	X	X	X	X	BA3	BA2	BA1	BA0
treble	0 0 0 0 0 0 1 1	X	X	X	X	TR3	TR2	TR1	TR0
fader	0 0 0 0 0 1 0 0	X	X	MFN	FCH	FA3	FA2	FA1	FA0
switch	0 0 0 0 0 1 0 1	GMU	X	X	X	X	SCC	SCB	SCA

Function of the bits:

VL0 to VL5	volume control left
VR0 to VR5	volume control right
BA0 to BA3	bass control
TR0 to TR3	treble control
FA0 to FA3	fader control
FCH	select fader channel (front or rear)
MFN	mute control of the selected fader channel (front or rear)
SCA to SCC	source selector control
GMU	mute control (general mute) for the outputs QLF, QLR, QRF and QRR
X	don't care bits (logic 1 during testing)

DEVELOPMENT DATA

Table 2 Bass setting

G_V dB	DATA			
	BA3	BA2	BA1	BA0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 3 Treble setting

G_V dB	DATA			
	TR3	TR2	TR1	TR0
+12	1	1	1	1
+12	1	1	1	0
+12	1	1	0	1
+12	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

DEVELOPMENT DATA

Table 4 Volume setting LEFT

G_V dB	DATA					
	VL5	VL4	VL3	VL2	VL1	VL0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute left	0	0	0	0	0	0

Table 5 Volume setting RIGHT

G_V dB	DATA					
	VR5	VR4	VR3	VR2	VR1	VR0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute right	0	0	0	0	0	0

Table 6 Fader function

setting front dB	setting rear dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
− 2	0	1	1	1	1	1	0
− 4	0	1	1	1	1	0	1
− 6	0	1	1	1	1	0	0
− 8	0	1	1	1	0	1	1
−10	0	1	1	1	0	1	0
−12	0	1	1	1	0	0	1
−14	0	1	1	1	0	0	0
−16	0	1	1	0	1	1	1
−18	0	1	1	0	1	1	0
−20	0	1	1	0	1	0	1
−22	0	1	1	0	1	0	0
−24	0	1	1	0	0	1	1
−26	0	1	1	0	0	1	0
−28	0	1	1	0	0	0	1
−30	0	1	1	0	0	0	0
		mute front					
−80	0	0	1	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
−80	0	0	1	0	0	0	0

setting front dB	setting rear dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	− 2	1	0	1	1	1	0
0	− 4	1	0	1	1	0	1
0	− 6	1	0	1	1	0	0
0	− 8	1	0	1	0	1	1
0	−10	1	0	1	0	1	0
0	−12	1	0	1	0	0	1
0	−14	1	0	1	0	0	0
0	−16	1	0	0	1	1	1
0	−18	1	0	0	1	1	0
0	−20	1	0	0	1	0	1
0	−22	1	0	0	1	0	0
0	−24	1	0	0	0	1	1
0	−26	1	0	0	0	1	0
0	−28	1	0	0	0	0	1
0	−30	1	0	0	0	0	0
		mute rear					
0	−80	0	0	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
0	−80	0	0	0	0	0	0

Table 7 Selected inputs

selected inputs	DATA SCC	SCB	SCA
data not allowed	1	1	1
data not allowed	1	1	0
data not allowed	1	0	1
INLC, INRC	1	0	0
data not allowed	0	1	1
INLB, INRB	0	1	0
INLA, INRA	0	0	1
data not allowed	0	0	0

Table 8 Mute control

MUTE control	DATA GMU	remarks
active	1	outputs QLF, QLR QRF and QRR are muted
passive	0	no general mute

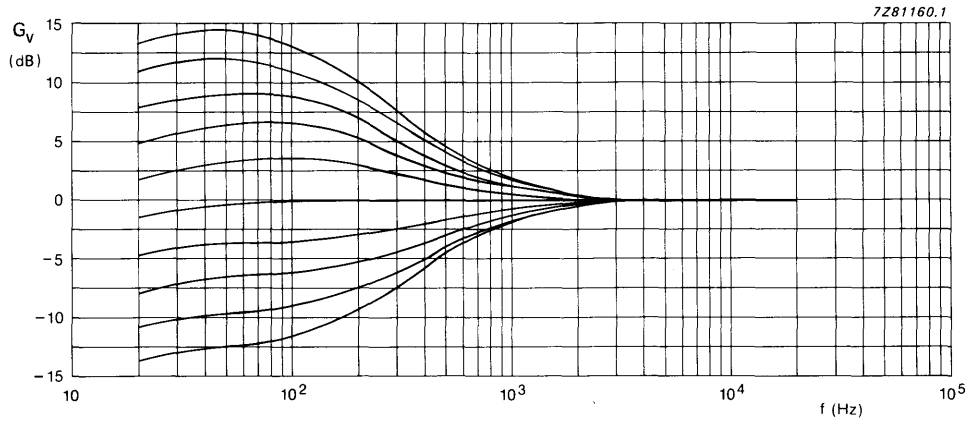


Fig. 3 Bass control without T-pass filter.

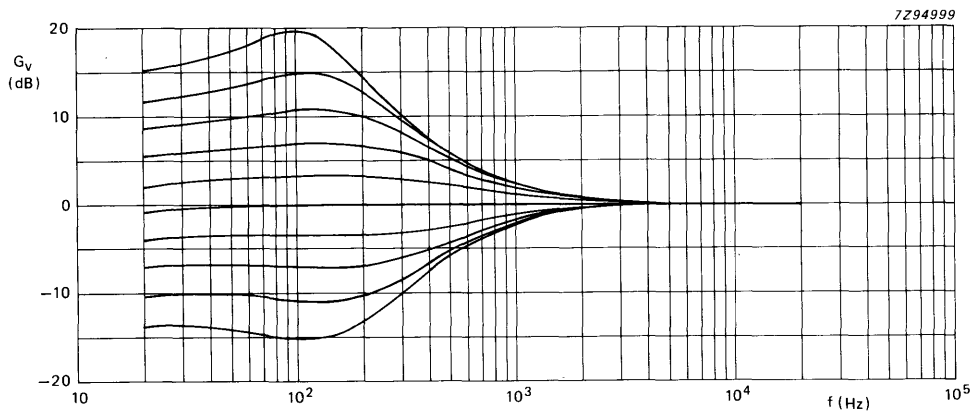
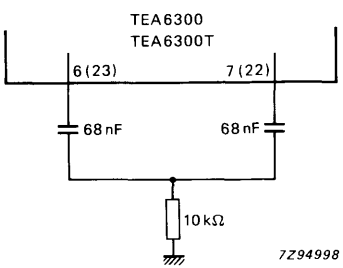


Fig. 4 Bass control with T-pass filter.



Pin numbers in parenthases refer to the bass control, right channel.

Fig. 5 T-pass filter.

DEVELOPMENT DATA

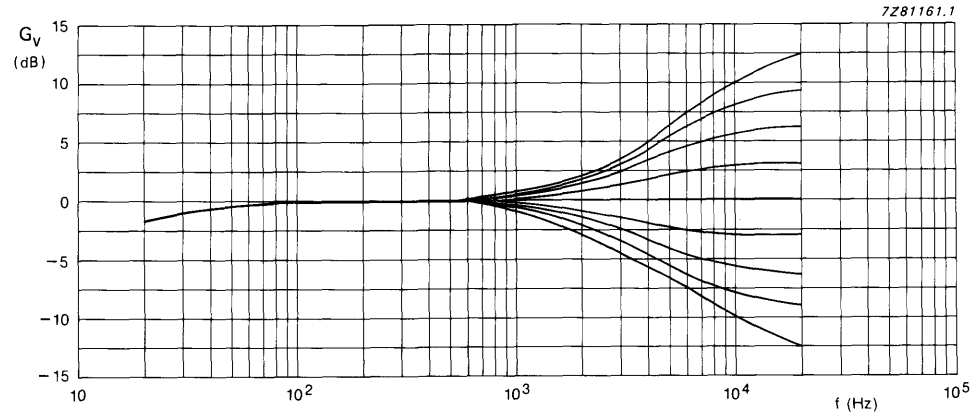


Fig. 6 Treble control.

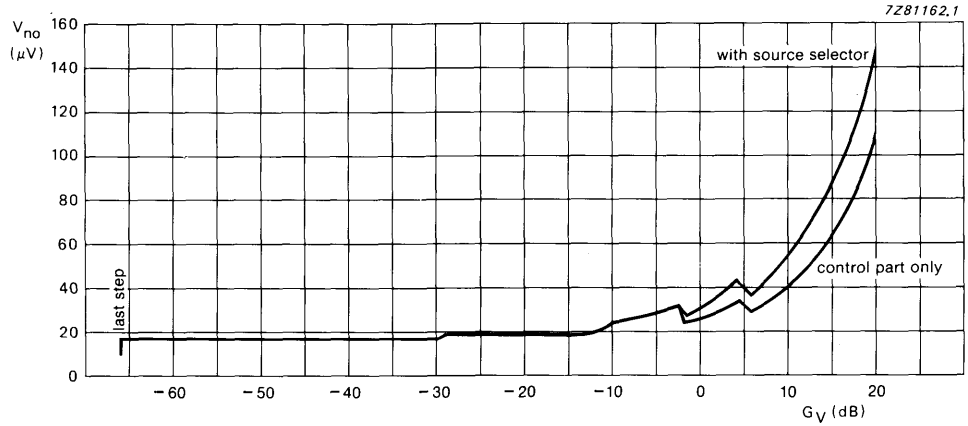


Fig. 7 Output noise voltage (CCIR 468-2 weighted: quasi peak).

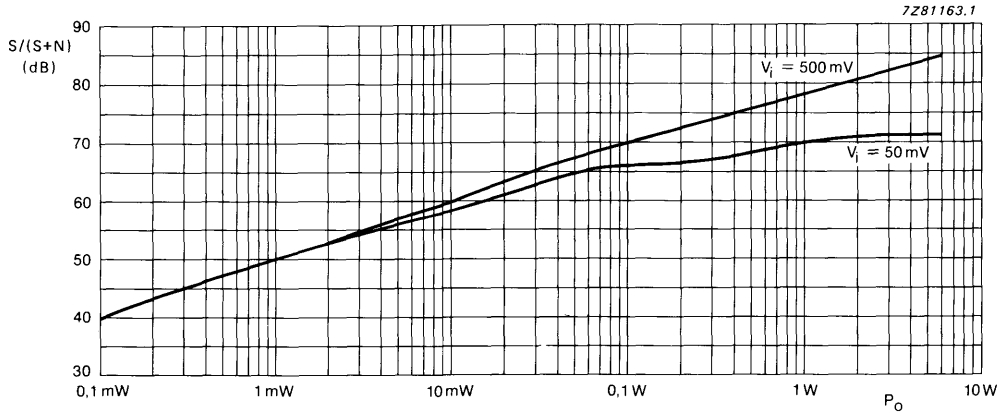


Fig. 8 Signal-to-noise ratio (CCIT 468-2 weighted; quasi peak) with a 6 W power amplifier (gain 20 dB) without noise contribution of the power amplifier (see Fig. 9).

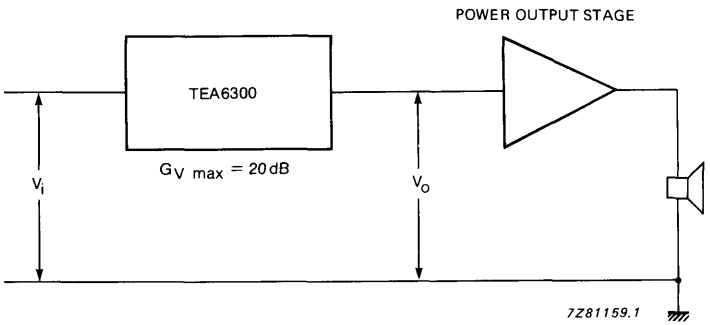


Fig. 9 Recommended level diagram; $V_{i\ min}$ = 50 mV, V_o = 500 mV for P_{max}.

DEVELOPMENT DATA

APPLICATION INFORMATION

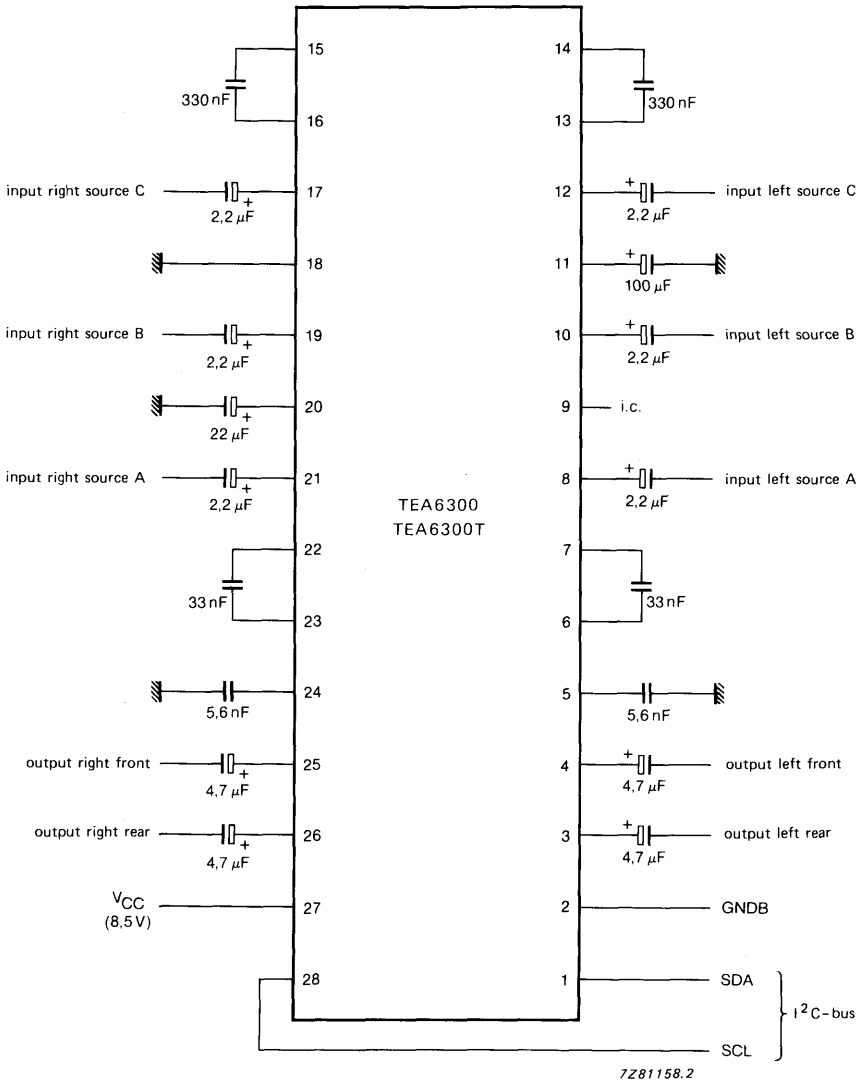


Fig. 10 Test and application circuit.

SOUND FADER CONTROL CIRCUIT

GENERAL DESCRIPTION

The Sound Fader Control circuit (SOFAC) is an I²C-bus controlled tone and volume control circuit for car radios.

Features

- Volume and balance control; control range of 86 dB in steps of 2 dB
- Bass and treble control from +15 dB (treble 12 dB) to −12 dB in steps of 3 dB
- Fader control form 0 dB to −30 dB in steps of 2 dB
- Fast muting
- Low noise suitable for Dolby* B and C NR (noise reduction)
- Signal handling suitable for compact disc
- I²C-bus control for all functions
- ESD protected

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Input sensitivity for full power at the output stage	$V_{i(rms)}$	–	50	–	mV
Input signal handling	$V_{i(rms)}$	–	1,65	–	V
Frequency response	f_r	35	–	20 000	Hz
Channel separation f = 250 Hz to 10 kHz	α_{CS}	70	96	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Signal plus noise-to-noise ratio	(S+N)/N	–	80	–	dB
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

* Dolby is a registered trademark of Dolby Laboratories Licencing Corporation, San Fransisco, California (U.S.A.).

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

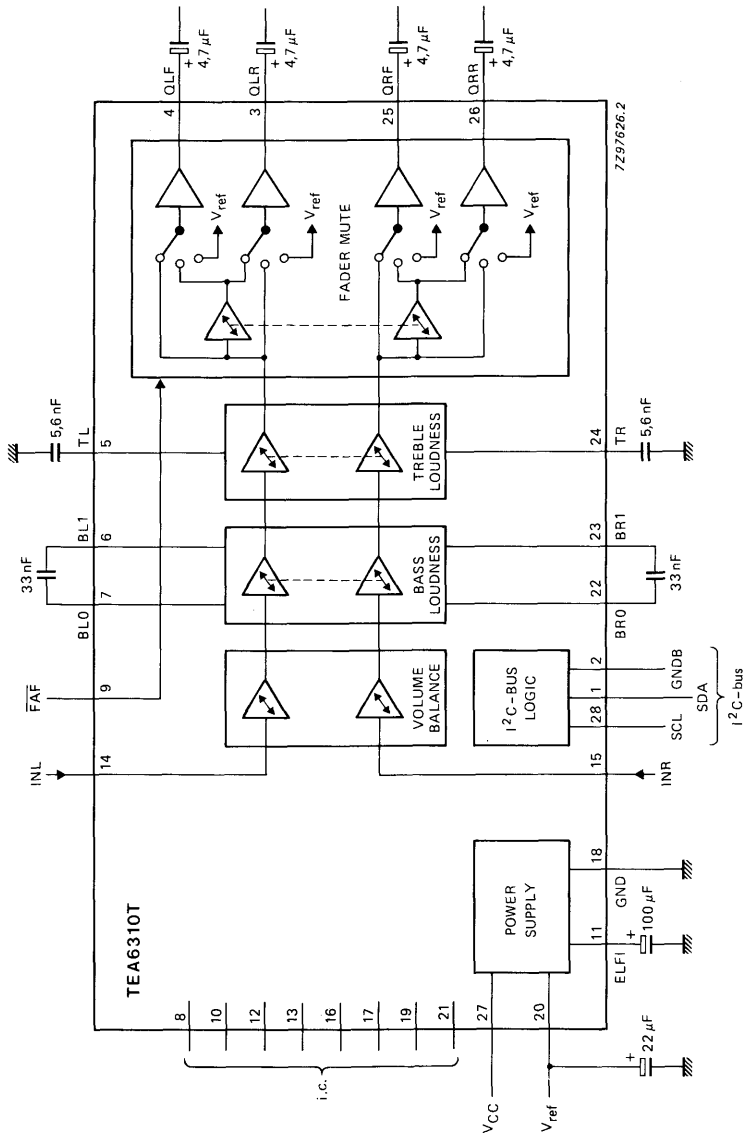


Fig. 1 Block diagram.

DEVELOPMENT DATA

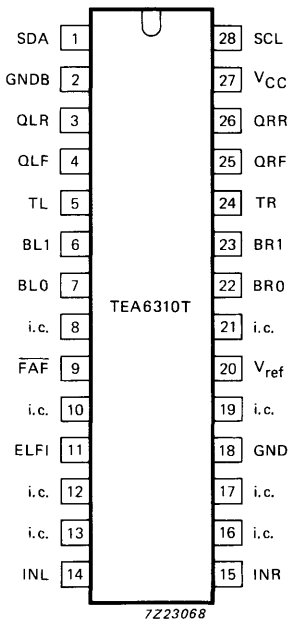


Fig. 2 Pinning diagram

PINNING

1	SDA	serial data input/output (I^2C-bus)
2	GNDB	ground for I^2C-bus terminals
3	QLR	output left rear
4	QLF	output left front
5	TL	treble control capacitor; left channel
6	BL1	bass control capacitor; left channel
7	BL0	bass control capacitor; left channel
8	i.c.	internally connected
9	$\overline{FAF}$	fader off control input
10	i.c.	internally connected
11	ELFI	electronic filtering for supply
12	i.c.	internally connected
13	i.c.	internally connected
14	INL	input left control part
15	INR	input right control part
16	i.c.	internally connected
17	i.c.	internally connected
18	GND	ground
19	i.c.	internally connected
20	V_{ref}	reference voltage (1/2 V_{CC})
21	i.c.	internally connected
22	BR0	bass control capacitor; right channel
23	BR1	bass control capacitor; right channel
24	TR	treble control capacitor; right channel
25	QRF	output right front
26	QRR	output right rear
27	V_{CC}	supply voltage
28	SCL	serial clock input (I^2C-bus)

FUNCTIONAL DESCRIPTION

The AC signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantage of this principle is the combination of low noise, low distortion and a high dynamic range for the circuit.

The separate volume controls of the left and the right channel facilitate correct balance control. The range and balance control is software programmable.

Because the TEA6310T has four outputs a low level fader is included. The fader control is independent of the volume control and an extra mute position is built in for the front, the rear or for all channels. The last function may be used for muting during preset selection. The Fader function can be disabled by an input signal at $\overline{FAF}$ (pin 9).
An extra pop suppression circuit is built in for pop-free switching on and off. As all switching and control functions are controllable via the two-wire I^2C-bus, no external interface between the micro-computer and the TEA6310T is required.

The on-chip power-on-reset sets the TEA6310T to the general mute mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 27-18)	V_{CC}	–	16	V
Maximum power dissipation	P_{tot}	–	1	W
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{CC} = 8,5 V; R_S = 600 Ω; R_L = 10 kΩ; f = 1 kHz; T_{amb} = 25 °C; test circuit Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Supply current	I_{CC}	–	26	–	mA
Supply current at 8,5 V	I_{CC}	–	–	30	mA
Supply current at 13,2 V	I_{CC}	–	–	44	mA
DC voltage inputs, outputs and reference	V_{DC}	0,45	0,5	0,55	V
Internal reference voltage (pin 20) V_{ref} = 0,5 V_{CC}	V_{REF}	–	4,25	–	V
Maximum voltage gain bass and treble linear, fader off	G_v	19	20	21	dB
Output voltage level for P_{max} at the output stage	$V_{o(rms)}$	–	500	–	mV
for start of clipping	$V_{o(rms)}$	–	1000	–	mV
Input sensitivity at V_o = 500 mV	$V_{i(rms)}$	–	50	–	mV
Frequency response bass and treble linear; roll-off frequency −1 dB	f_r	35	–	20 000	Hz
Channel separation G_v = 0 dB; bass and treble linear; frequency range 250 Hz to 10 kHz	α_{CS}	70	96	–	dB
Total harmonic distortion frequency range 20 Hz to 12,5 kHz					
V_i = 50 mV; G_v = 20 dB	THD	–	0,1	0,3	%
V_i = 500 mV; G_v = 0 dB	THD	–	0,05	0,2	%
V_i = 1,6 V; G_v = −10 dB	THD	–	0,2	0,5	%
Ripple rejection $V_{r(rms)}$ <200 mV; G_v = 0 dB; bass and treble linear;					
at f = 100 Hz	RR_{100}	–	70	–	dB
at f = 40 Hz to 12,5 kHz	RR_{range}	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal-to-noise ratio; bass and treble linear; notes 1 and 2; CCIR 468-2 weighted; quasi peak;					
V_i = 50 mV; V_o = 46 mV; P_o = 50 mW	S/(S + N)	–	65	–	dB
V_i = 500 mV; V_o = 45 mV; P_o = 50 mW	S/(S + N)	–	67	–	dB
V_i = 50 mV; V_o = 200 mV; P_o = 1 W	S/(S + N)	65	72	–	dB
V_i = 500 mV; V_o = 200 mV; P_o = 1 W	S/(S + N)	65	78	–	dB
V_i = 50 mV, V_o = 500 mV; P_o = 6 W	S/(S + N)	–	72	–	dB
V_i = 500 mV; V_o = 500 mV; P_o = 6 W	S/(S + N)	–	86	–	dB
Noise output power mute position, only contribution of TEA310T, power amplifier for 25 W	P_{no}	–	–	10	nW
Crosstalk (20 log $V_{bus(p-p)}/V_{o(rms)}$) between bus inputs and signal outputs G_v = 0 dB; bass and treble linear;	α_B	–	110	–	dB
Control part					
Input impedance	Z_i	35	50	65	kΩ
Output impedance	Z_o	–	100	150	Ω
Output load resistance	R_L	5	–	–	kΩ
Output load capacity	C_L	0	–	2500	pF
Maximum input voltage; THD < 0,5%; G_v = −10 dB; bass and treble linear	$V_{i(rms)}$	–	2,0	–	V
Noise output voltage; weighted acc CCIR 468-2, quasi peak, bass and treble linear, fader off;					
G_v = 20 dB	V_{no}	–	110	220	μV
G_v = 0 dB	V_{no}	–	25	50	μV
G_v = −66 dB	V_{no}	–	19	38	μV
mute position	V_{no}	–	11	22	μV
Volume control					
Continuous control range	G_c	–	86	–	dB
Step resolution		–	2	–	dB
Attenuator set error; (G_v = + 20 to −50 dB)	ΔG_a	–	–	2	dB
Attenuator set error; (G_v = + 20 to −66 dB)	ΔG_a	–	–	3	dB
Gain tracking error; balance in mid position, bass and treble linear	ΔG_t	–	–	2	dB
Mute attenuation	α_m	76	90	–	dB

parameter	symbol	min.	typ.	max.	unit
DC step offset					
Between any adjoining step and any step to mute					
G_v = 0 to −66 dB		–	0,2	10	mV
G_v = 20 to 0 dB		–	2	15	mV
In any treble and fader position					
G_v = 0 to −66 dB		–	–	10	mV
In any bass position					
G_v = 0 to −66 dB		–	–	20	mV
Bass control					
Bass control range;					
f = 40 Hz; maximum boost	G_b	14	15	16	dB
f = 40 Hz; maximum attenuation	G_b	11	12	13	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Treble control					
Treble control range					
f = 15 kHz; maximum boost	G_t	11	12	13	dB
f = 15 kHz; maximum attenuation	G_t	11	12	13	dB
f > 15 kHz; maximum boost	G_t	–	–	15	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Fader control					
Continous attenuation fader control range	G_f	–	30	–	dB
Step resolution		–	2	–	dB
Attenuator set error		–	–	1,5	dB
Mute attenuation	α_m	74	84	–	dB
Fader enable/disable control (pin 9)					
Fader enabled					
Input voltage HIGH	$V_{9\text{-}18}$	3	–	12	V
Fader disabled					
Input voltage LOW	$V_{9\text{-}18}$	−0,3	–	1,5	V
Input current					
HIGH	I_9	−10	–	+10	μA
LOW	I_9	−10	–	+10	μA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Digital part					
Bus terminals					
Input voltage					
HIGH	V_{IH}	3	–	12	V
LOW	V_{IL}	−0,3	–	1,5	V
Input current					
HIGH	I_{IH}	−10	–	+10	μA
LOW	I_{IL}	−10	–	+10	μA
Output voltage LOW I_L = 3 mA	V_{OL}	–	–	0,4	V
AC characteristics					
in accordance with the I^2C-bus specification					
Power-on-Reset					
When RESET is active the GMU (general mute) bit is set and the I^2C-bus receiver is in RESET position					
Increasing supply voltage					
start of reset	V_{CC}	–	–	2,5	V
end of reset	V_{CC}	5,2	6,0	6,8	V
Decreasing supply voltage start of reset	V_{CC}	4,2	5,0	5,8	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier with 20 dB gain, connected to the output of the circuit. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. Signal-to-noise ratios on a CCIR 468-2 average meter reading are 4,5 dB better than on CCIR 468-2 quasi peak.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

S = start condition
SLAVE ADDRESS = 10000 0000
A = acknowledge, generated by the slave
SUBADDRESS = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; subaddress/data

function	subaddress	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
volume left	00000000	X	X	VL5	VL4	VL3	VL2	VL1	VL0
volume right	00000001	X	X	VR5	VR4	VR3	VR2	VR1	VR0
bass	00000010	X	X	X	X	BA3	BA2	BA1	BA0
treble	00000011	X	X	X	X	TR3	TR2	TR1	TR0
fader	00000100	X	X	MFN	FCH	FA3	FA2	FA1	FA0
switch	00000101	GMU	X	X	X	X	X	X	X

Function of the bits:

VL0 to VL5	volume control left
VR0 to VR5	volume control right
BA0 to BA3	bass control
TR0 to TR3	treble control
FA0 to FA3	fader control
FCH	select fader channel (front or rear)
MFN	mute control of the selected fader channel (front or rear)
GMU	mute control (general mute) for the outputs QLF, QLR, QRF and QRR
X	don't care bits (logic 1 during testing)

DEVELOPMENT DATA

Table 2 Bass setting

G_V dB	DATA			
	BA3	BA2	BA1	BA0
+ 15	1	1	1	1
+ 15	1	1	1	0
+ 15	1	1	0	1
+ 15	1	1	0	0
+ 12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 3 Treble setting

G_V dB	DATA			
	TR3	TR2	TR1	TR0
+ 12	1	1	1	1
+ 12	1	1	1	0
+ 12	1	1	0	1
+ 12	1	1	0	0
+ 12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

DEVELOPMENT DATA

Table 4 Volume setting LEFT

G_V dB	DATA					
	VL5	VL4	VL3	VL2	VL1	VL0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute left	0	0	0	0	0	0

Table 5 Volume setting RIGHT

G_V dB	DATA					
	VR5	VR4	VR3	VR2	VR1	VR0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute right	0	0	0	0	0	0

Table 6 Fader function

setting		DATA					
front dB	rear dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
− 2	0	1	1	1	1	1	0
− 4	0	1	1	1	1	0	1
− 6	0	1	1	1	1	0	0
− 8	0	1	1	1	0	1	1
−10	0	1	1	1	0	1	0
−12	0	1	1	1	0	0	1
−14	0	1	1	1	0	0	0
−16	0	1	1	0	1	1	1
−18	0	1	1	0	1	1	0
−20	0	1	1	0	1	0	1
−22	0	1	1	0	1	0	0
−24	0	1	1	0	0	1	1
−26	0	1	1	0	0	1	0
−28	0	1	1	0	0	0	1
−30	0	1	1	0	0	0	0
		mute front					
−80	0	0	1	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
−80	0	0	1	0	0	0	0

setting		DATA					
front dB	rear dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	− 2	1	0	1	1	1	0
0	− 4	1	0	1	1	0	1
0	− 6	1	0	1	1	0	0
0	− 8	1	0	1	0	1	1
0	−10	1	0	1	0	1	0
0	−12	1	0	1	0	0	1
0	−14	1	0	1	0	0	0
0	−16	1	0	0	1	1	1
0	−18	1	0	0	1	1	0
0	−20	1	0	0	1	0	1
0	−22	1	0	0	1	0	0
0	−24	1	0	0	0	1	1
0	−26	1	0	0	0	1	0
0	−28	1	0	0	0	0	1
0	−30	1	0	0	0	0	0
		mute rear					
0	−80	0	0	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
0	−80	0	0	0	0	0	0

Table 7 Mute control

MUTE control	DATA GMU	remarks
active	1	outputs QLF, QLR QRF and QRR are muted
passive	0	no general mute

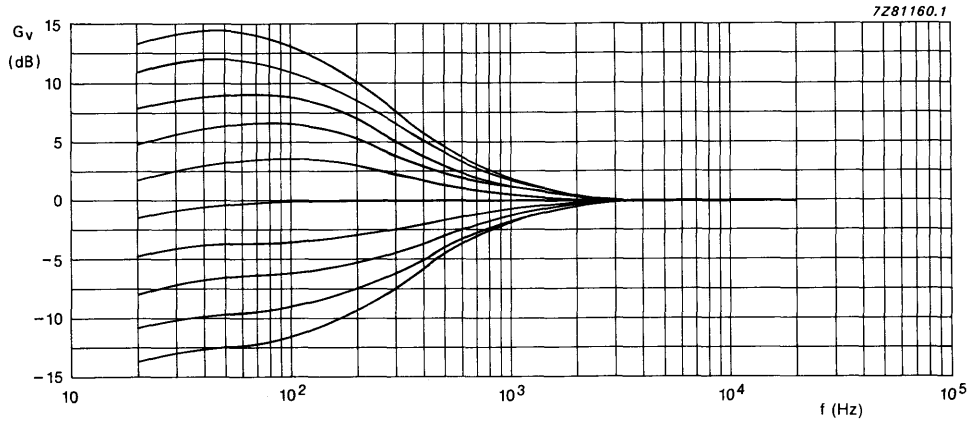


Fig. 3 Bass control without T-pass filter.

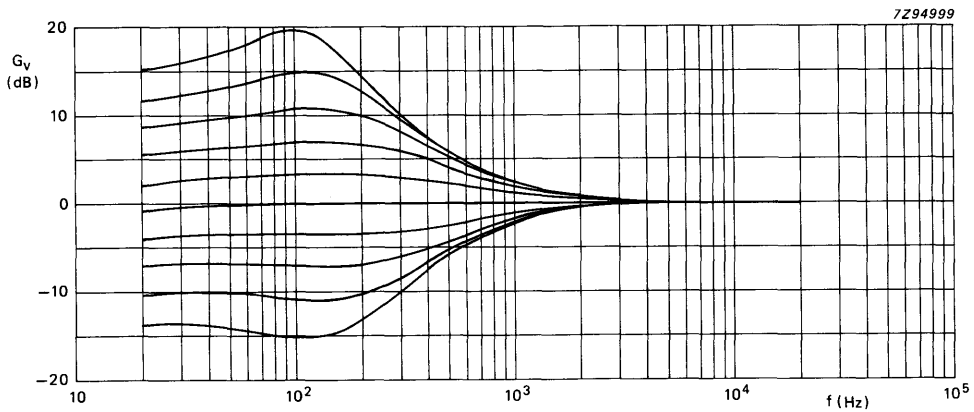
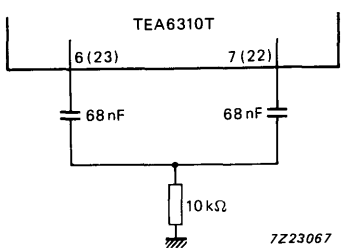


Fig. 4 Bass control with T-pass filter.



Pin numbers in parentheses refer to the bass control, right channel.

Fig. 5 T-pass filer.

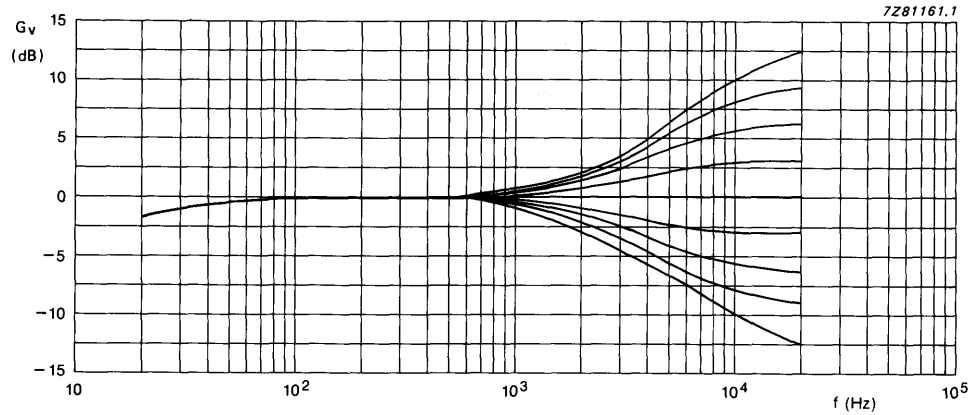


Fig. 6 Treble control.

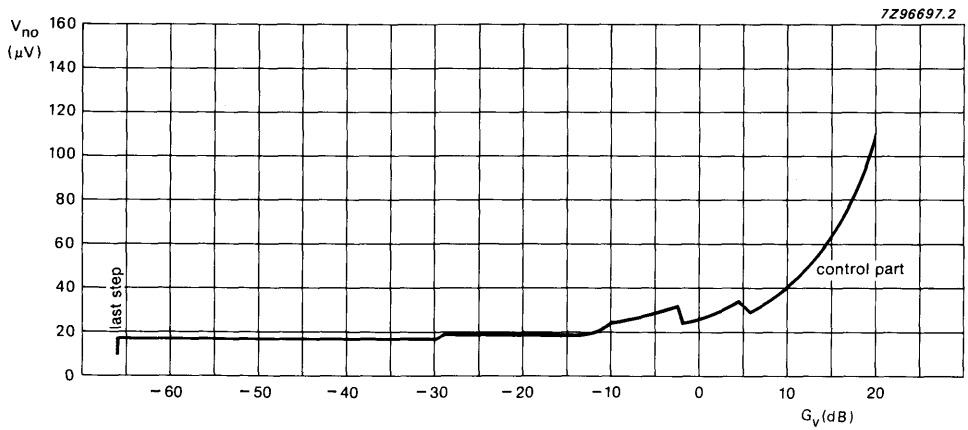


Fig. 7 Output noise voltage (CCIR 468-2 weighted: quasi peak).

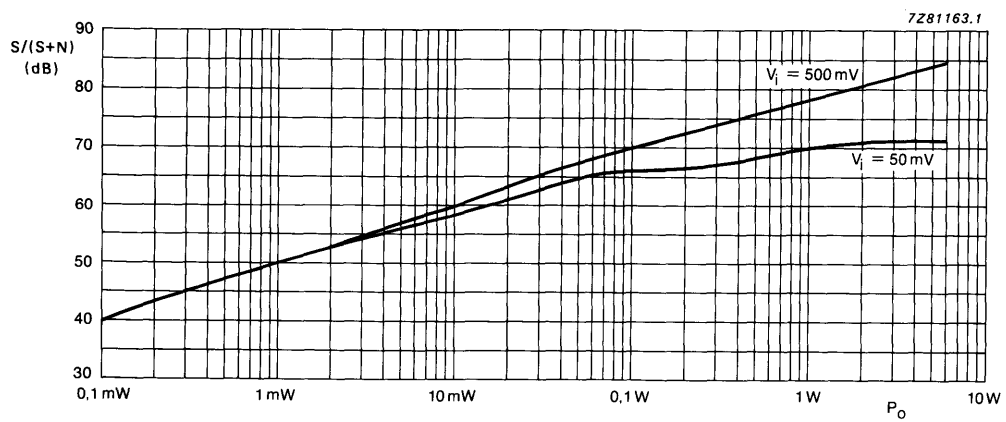


Fig. 8 Signal-tc-noise ratio (CCIT 468-2 weighted; quasi peak) with a 6 W power amplifier (gain 20 dB) without noise contribution of the power amplifier (see Fig. 9).

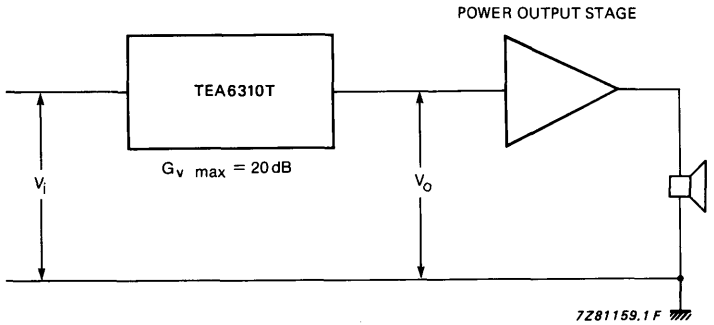


Fig. 9 Recommended level diagram; $V_{i\,min}$ = 50 mV, V_o = 500 mV for P_{max}.

DEVELOPMENT DATA

APPLICATION INFORMATION

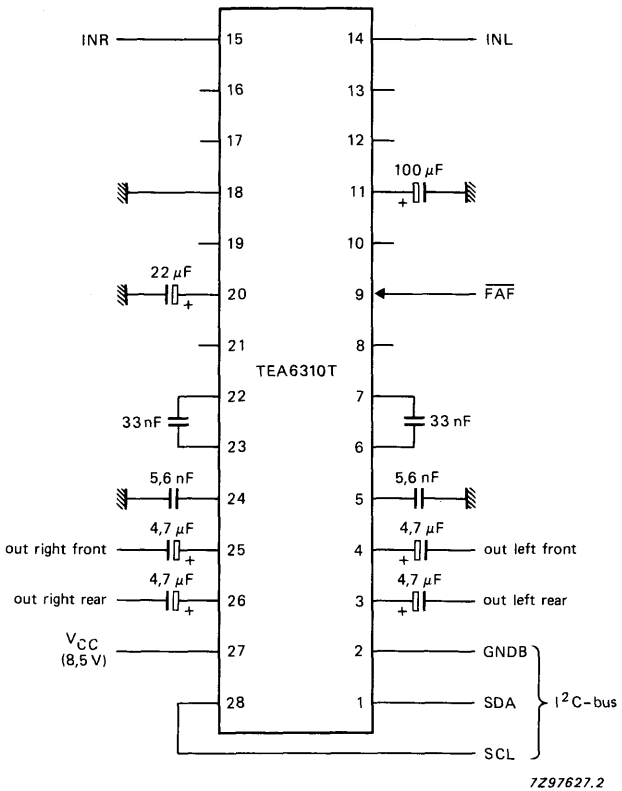


Fig. 10 Test and application circuit.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

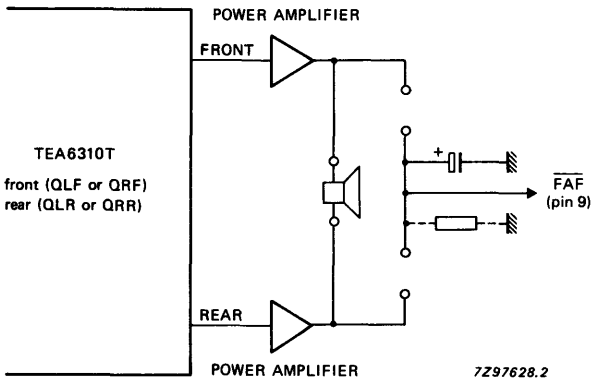


Fig. 11 Automatic FADER control; P_o = 24 W, V_{9-18} = 0 V (FADER disabled).

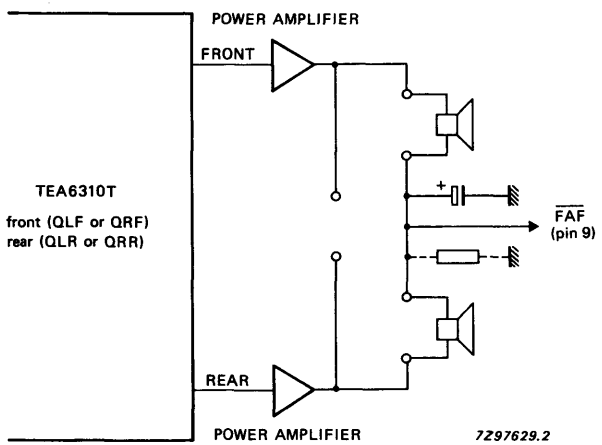


Fig. 12 Automatic FADER control; P_o = 2 x 6 W, V_{9-18} = 7 V (FADER enabled).

RADIO TUNING PLL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The TSA6057/6057T is a bipolar single chip frequency synthesizer manufactured in SUBILO-N technology (components laterally separated by oxide). It performs all the tuning functions of a PLL radio tuning system. The IC is designed for application in all types of radio receivers.

Features

- On-chip AM and FM prescalers with high input sensitivity
- On-chip high performance one input (two output) tuning voltage amplifier for the AM and FM loop filters
- On-chip 2-level current amplifier (charge pump) to adjust the loop gain
- Only one reference oscillator (4 MHz) for both AM and FM
- High speed tuning due to a powerful digital memory phase detector
- 40 kHz output reference frequency for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100)
- Oscillator frequency ranges of: 512 kHz to 30 MHz and 30 MHz to 150 MHz
- Three selectable reference frequencies of 1 kHz, 10 kHz or 25 kHz for both tuning ranges
- Serial 2-wire I²C-bus interface to a microcomputer and one programmable address input
- Software controlled bandswitch output

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 3		$V_{CC1} = V_{3-4}$	4.5	5.0	5.5	V
pin 16		$V_{CC2} = V_{16-4}$	V_{CC1}	8.5	12	V
Supply current	no outputs loaded					
pin 3		I_3	12	20	28	mA
pin 16		I_{16}	0.7	1.0	1.3	mA
Max. input frequency on AM_I		f_{iAM}	30	–	–	MHz
Min. input frequency on AM_I		f_{iAM}	–	–	0.512	MHz
Max. input frequency on FM_I		f_{iFM}	150	–	–	MHz
Min. input frequency on FM_I		f_{iFM}	–	–	30	MHz
Input voltage on AM_I (RMS value)	$V_{iFM} = 0$ V	$V_{iAM(rms)}$	30	–	500	mV
Input voltage on FM_I (RMS value)	$V_{iAM} = 0$ V	$V_{iFM(rms)}$	20	–	300	mV
Total power dissipation		P_{tot}	–	0.14	–	W
Operating ambient temperature range		T_{amb}	−30	–	+ 85	°C

PACKAGE OUTLINES

TSA6057: 16-lead DIL; plastic (SOT38).
TSA6057T: 16-lead minipack; plastic (SO16L; SOT162A).

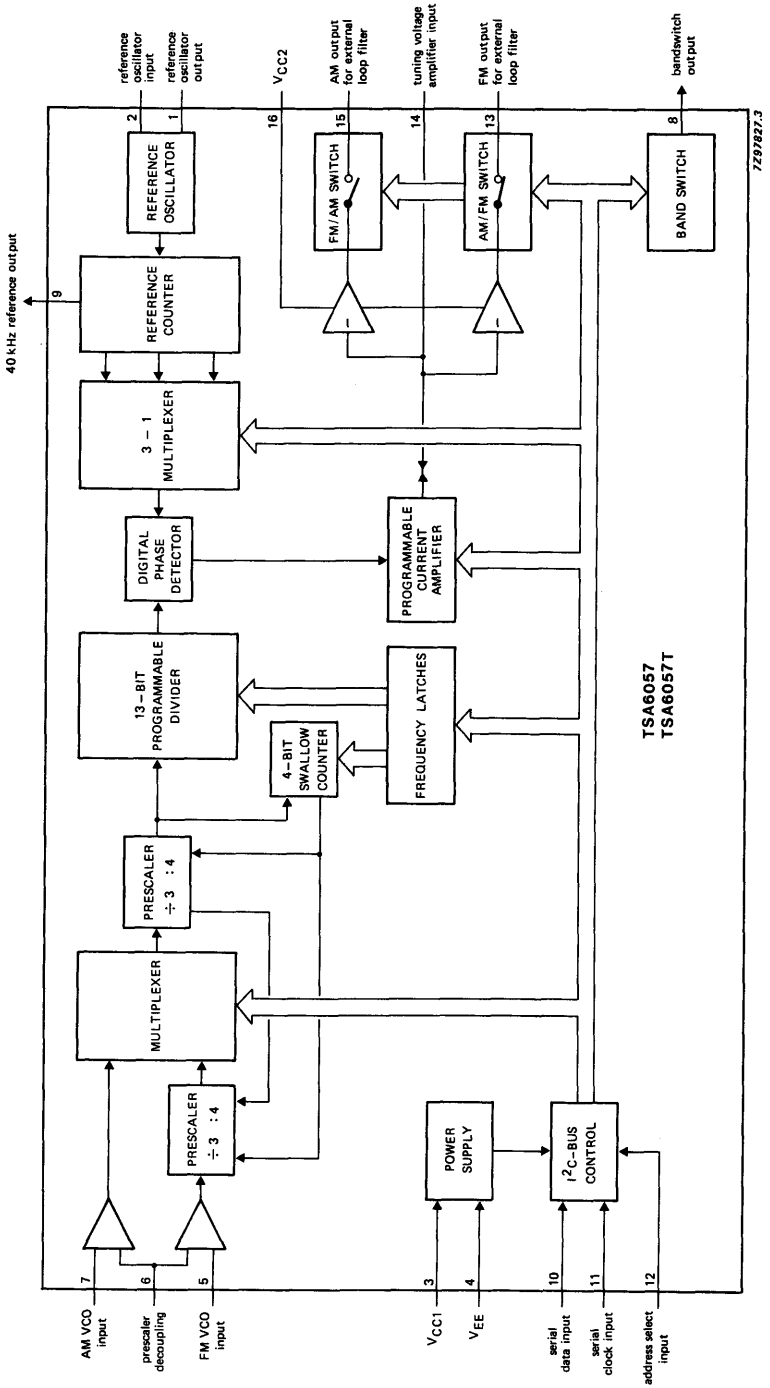


Fig.1 Block diagram.

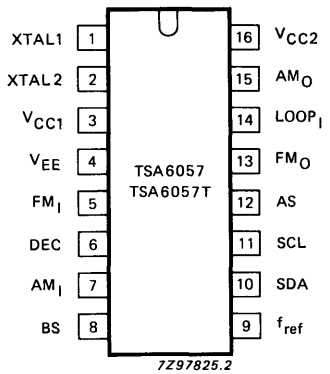


Fig.2 Pinning diagram.

PINNING

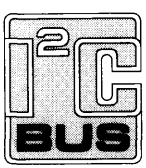
1	XTAL1	reference oscillator output
2	XTAL2	reference oscillator input
3	V_{CC1}	positive supply voltage
4	V_{EE}	ground
5	FM_I	FM VCO input
6	DEC	prescaler decoupling
7	AM_I	AM VCO input
8	BS	bandswitch output
9	f_{ref}	40 kHz reference output
10	SDA	serial data input (I²C-bus)
11	SCL	serial clock input (I²C-bus)
12	AS	address select input (I²C-bus)
13	FM_O	FM output for external loop filter
14	$LOOP_I$	tuning voltage amplifier input
15	AM_O	AM output for external loop filter
16	V_{CC2}	positive supply voltage

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TSA6057/6057T contains the following parts and facilities:

- Separate input amplifiers for the AM and FM VCO-signals.
- A prescaler with the divisors 3:4 on AM and 15:16 on FM, a multiplexer to select AM or FM and a 4-bit programmable swallow counter.
- A 13-bit programmable counter.
- A digital memory phase detector.
- A reference frequency channel comprised of a 4 MHz crystal oscillator followed by a reference counter. The reference frequency can be 1 kHz, 10 kHz or 25 kHz and is applied to the digital memory phase detector. The reference counter also outputs a 40 kHz reference frequency to pin 9 for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100).
- A programmable current amplifier (charge pump) which consists of a 5 μA and a 450 μA current source. This allows adjustment of loop gain, thus providing high current-high speed tuning and low current-stable tuning.
- A one input – two output tuning voltage amplifier. One output is connected to the external AM loop filter and the other output to the external FM loop filter. Under software control, the AM output is switched to a high impedance state by the FM/AM switch in the FM position and the FM output is switched to a high impedance state by the AM/FM switch in the AM position. The outputs can deliver a tuning voltage of up to 10.5 V.
- An I²C-bus interface with data latches and control logic. The I²C-bus is intended for communication between microcontrollers and different ICs or modules. Detailed information on the I²C-bus specification is available on request.
- A software-controlled bandswitch output.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

FUNCTIONAL DESCRIPTION (continued)

Controls

The TSA6057/6057T is controlled via the 2-wire I²C-bus. For programming there is one module address, a logic 0 R/W bit, a subaddress byte and four data bytes. The subaddress determines which one of the four data bytes is transmitted first. The module address contains a programmable address bit (D1) which with address select input AS (pin 12) makes it possible to operate two TSA6057s in one system.

The auto increment facility of the I²C-bus allows programming of the TSA6057/6057T within one transmission (address + subaddress + 4 data bytes).

- The TSA6057/6057T can also be partially programmed. Transmission must then be ended by a stop condition.

The bit organization of the 4 data bytes is shown in Fig.3 and are described in sections (a) to (f).

(a) The bits S0 to S16 (DB0: D7-D1; DB1: D7-D0; DB2: D1-D0) together with bit FM/AM (DB2: D5) are used to set the divisor of the input frequency at inputs AM_I (pin 7) or FM_I (pin 5). If the system is in lock the following is valid:

FM/$\overline{AM}$	input frequency (f_i)	input
0	$(S0 \times 2^0 + S1 \times 2^1 \ldots\ldots + S13 \times 2^{13} + S14 \times 2^{14}) \times f_{ref}$	AM_I
1	$(S0 \times 2^0 + S1 \times 2^1 \ldots\ldots + S15 \times 2^{15} + S16 \times 2^{16}) \times f_{ref}$	FM_I

Where

The minimum dividing ratio for AM mode is $2^6 = 64$
The minimum dividing ratio for FM mode is $2^8 = 256$

(b) The bit CP is used to control the charge pump current (DB0: D0).

CP	current
0	low
1	high

(c) The bits REF1 and REF2 are used to set the reference frequency applied to the phase detector (DB2: D7-D6).

REF1	REF2	frequency (kHz)
0	0	1
0	1	10
1	0	25
1	1	none

(d) The bit $\overline{FM}$/AM OPAMP controls the switch AM/FM; FM/AM in the tuning voltage amplifier output circuitry (DB2: D4).

$\overline{FM}$/AM OPAMP	switch FM/AM	switch AM/FM
1	closed	open
0	open	closed

(e) The bit BS controls the open collector bandswitch output (DB2: D2).

BS	bandswitch output
1	sink current
0	floating

(f) The data byte DB3 must be set to 0 . . . . . 0. It is also used for test purposes.

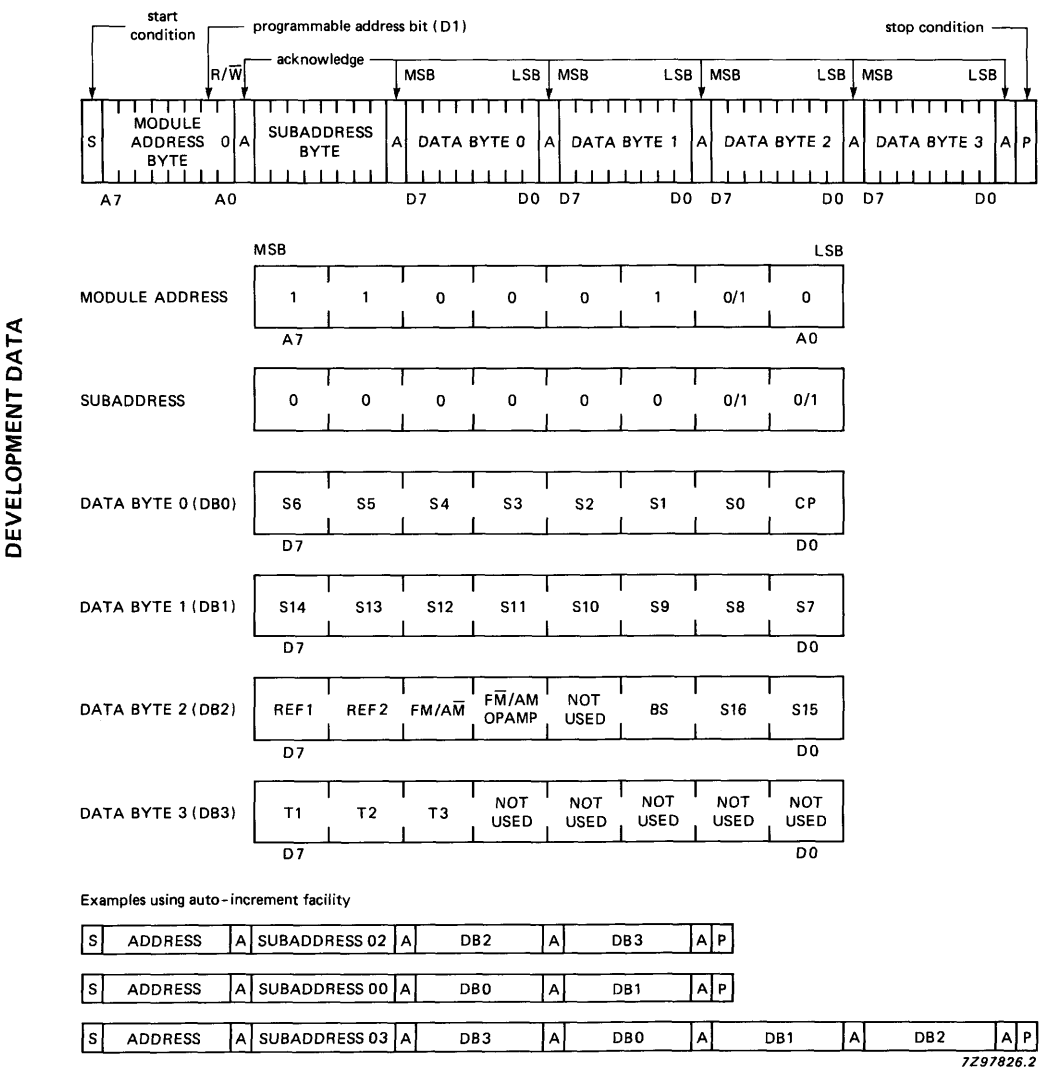


Fig.3 Bit organization.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	$V_{CC1} = V_{3-4}$	−0.3	5.5	V
Supply voltage (pin 16)	$V_{CC2} = V_{16-4}$	V_{CC1}	12.5	V
Total power dissipation	P_{tot}	–	0.85	W
Operating ambient temperature	T_{amb}	−30	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{CC1} = 5 V; V_{CC2} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		V_{CC1}	4.5	5.0	5.5	V
Supply voltage (pin 16)		V_{CC2}	V_{CC1}	8.5	12	V
Supply current	no outputs loaded					
pin 3		I_{CC1}	12	20	28	mA
pin 16		I_{CC2}	0.7	1.0	1.3	mA
I²C-bus inputs (SDA; SCL)						
Input voltage HIGH		V_{IH}	3.0	–	5.0	V
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input current HIGH		I_{IH}	–	–	10	μA
Input current LOW		I_{IL}	–	–	10	μA
SDA output	open collector					
Output voltage LOW	I_{OL} = 3.0 mA	V_{OL}	–	–	0.4	V
AS input						
Input voltage HIGH		V_{IH}	3.0	–	5.0	V
Input voltage LOW		V_{IL}	−0.3	–	1.0	V
Input current HIGH		I_{IH}	–	–	10	μA
Input current LOW		I_{IL}	–	–	10	μA
RF input (AM; FM)						
Max. input frequency on AM_I		f_{iAM}	30	–	–	MHz
Min. input frequency on AM_I		f_{iAM}	–	–	0.512	MHz
Max. input frequency on FM_I		f_{iFM}	150	–	–	MHz
Min. input frequency on FM_I		f_{iFM}	–	–	30	MHz
Input voltage on AM_I (RMS value)	V_{iFM} = 0 V measured in Fig.4	$V_{iAM(rms)}$	30	–	500	mV
Input impedance AM_I						
resistance		R_{AM}	–	5.9	–	kΩ
capacitance		C_{AM}	–	2	–	pF

parameter	conditions	symbol	min.	typ.	max.	unit
RF input (continued)						
Input voltage on FM_I (RMS value)	V_{iAM} = 0 V measured in Fig.4	$V_{iFM(rms)}$	20	–	300	mV
Input impedance FM_I						
resistance		R_{FM}	–	3.6	–	kΩ
capacitance		C_{FM}	–	2	–	pF
Oscillator (XTAL1; XTAL2)						
Crystal resonance resistance (4 MHz)	see Fig.5	R_{XTAL}	–	–	150	Ω
Programmable charge pump						
Output current to loop filter						
bit CP = logic 0		I_{chp}	3	5	7	μA
bit CP = logic 1		I_{chp}	400	500	600	μA
Ripple rejection	f_{ripple} = 100 Hz					
20 log $\Delta V_{CC1}/\Delta V_O$		RR	40	50	–	dB
20 log $\Delta V_{CC2}/\Delta V_O$		RR	40	50	–	dB
Bandswitch output (pin 8)						
Output voltage HIGH		V_{OH}	–	–	12	V
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	–	–	0.8	V
Output leakage current	V_{OH} = 12 V	I_{LO}	–	–	10	μA
Reference frequency output (pin 9)						
Output frequency	4 MHz crystal	f_{ref}	–	40	–	kHz
Output voltage HIGH	I_{source} = 5 μA	V_{OH}	1.2	1.4	1.7	V
Output voltage LOW		V_{OL}	–	0.1	0.2	V
Tuning voltage amplifier outputs						
AM output (pin 15)						
max. output voltage	I_{source} = 0.5 mA	$V_{O(max)}$	V_{CC2} −1.5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0.8	V
max. output source current		I_{source}	0.5	–	–	mA
max. output sink current		I_{sink}	1.0	–	–	mA
FM output (pin 13)						
max. output voltage	I_{source} = 0.5 mA	$V_{O(max)}$	V_{CC2} −1.5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0.8	V
max. output source current		I_{source}	0.5	–	–	mA
max. output sink current		I_{sink}	1.0	–	–	mA
Impedance of switched off output		$Z_{O(off)}$	5	–	–	MΩ
Input bias current (absolute value)		I_{bias}	–	1	5	nA

DEVELOPMENT DATA

SENSITIVITY MEASUREMENT

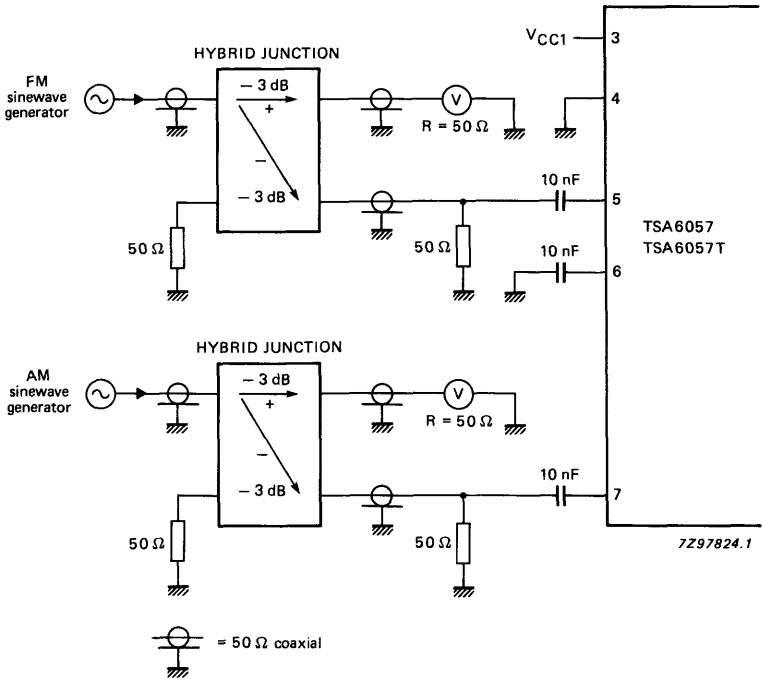


Fig.4 Prescaler input sensitivity.

APPLICATION INFORMATION

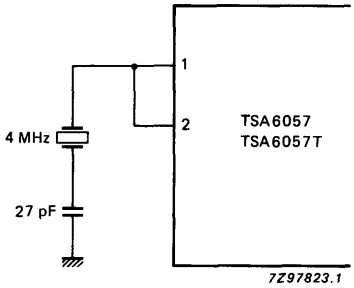


Fig.5 Crystal connection (4 MHz).

DEVELOPMENT DATA

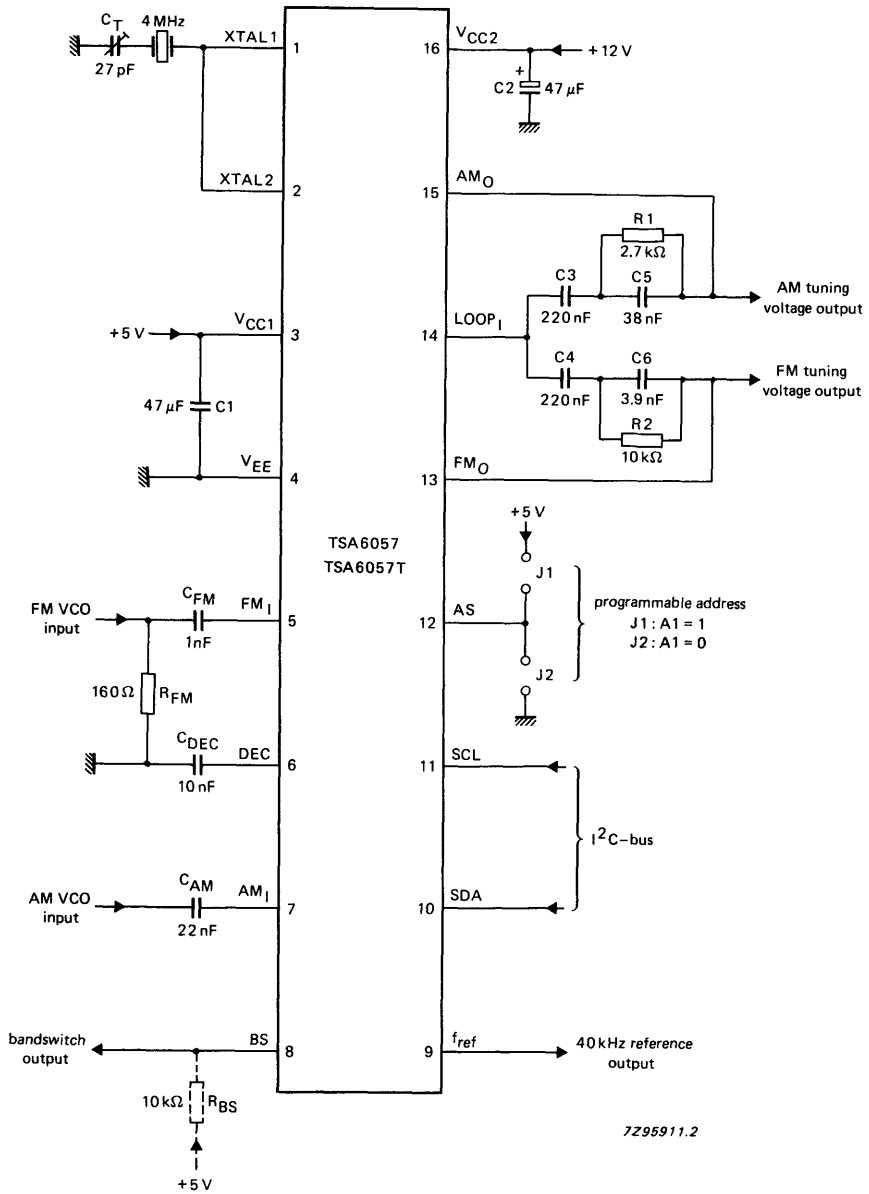


Fig.6 Application diagram

μA758
FM Stereo Multiplex Decoder, Phase-Locked Loop

Product Specification

DESCRIPTION

The μA758 is a monolithic phase-locked loop FM stereo multiplex decoder. The device decodes an FM stereo multiplex signal into right and left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. The device includes automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The μA758 operates over a large voltage range and requires a minimum number of external components. A simple setting of an external potentiometer adjusts the oscillator frequency. No coils are required.

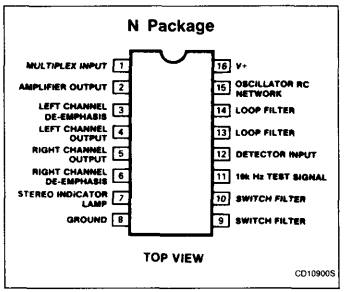
FEATURES

- **45dB channel separation**
- **Automatic stereo/mono switching**
- **70dB SCA rejection**
- **10V to 16V supply range**
- **High impedance input — low impedance output**

APPLICATIONS

- **Stereo decoder for radios**

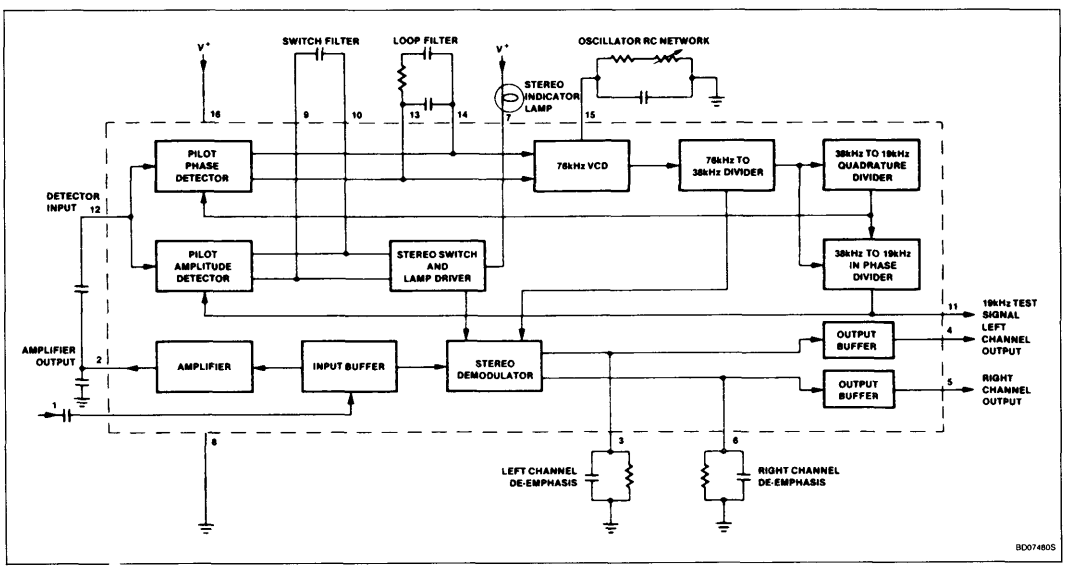
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	−40°C to +85°C	μA758N

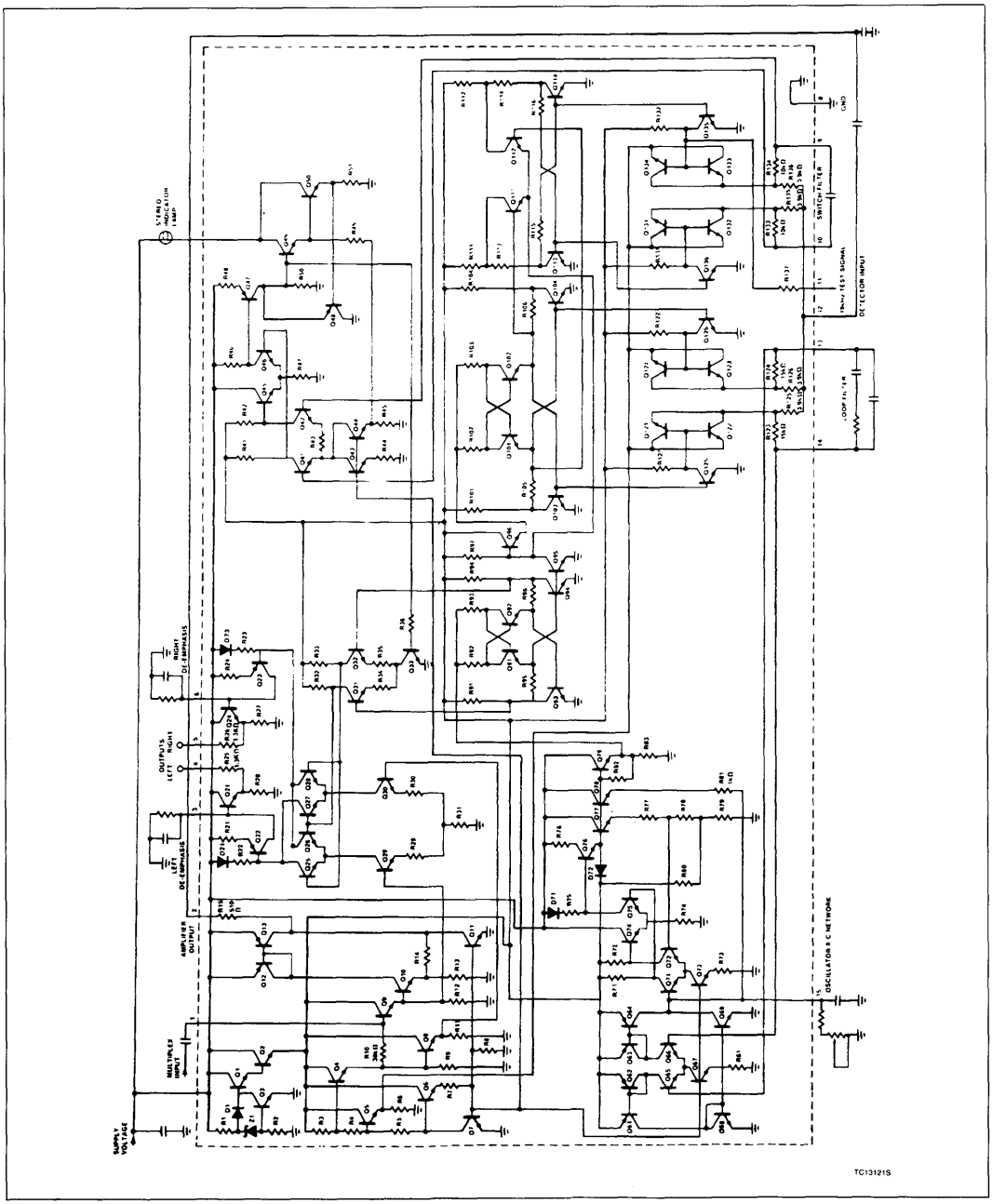
BLOCK DIAGRAM



FM Stereo Multiplex Decoder, Phase-Locked Loop

μA758

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+18	V
V_{CC}	Supply voltage ($\leqslant$ 15 seconds)	+22	V
	Voltage at lamp driver terminal (Lamp OFF)	+22	V
P_D	Internal power dissipation	730	mW
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +125	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V+ = +12V, 19kHz pilot level = 30mV$_{RMS}$, multiplex signal (L = R, pilot OFF) = 300V$_{RMS}$, modulation frequency = 400Hz or 1Hz, Test Circuit 1, unless otherwise specified .

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
I_{CC} I_L	Supply current Maximum available lamp current	Lamp OFF	 75	31 150	38	mA mA
V_7	Voltage at lamp driver terminal	Lamp = 50mA		1.3	1.8	V
R_{IN}	Input resistance		20	35		kΩ
R_{OUT}	Output resistance		0.9	1.3	2.0	kΩ

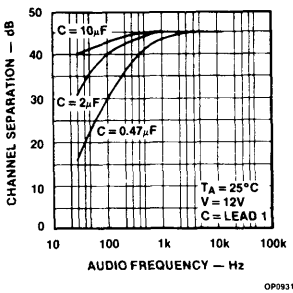
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
$\Delta(V_4 \& V_5)$	DC voltage shift at either output terminal	Stereo to mono operation		30	150	mV
PSRR	Power supply ripple rejection	200Hz, 200mV$_{RMS}$	35			dB
SEP	Channel separation	100Hz 400Hz 10kHz	30	40 45 45		dB dB dB
BAL	Channel balance			0.3	1.5	dB
A_V	Voltage gain	1kHz	0.5	0.9	1.4	V/V
	Pilot input level	Lamp turn-on Lamp turn-off	 2.0	18 7.0	25	mV$_{RMS}$ mV$_{RMS}$
	Pilot input level hysteresis	Lamp turn-off to turn-on	3.0	7.0		dB
THD	Capture range Total harmonic distortion	Multiplex level = 600mV$_{RMS}$ pilot OFF	2.0	4.0 0.4	6.0 1.0	% %
	19kHz rejection 38kHz rejection SCA rejection[1]		25 25	35 45 70		dB dB dB
VCO	Tuning resistance[2]		21.0	23.3	25.5	kΩ
VCO	Frequency drift	0°C $\leqslant T_A \leqslant$ 25°C 25°C $\leqslant T_A \leqslant$ 70°C		+0.1 −0.4	±2 ±2	% %

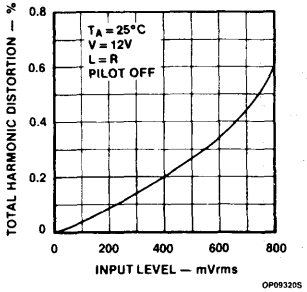
NOTES:
1. Measured with a stereo composite consistency of 80% stereo. 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.
2. Total resistance from Pin 15 to ground, in Test Circuit, required to set reference frequency at Pin 11 to 19kHz ± 10Hz.

TYPICAL PERFORMANCE CHARACTERISTICS

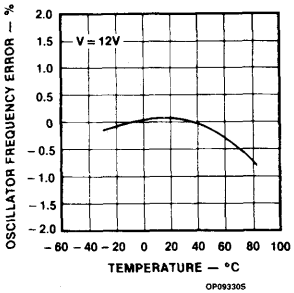
Channel Separation vs Audio Frequency



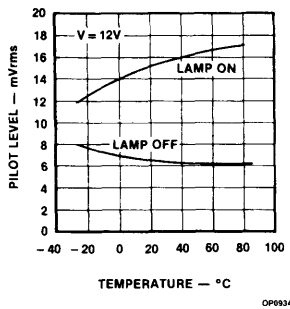
Harmonic Distortion vs Input Level



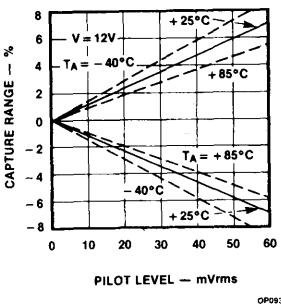
Oscillator Free-Running Frequency Error vs Ambient Temperature



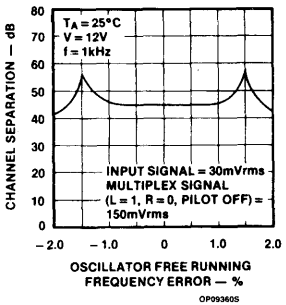
Lamp Turn-On & Turn-Off Sensitivity vs Ambient Temperature



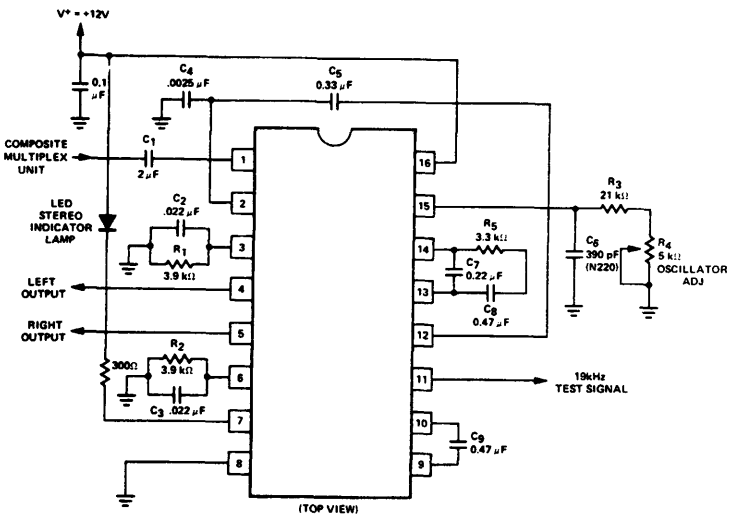
Capture Ranges vs Pilot Level



Channel Separation vs Oscillator Free-Running Frequency Error



TEST CIRCUIT AND TYPICAL APPLICATION



NOTE:
Tolerance on resistors is ±5% and tolerance on capacitors is ±20%, unless otherwise specified. C_1 *tolerance* = +100%; −20%, C_6 *tolerance* = ±1% *in test circuit and* ±5% *in typical applications.* R_3 *tolerance* = ±1%, R_4 *tolerance* = ±10%, R_1 *and* R_2 *tolerance* = ±1% *in Test Circuit and* ±5% *in Typical Application.*

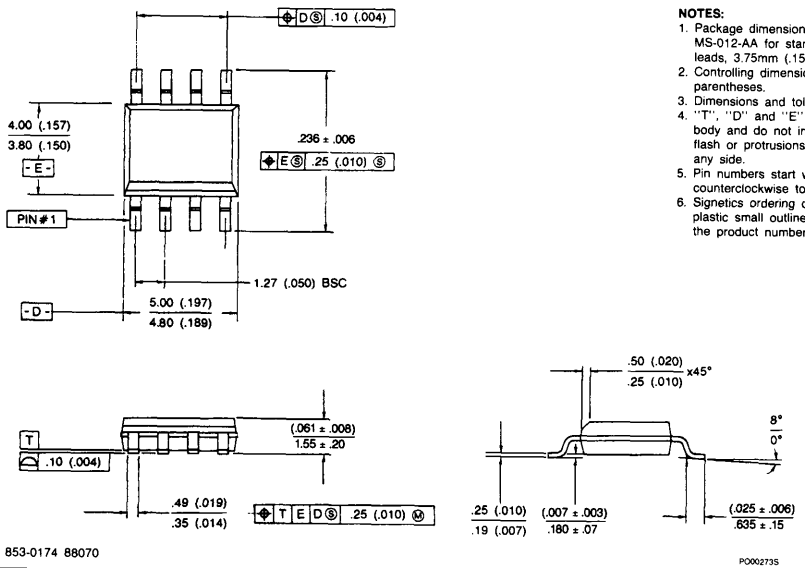
PACKAGE INFORMATION

Package outlines

Soldering

Package outlines for prefixes:
CA, MC, NE, SA, SE, and μA

8-PIN PLASTIC SO (D PACKAGE)

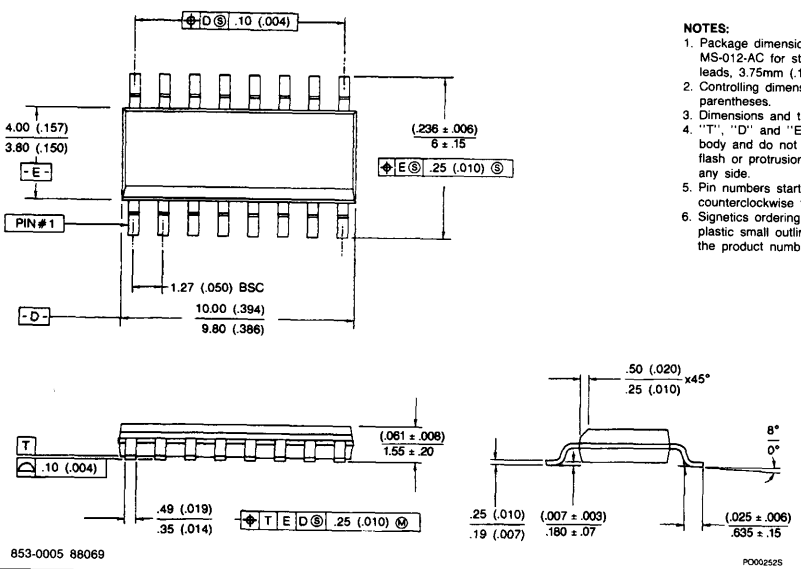


853-0174 88070

PO00273S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16-PIN PLASTIC SO (D PACKAGE)

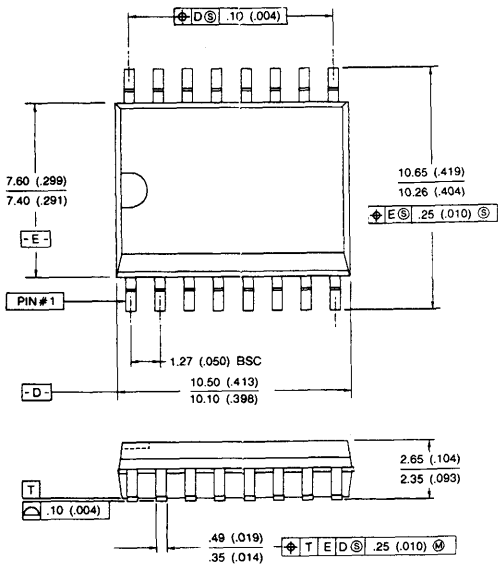


853-0005 88069

PO00252S

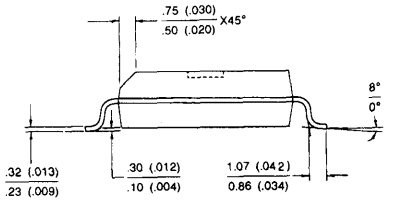
NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16-PIN PLASTIC SOL (D PACKAGE)



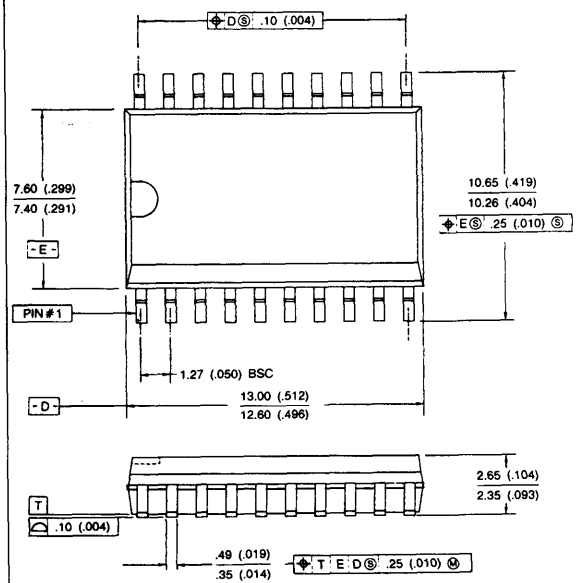
853-0171 81218

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.



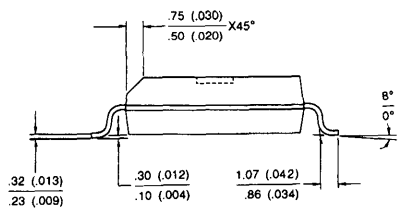
PO00241S

20-PIN PLASTIC SOL (D PACKAGE)



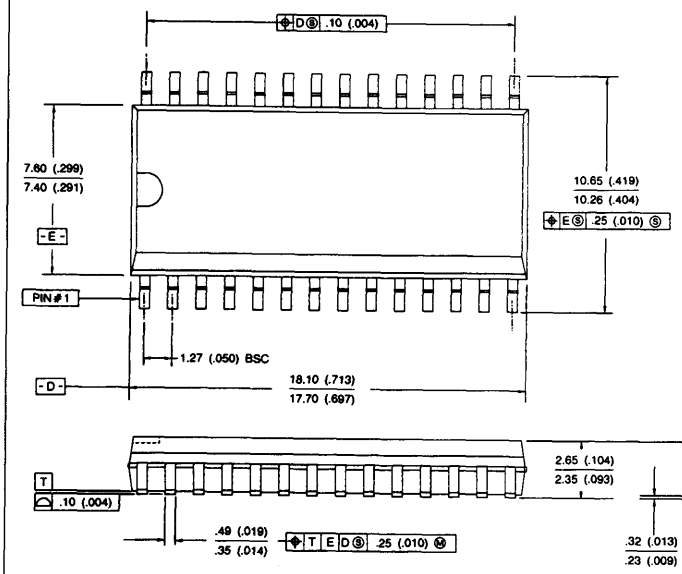
853-0172 81219

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.



PO00231S

28-PIN PLASTIC SOL (D PACKAGE)

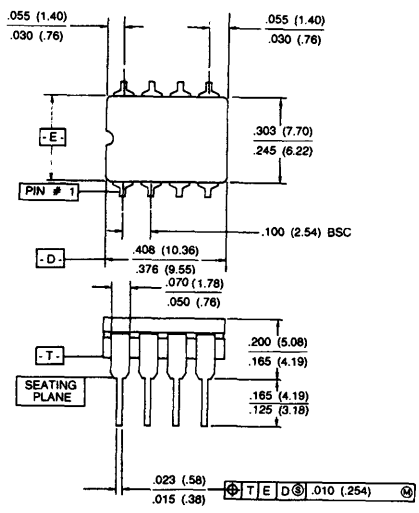


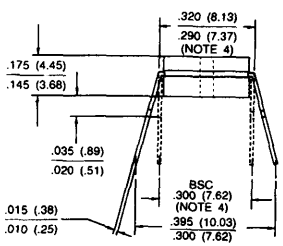
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

853-0006 81217

P000212S

8-PIN CERDIP (FE PACKAGE)



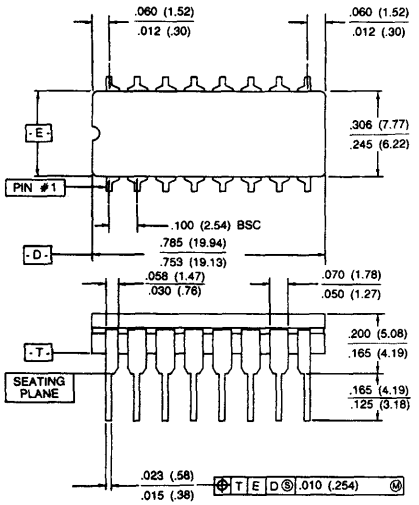


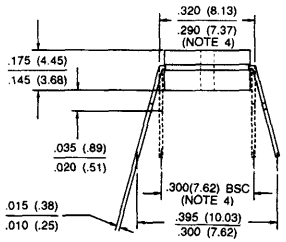
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

853-0580 81594

P000480S

16-PIN CERDIP (F PACKAGE)



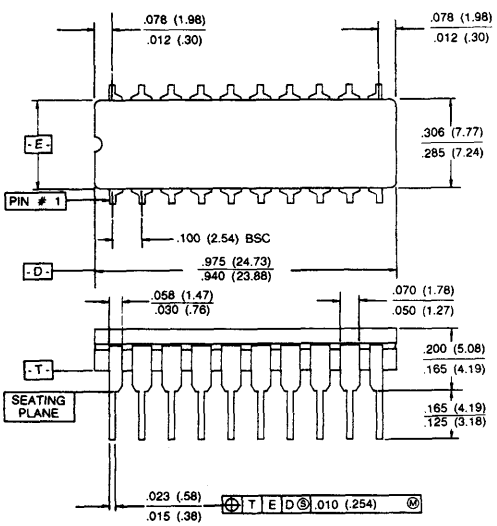


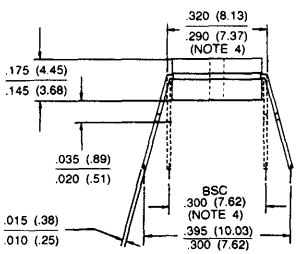
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

853-0582 81594

PO00490S

20-PIN CERDIP (F PACKAGE)



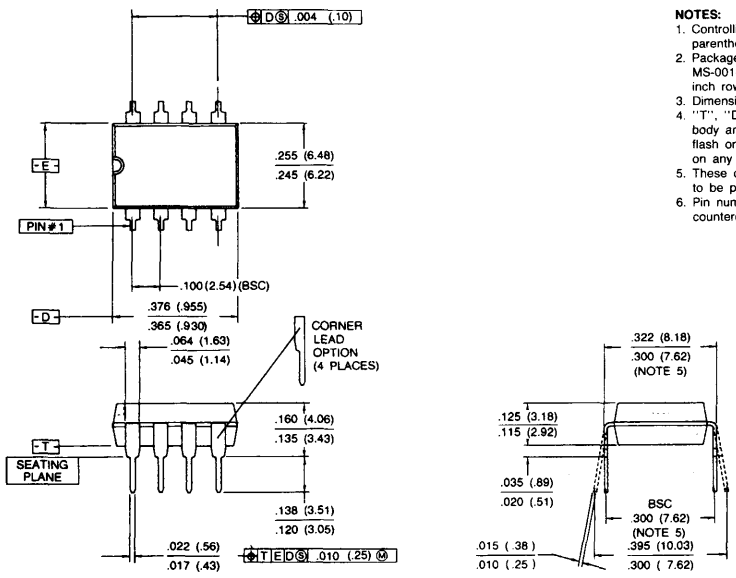


NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

853-0584 81594

PO00430S

8-PIN PLASTIC PDIP (N PACKAGE)

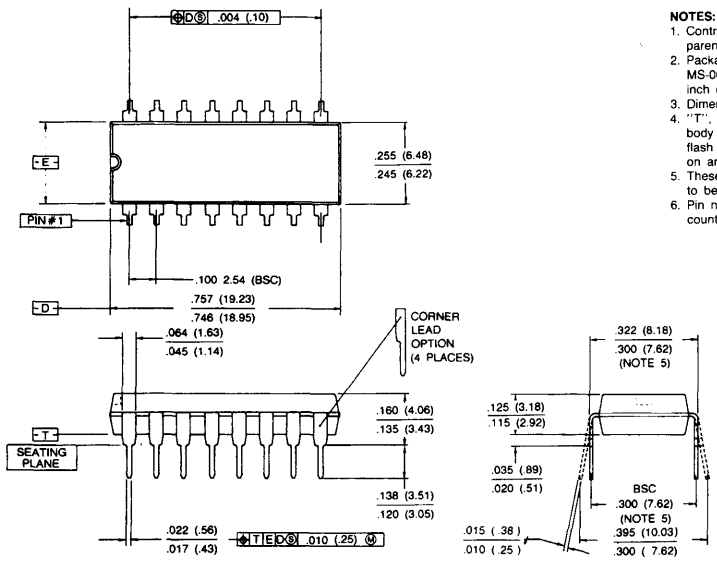


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and *do not include mold flash or protrusions.* Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

853-0404 81230

PO00312S

16-PIN PLASTIC DIP (N PACKAGE)

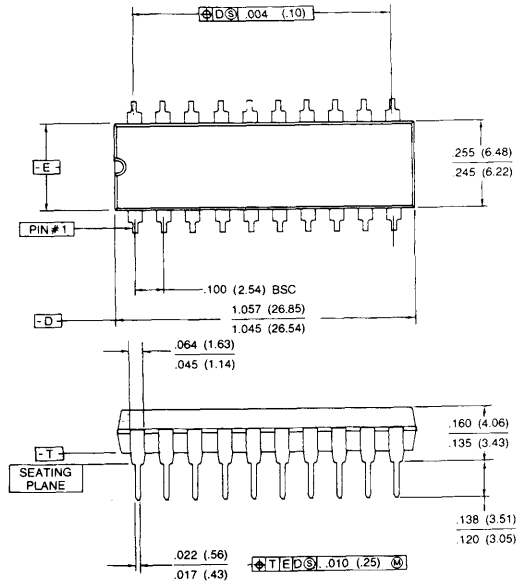


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

853-0406 81232

PO00280S

20-PIN PLASTIC DIP (N PACKAGE)

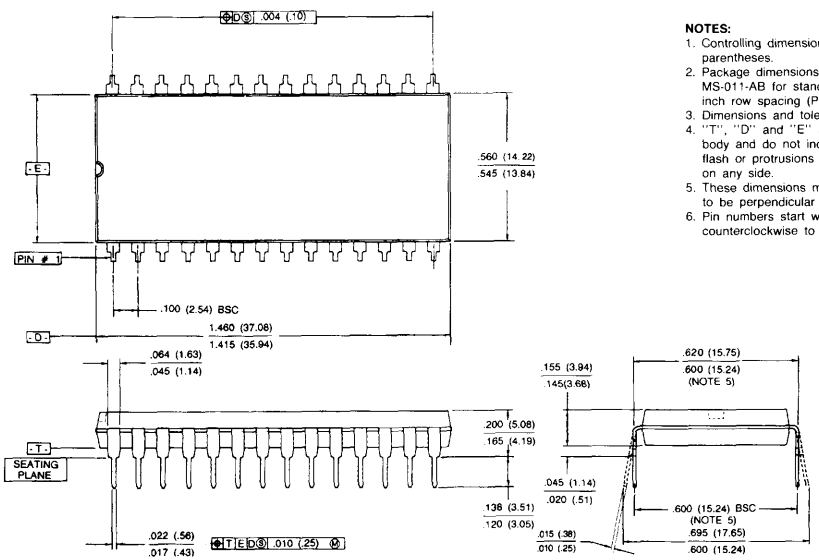


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

853-0408 81234

PO00290S

28-PIN PLASTIC DIP (N PACKAGE)



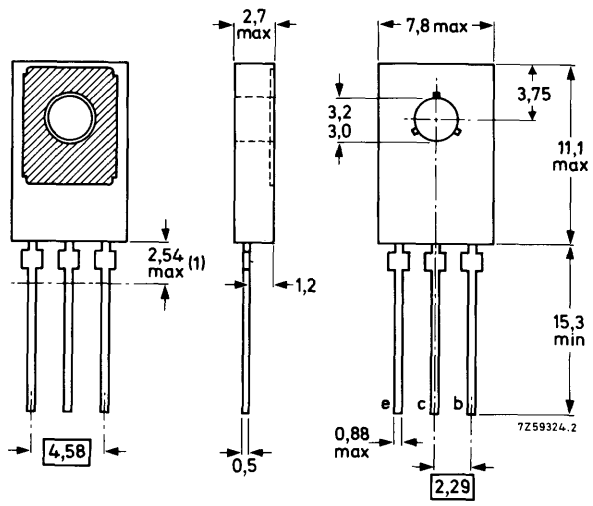
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AB for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 28 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.

853-0413 84099

PO00372S

Package outlines for prefixes:
HEF, MAB, MAF, OM, PCA, PCB, PCF,
PNA, SAA, SAD, SAF, TDA, TDB, TDD, TEA and TSA

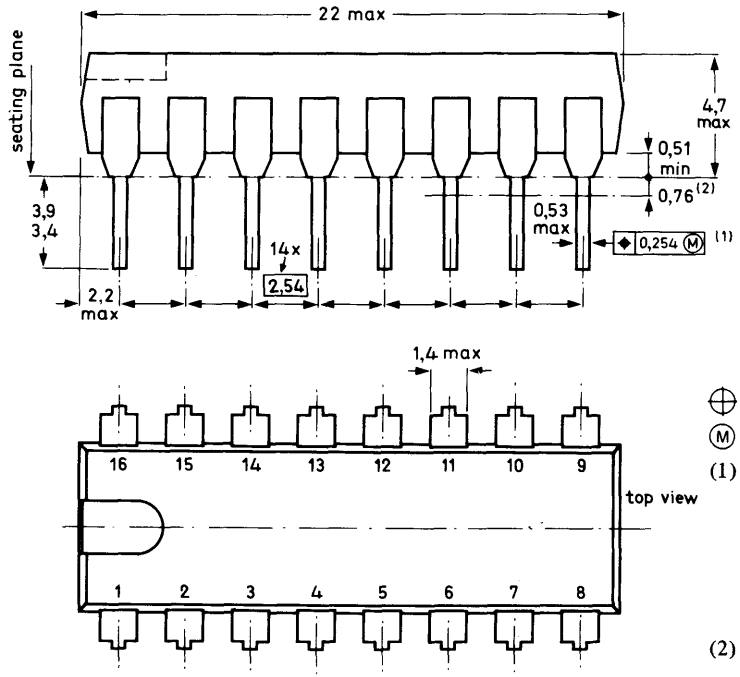
3-LEAD SINGLE IN-LINE; PLASTIC WITH HEATSINK (SOT32)



(1) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (SOT38)



Dimensions in mm

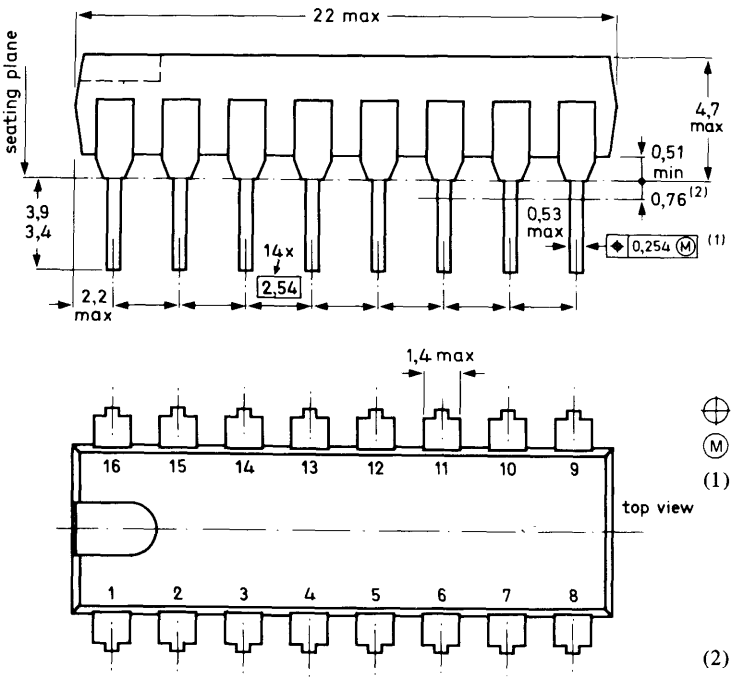
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT38)



⊕ Positional accuracy.

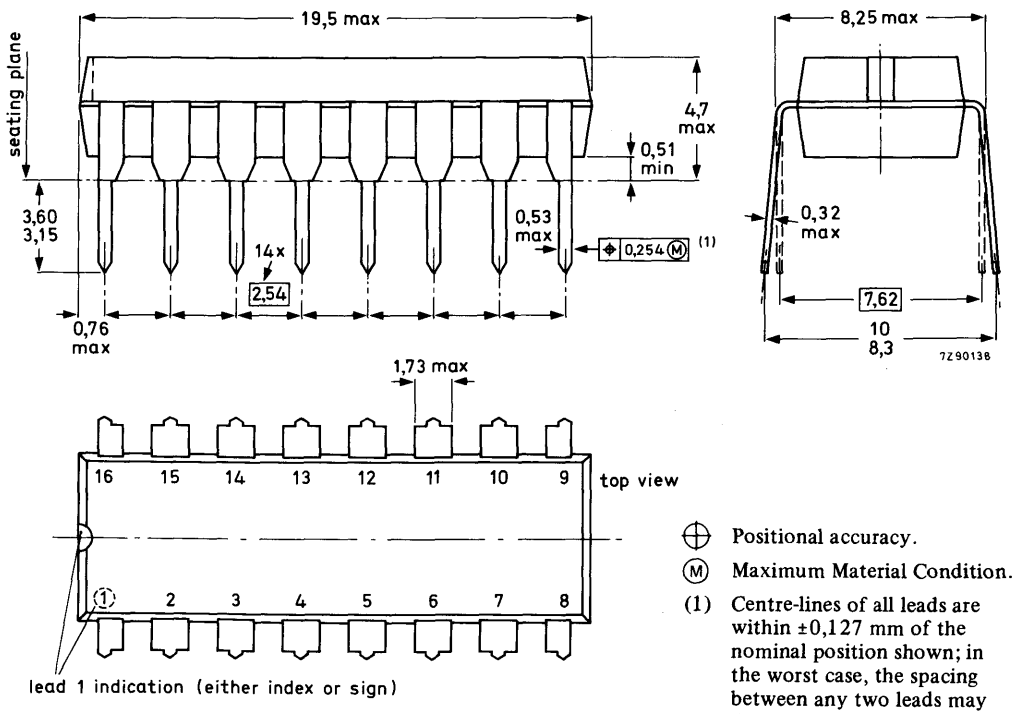
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (SOT38D)



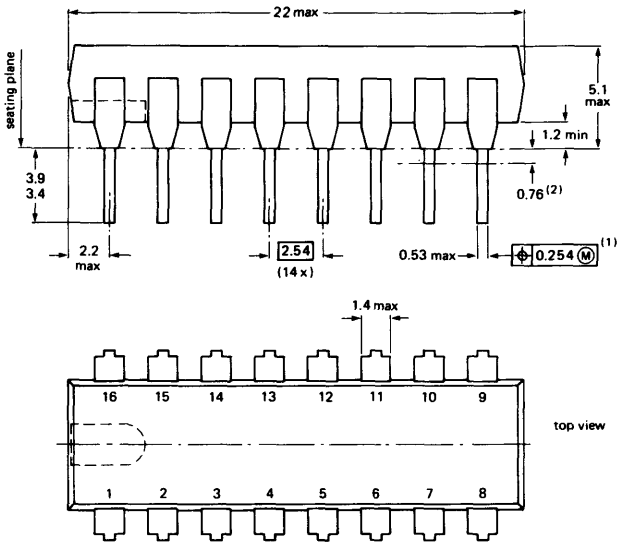
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (OPPOSITE BENT LEADS) (SOT38WBE)

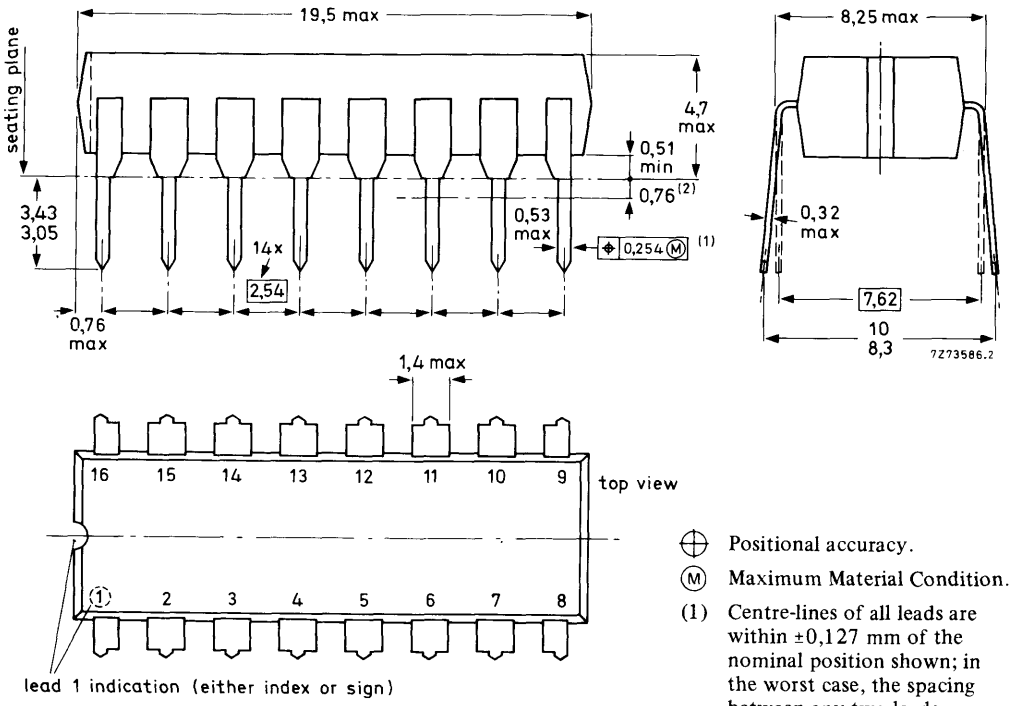


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (SOT38Z)



⊕ Positional accuracy.

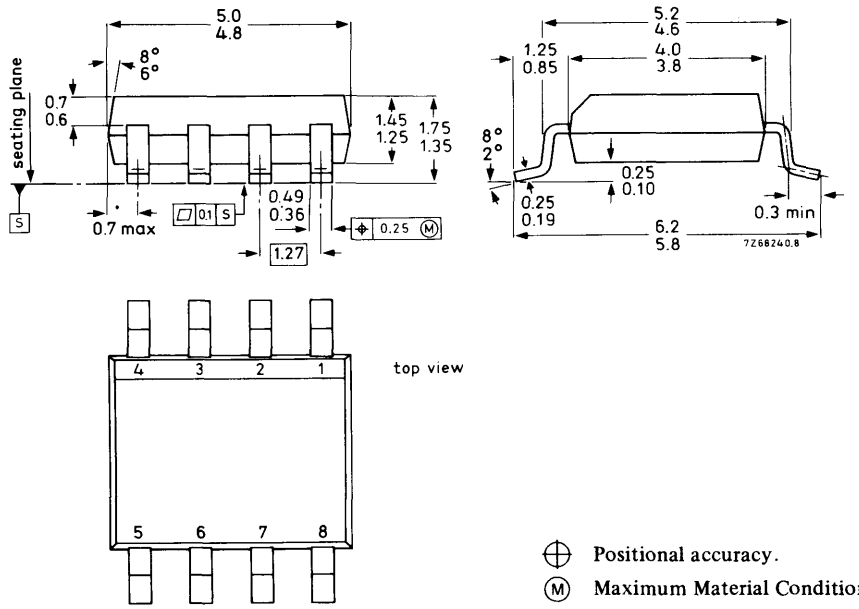
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8; SOT96A)

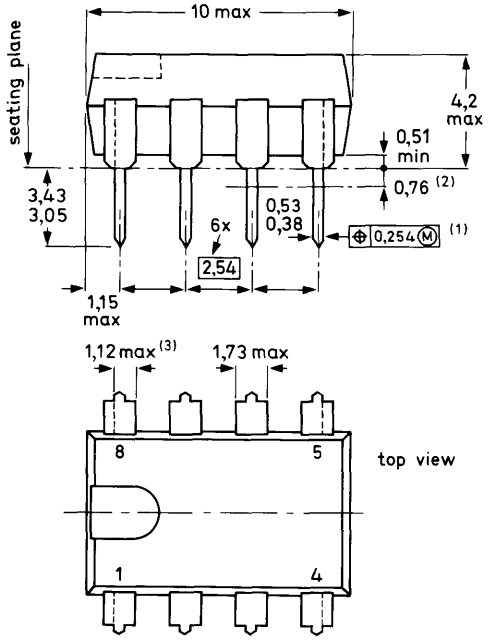


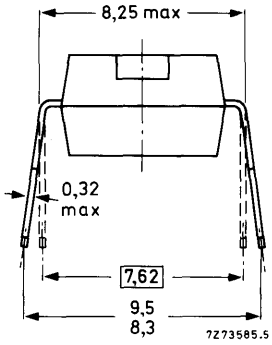
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD DUAL IN-LINE; PLASTIC (SOT97)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

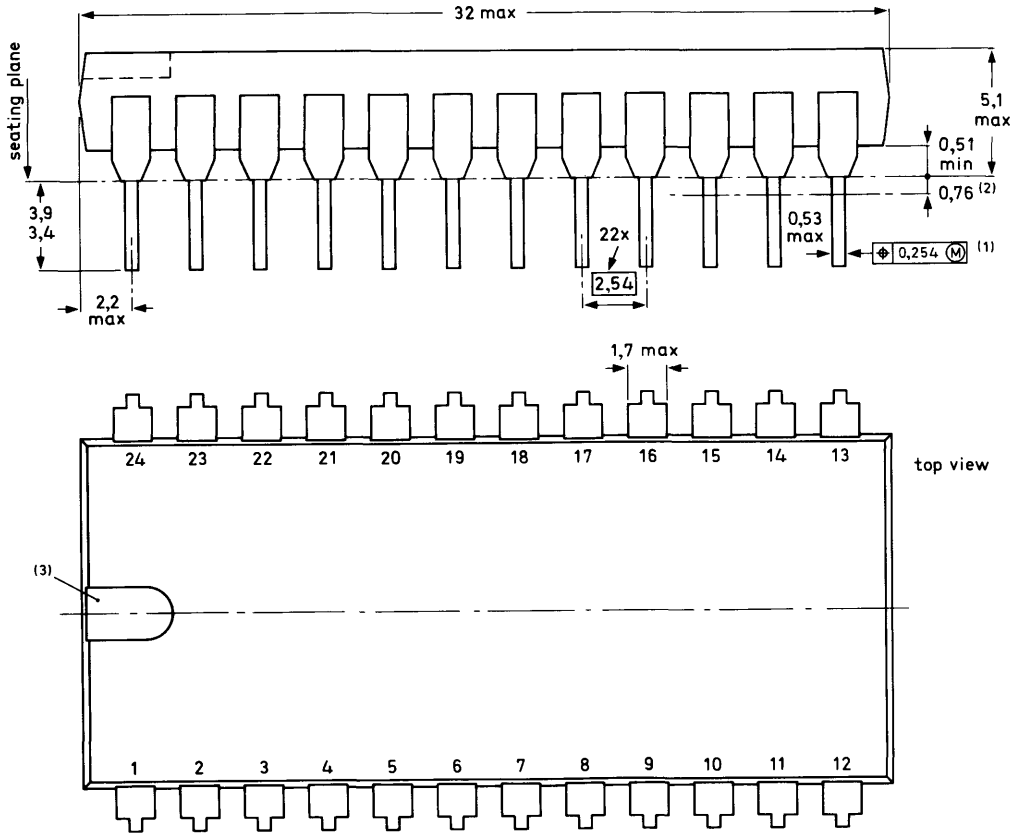
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC (SOT101A, B, F, G, L)



Dimensions in mm

⊕ Positional accuracy.

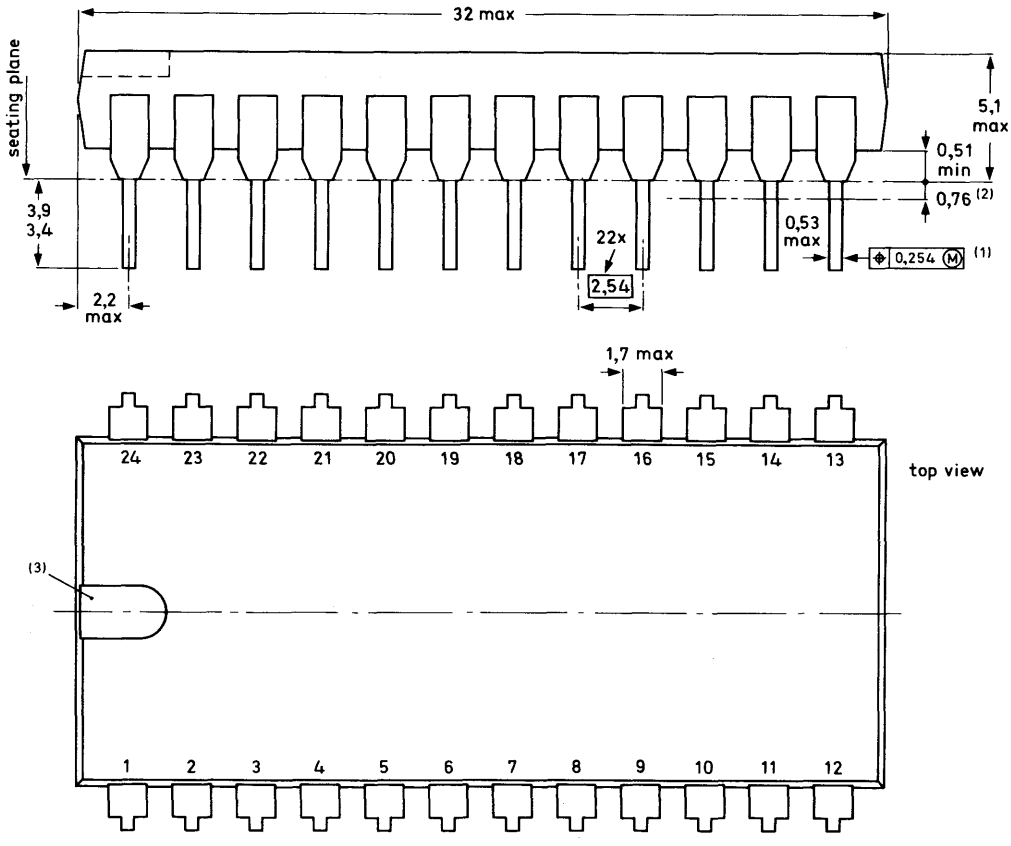
Ⓜ Maximum Material Condition.

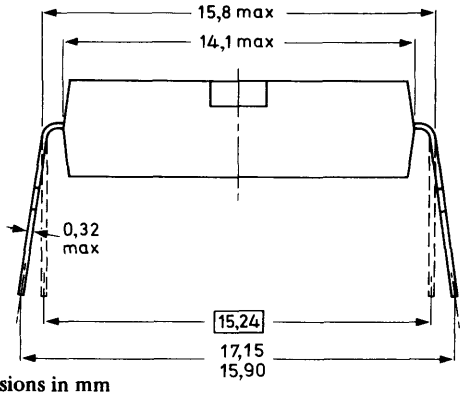
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

24-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT101A, B, F, G, L)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

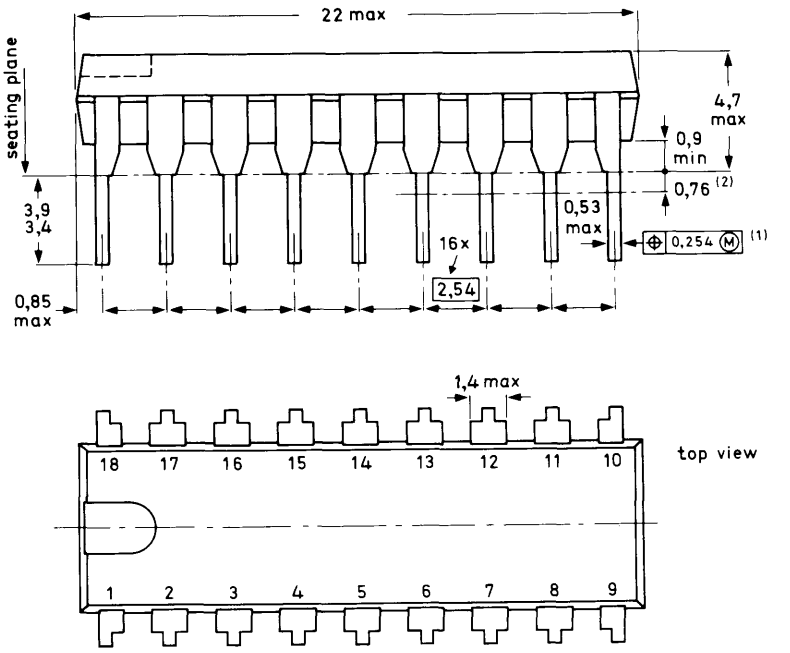
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT102)



⊕ Positional accuracy.

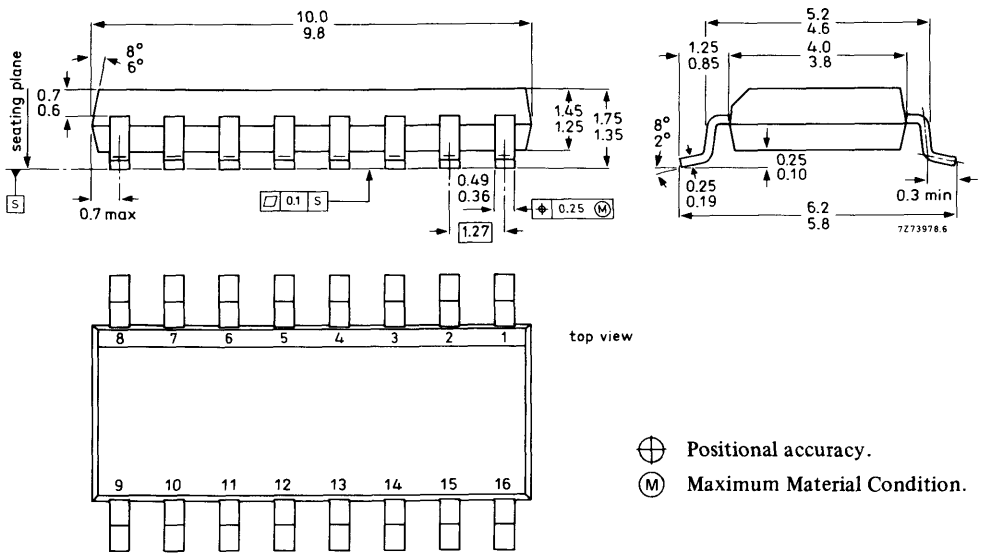
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16; SOT109A)

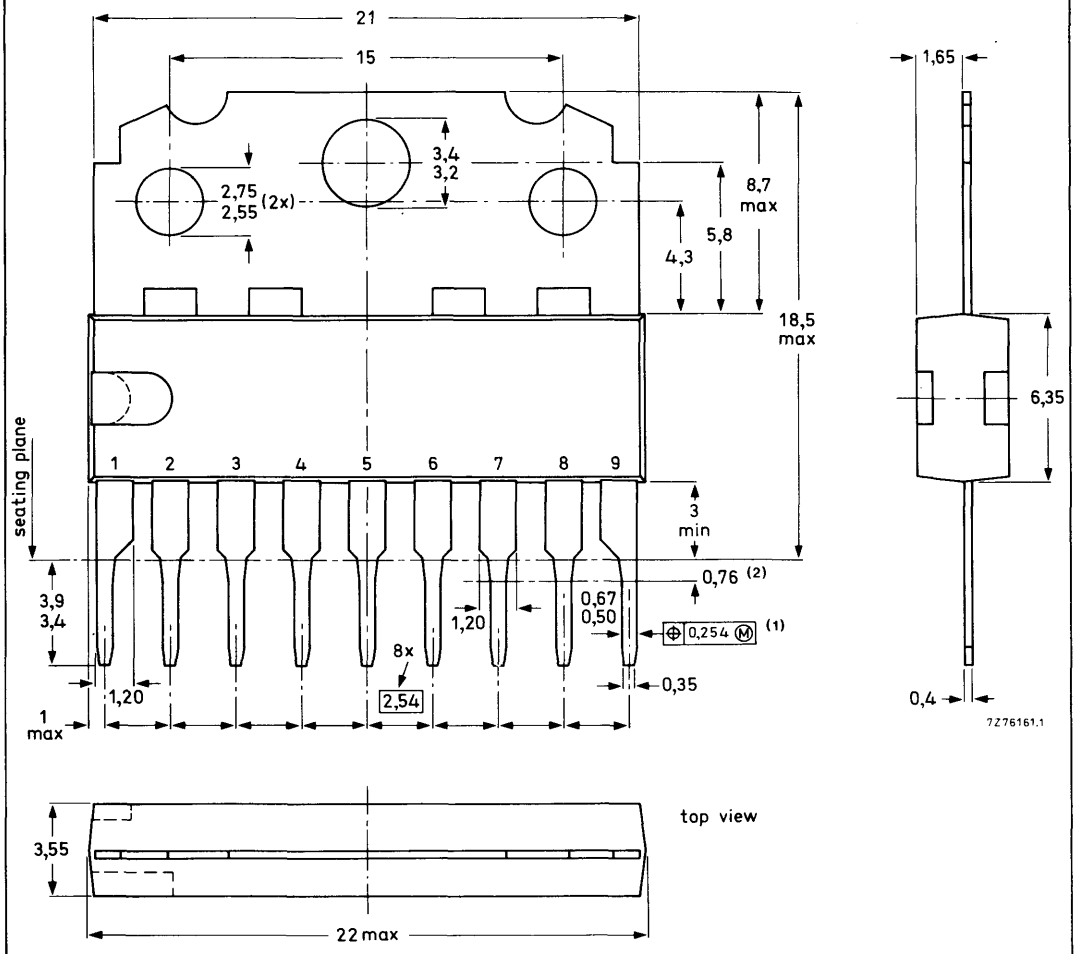


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC (SOT110B)



⊕ Positional accuracy.

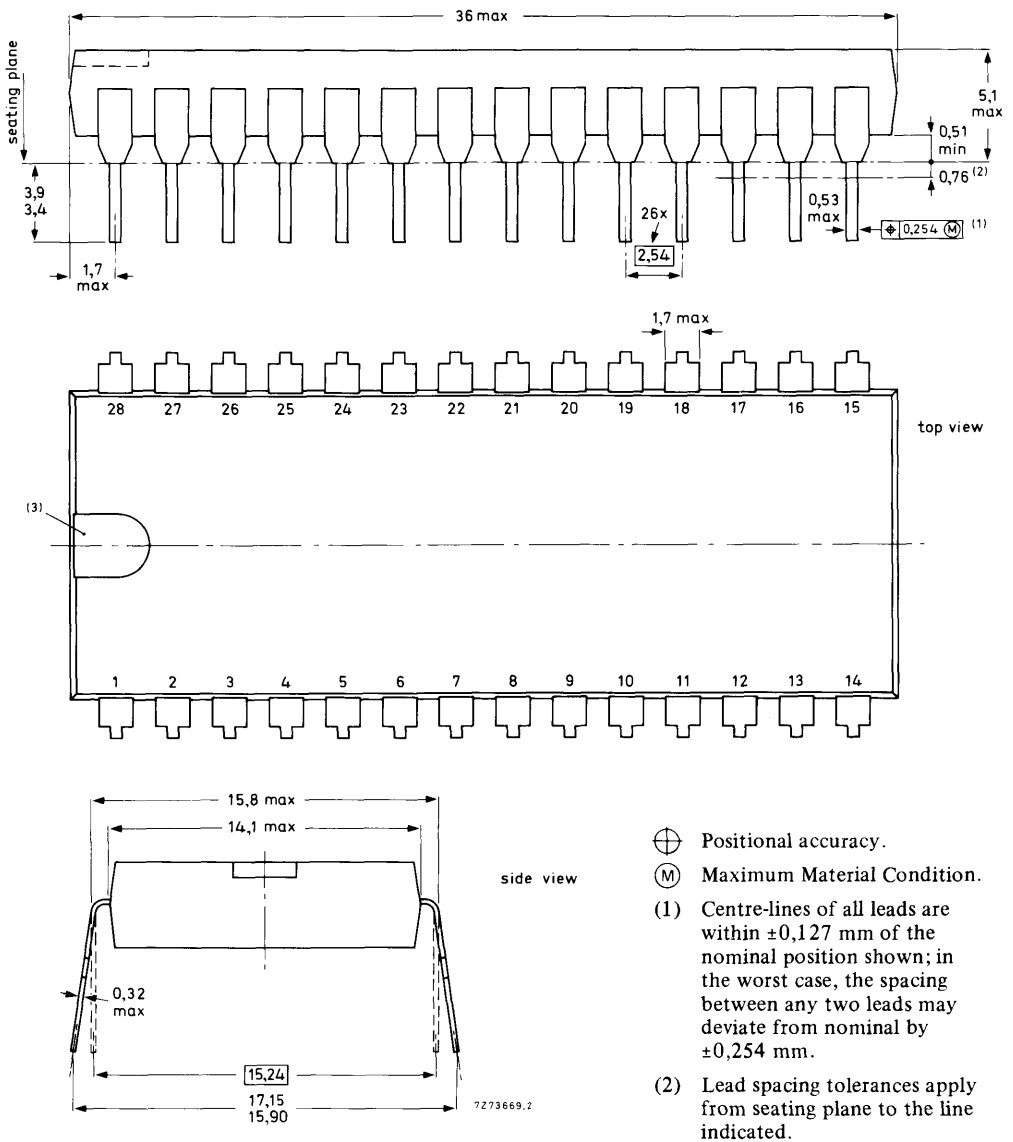
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

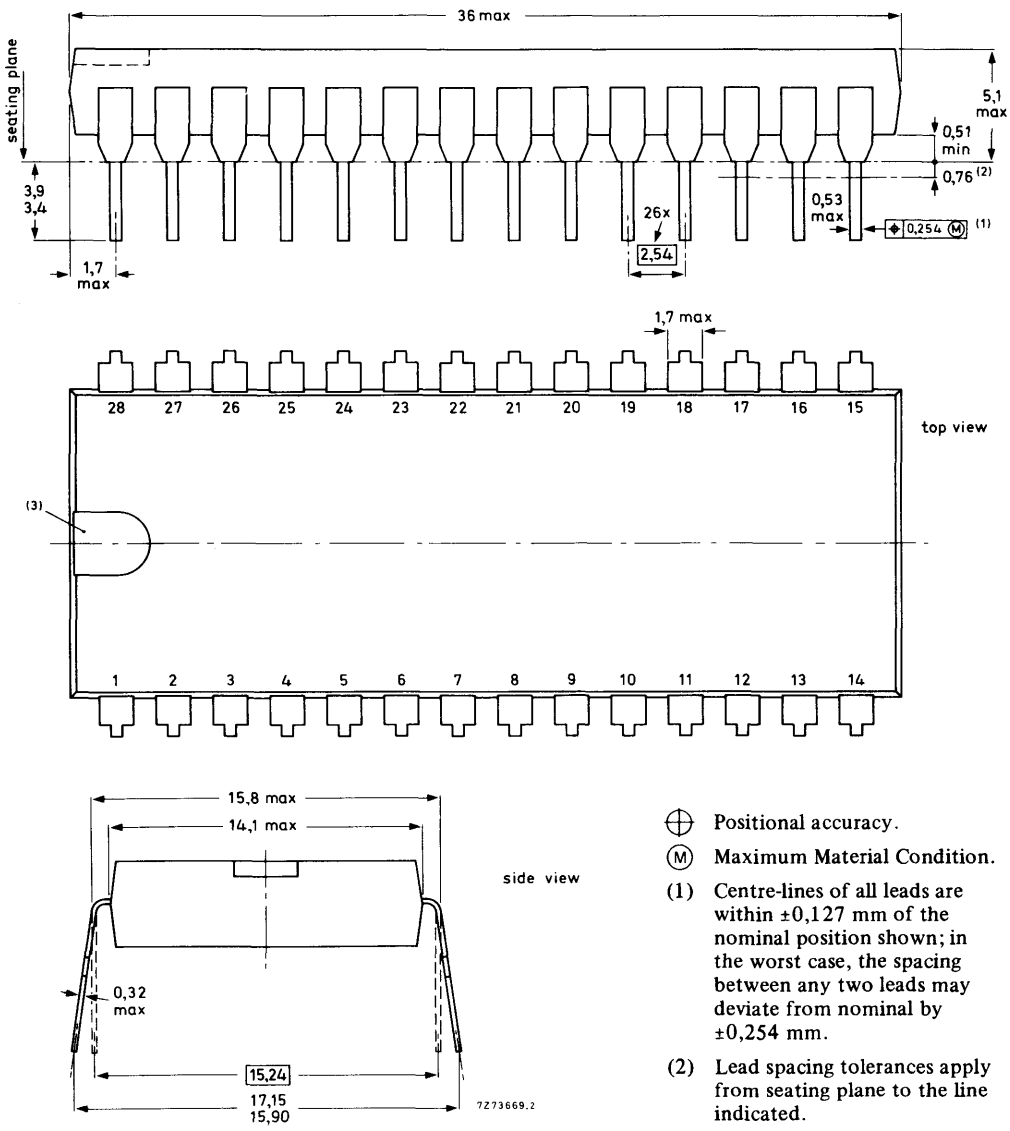
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

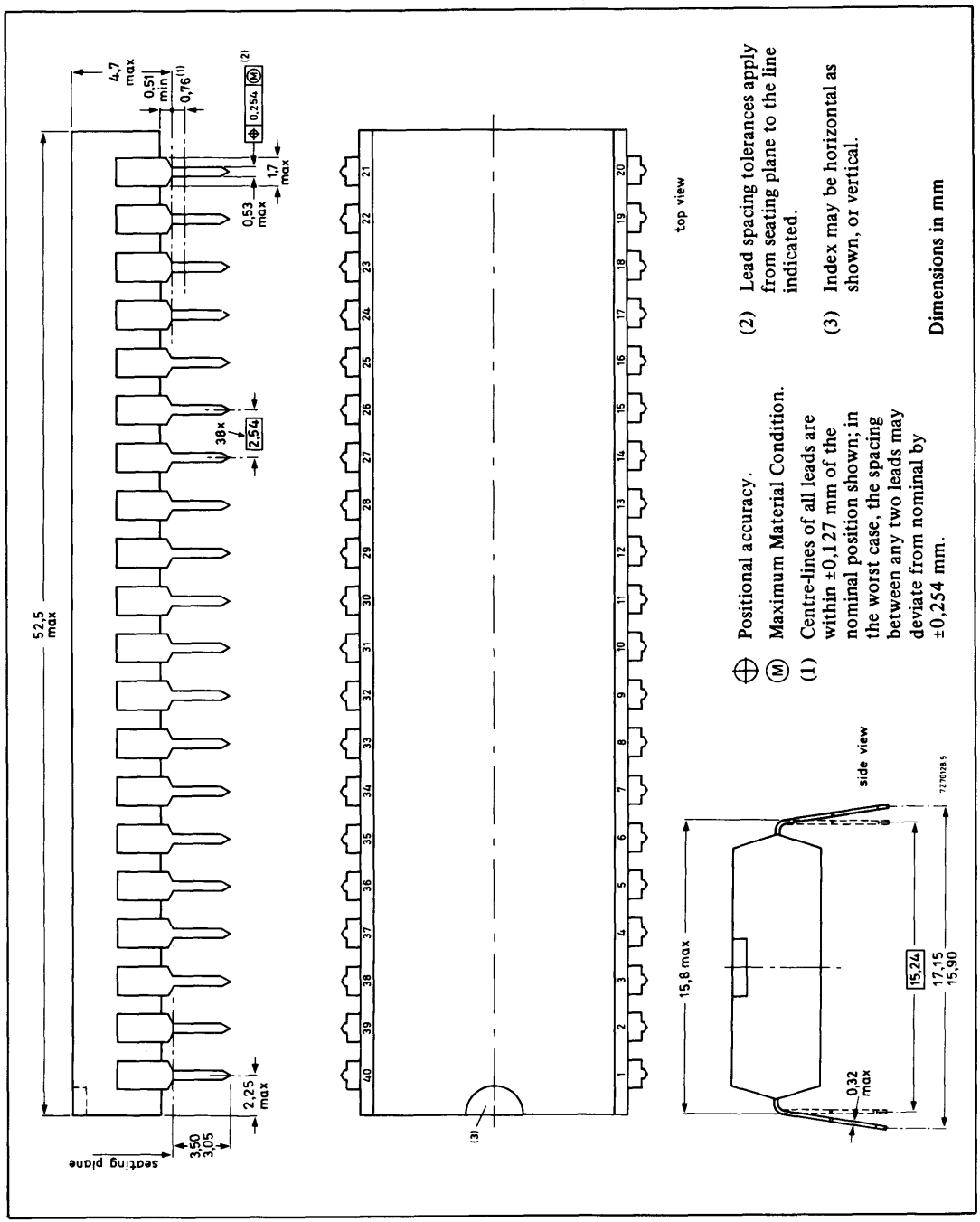
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

40-LEAD DUAL IN-LINE; PLASTIC (SOT129)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

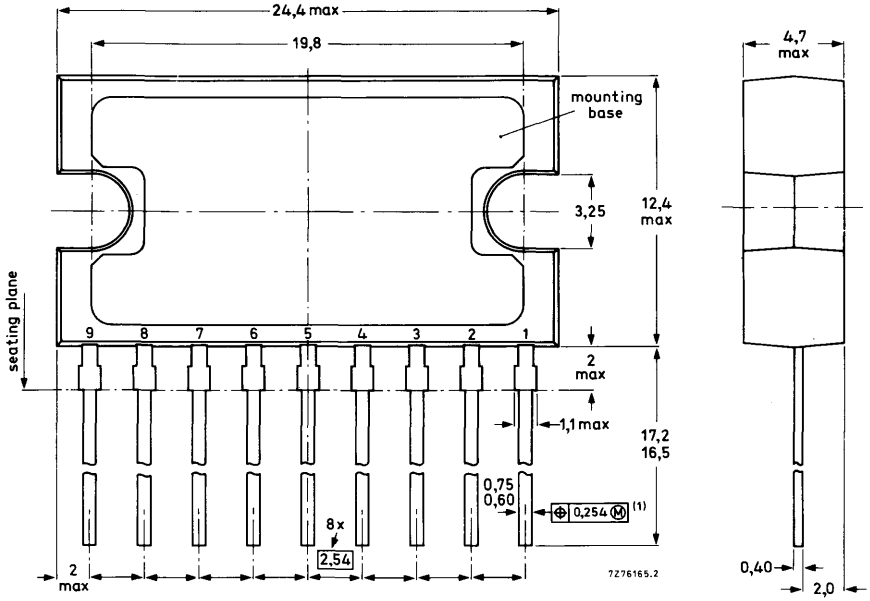
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC POWER (SOT131)



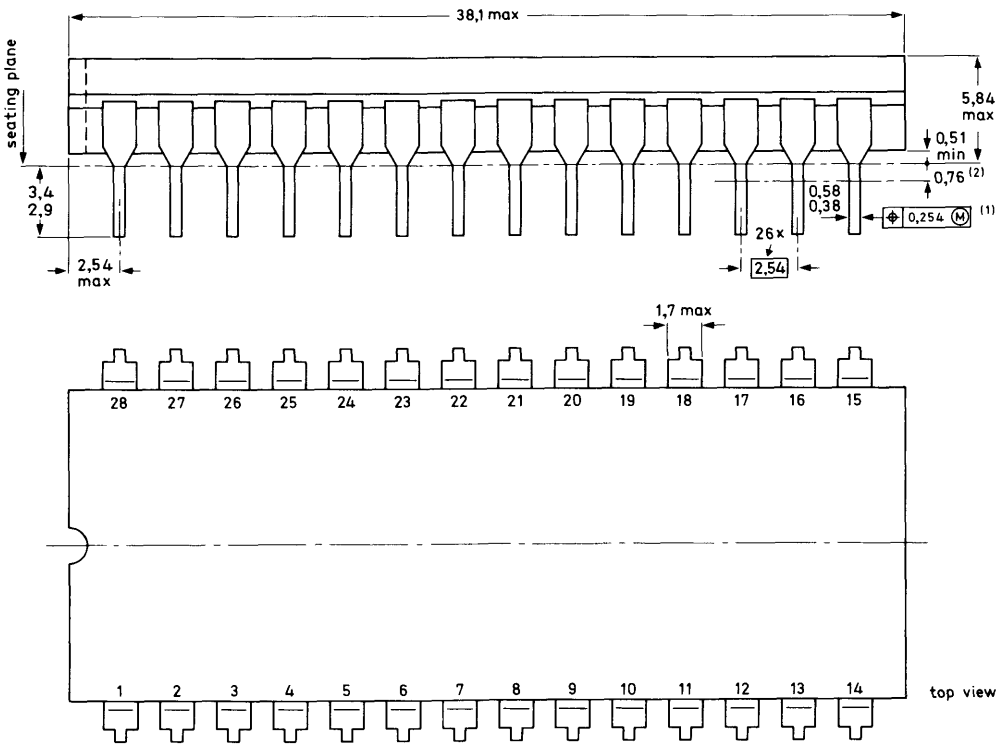
⊕ Positional accuracy.

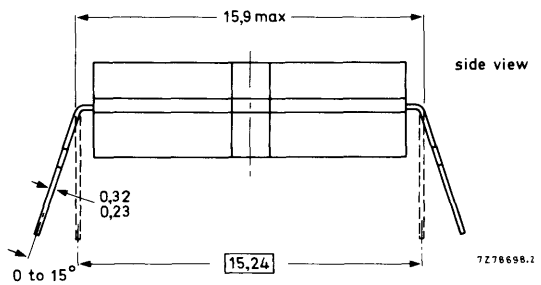
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

Dimensions in mm

28-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT135A)





⊕ Positional accuracy.

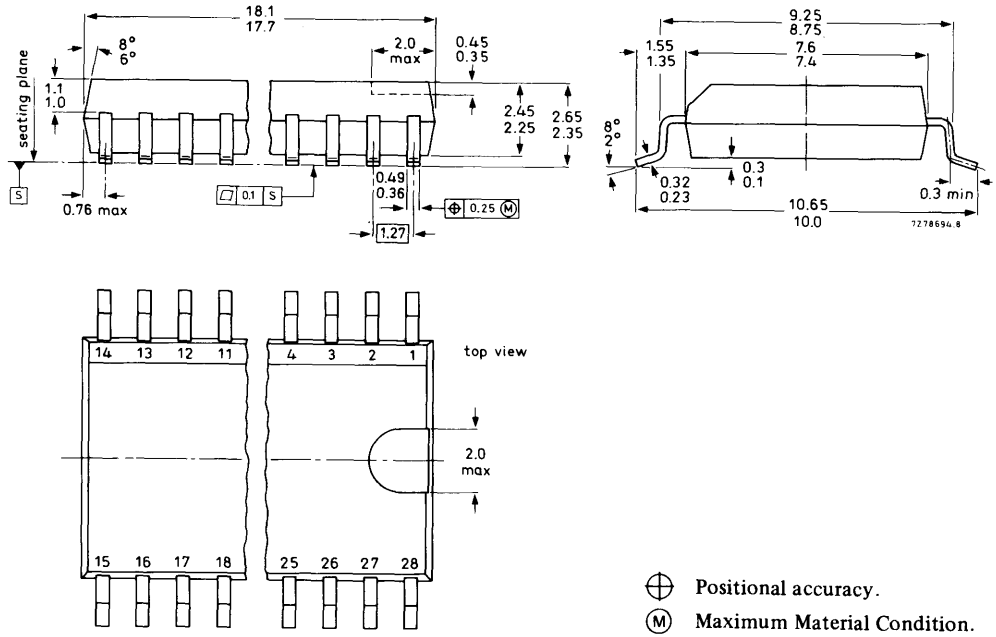
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD MINI-PACK; PLASTIC (SO28; SOT136A)

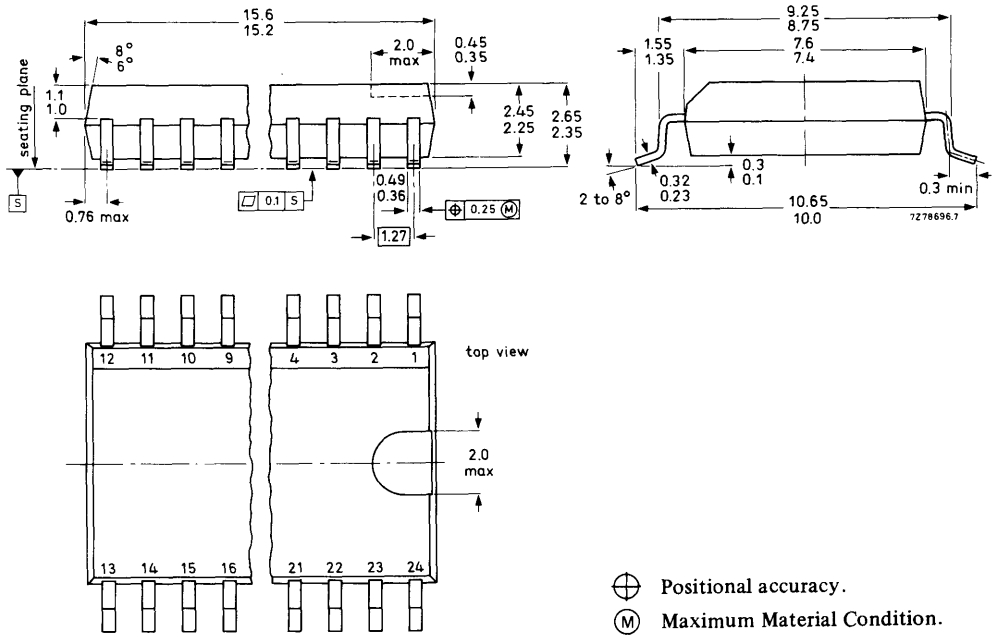


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

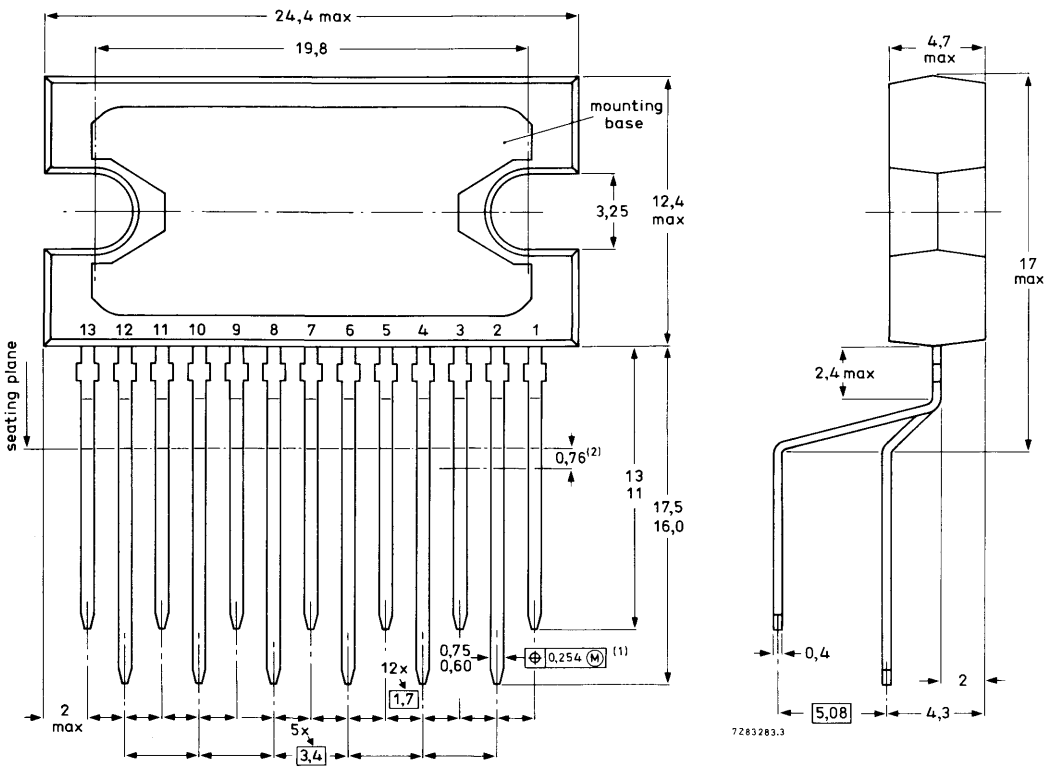
Dimensions in mm

24-LEAD MINI-PACK; PLASTIC (SO24; SOT137A)



Dimensions in mm

13-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT141B,C)



⊕ Positional accuracy.

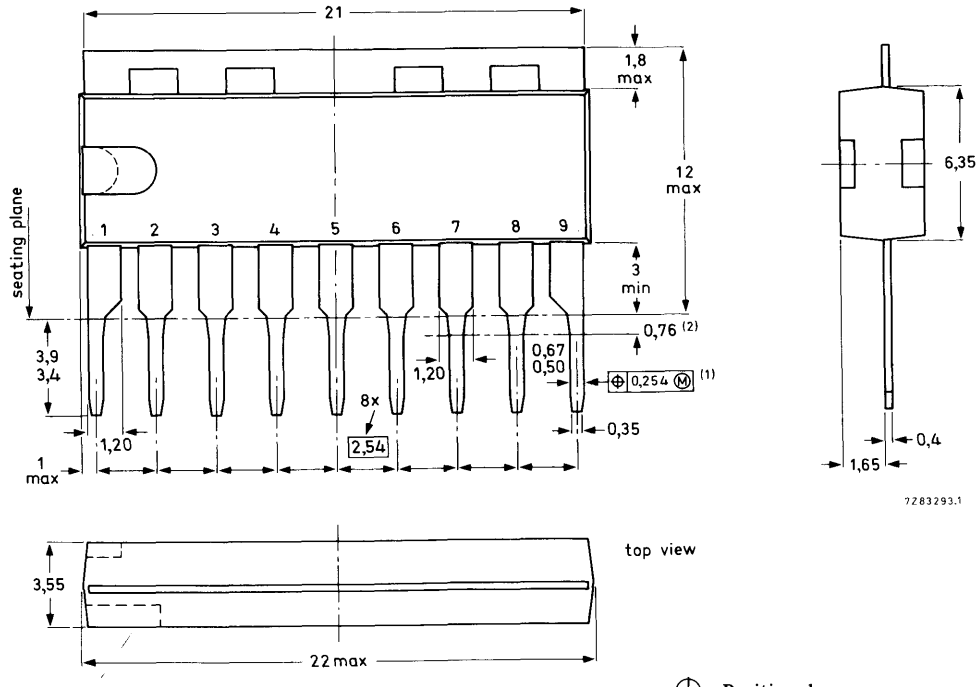
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC (SOT142)



⊕ Positional accuracy.

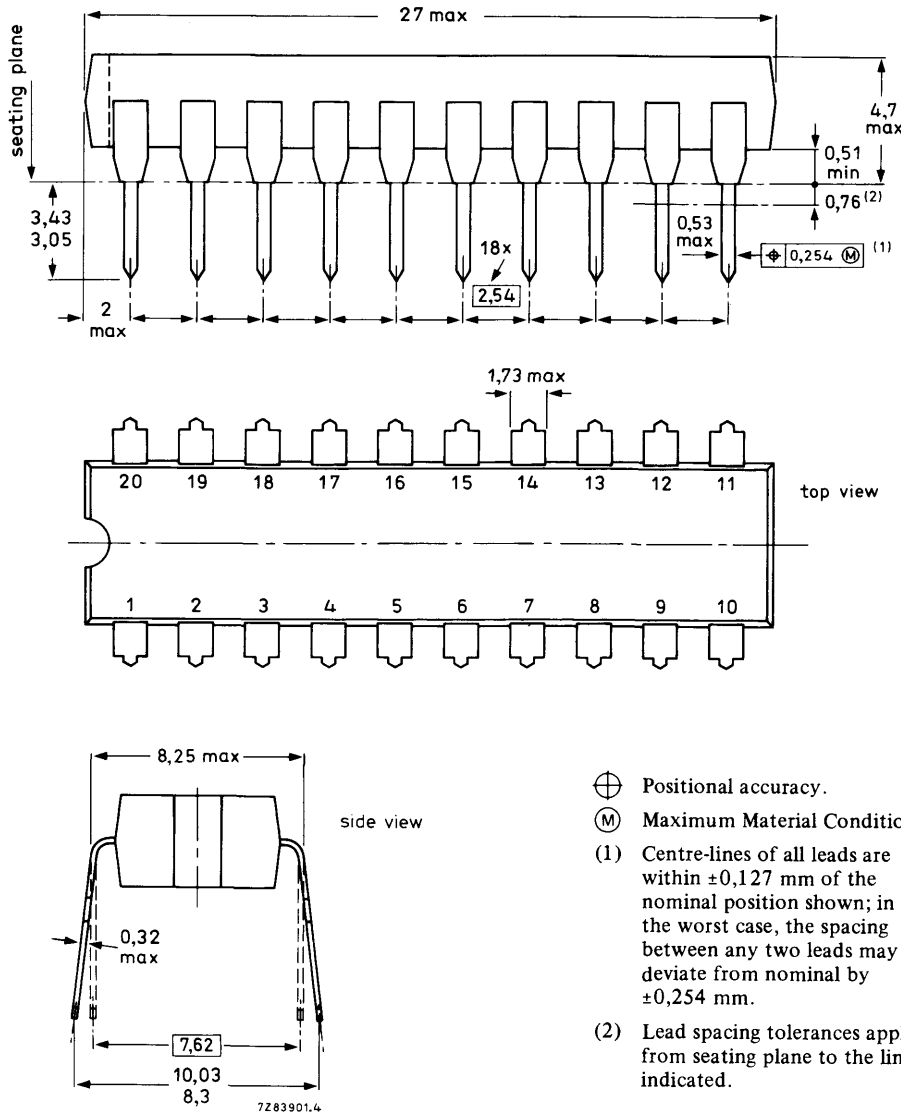
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

20-LEAD DUAL IN-LINE; PLASTIC (SOT146)



⊕ Positional accuracy.

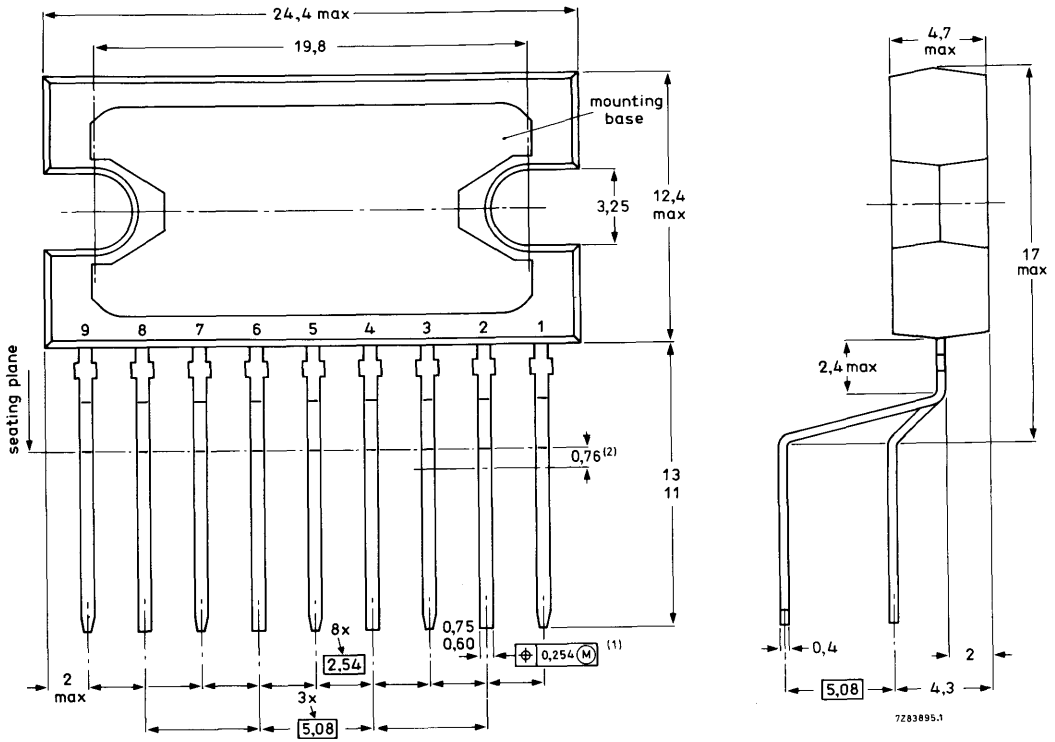
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

9-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT157)



⊕ Positional accuracy.

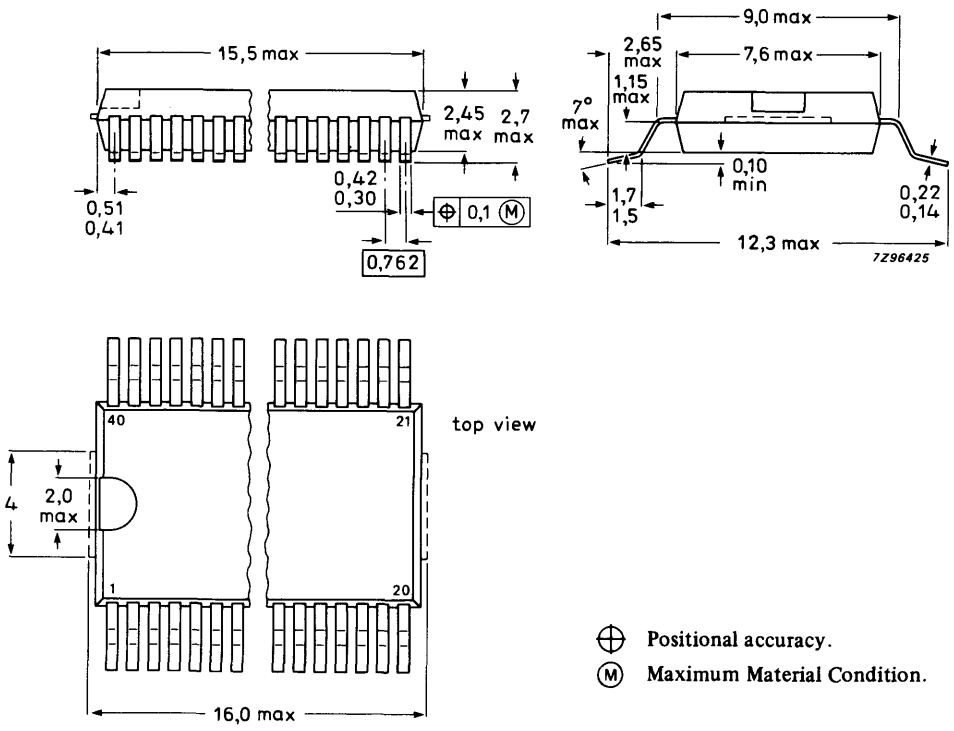
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

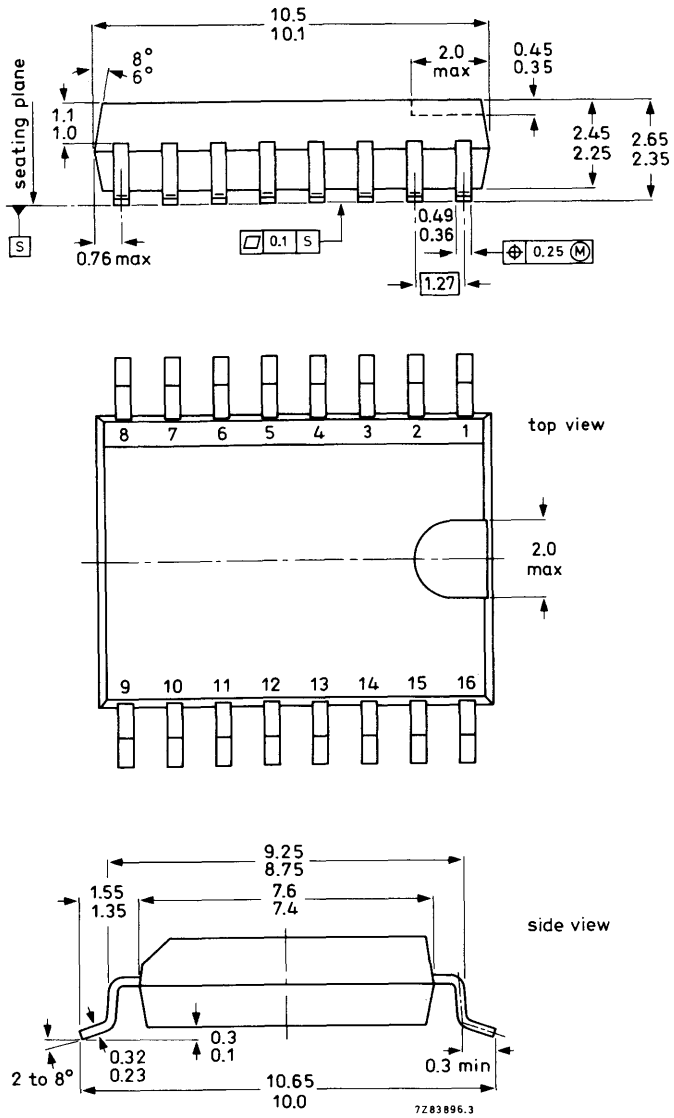
Dimensions in mm

40-LEAD MINI-PACK; PLASTIC (VSO40; SOT158A)



Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16L; SOT162A)

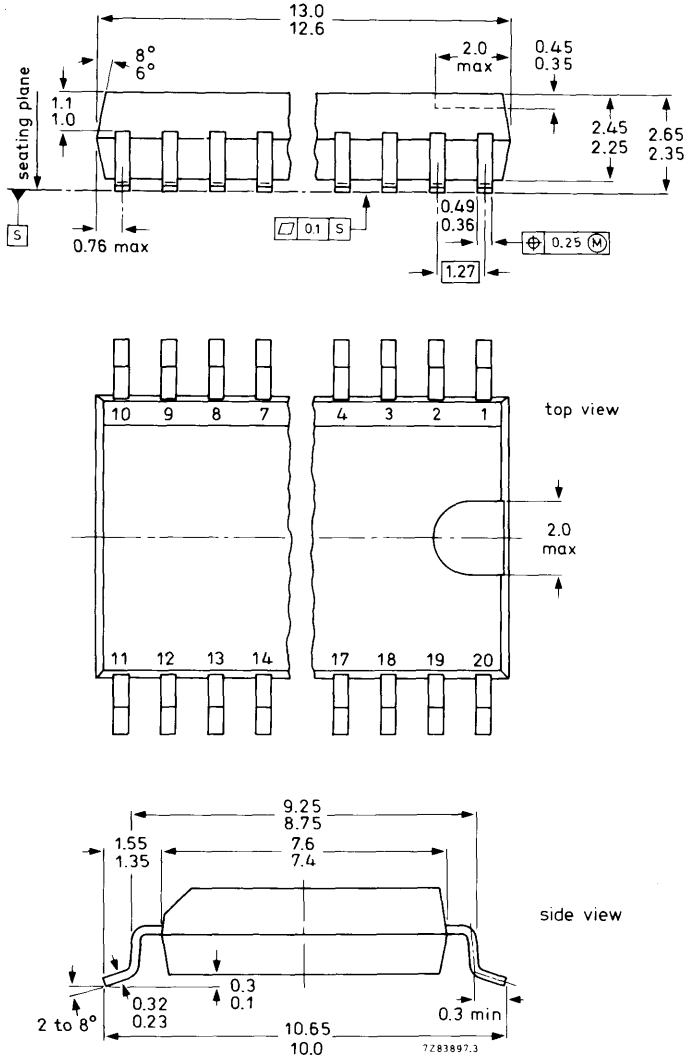


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

20-LEAD MINI-PACK; PLASTIC (SO20; SOT163A)

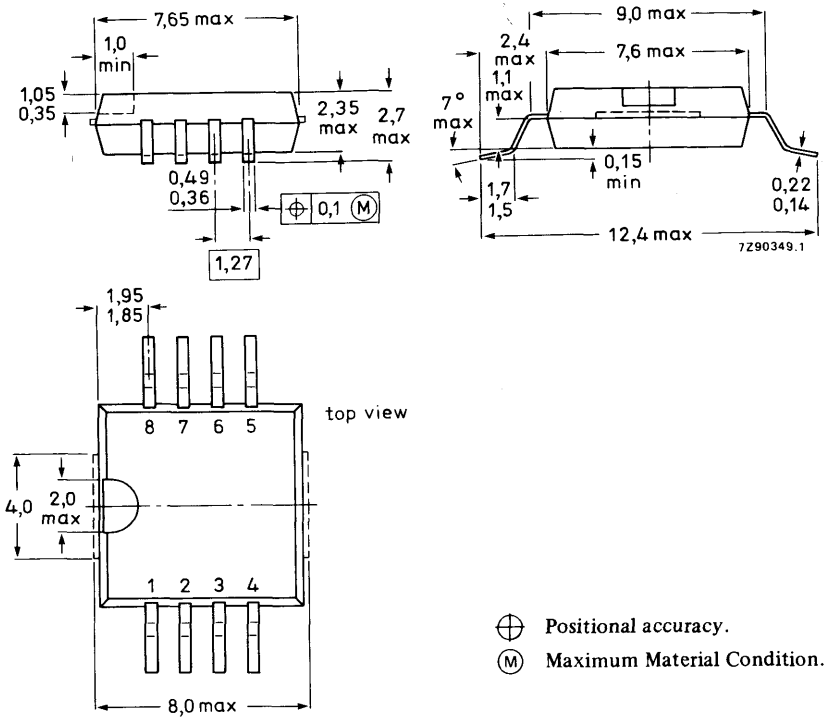


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8L; SOT176A)

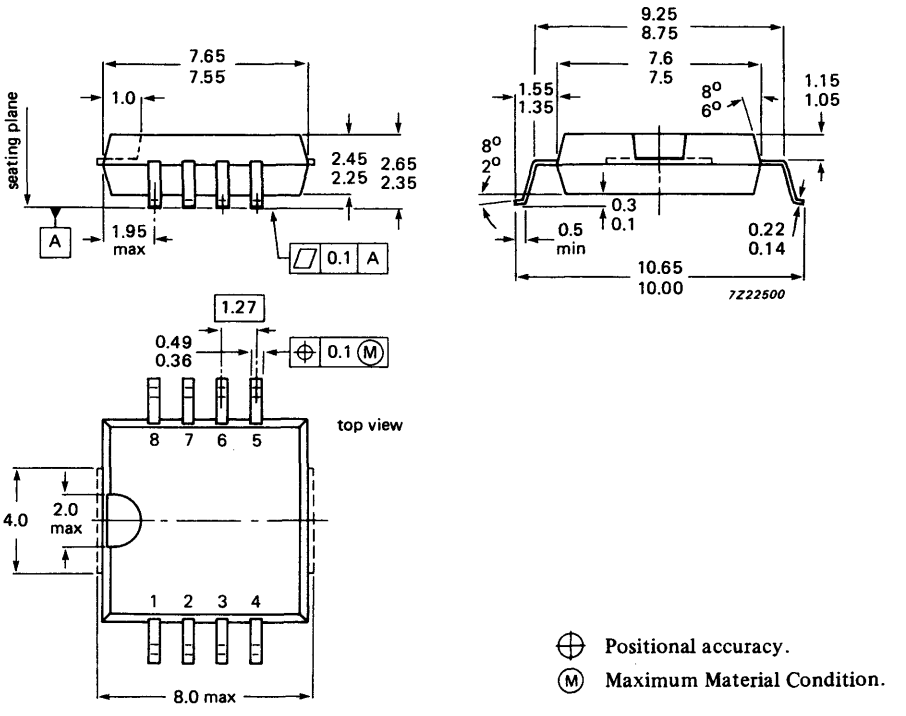


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8L; SOT176C)

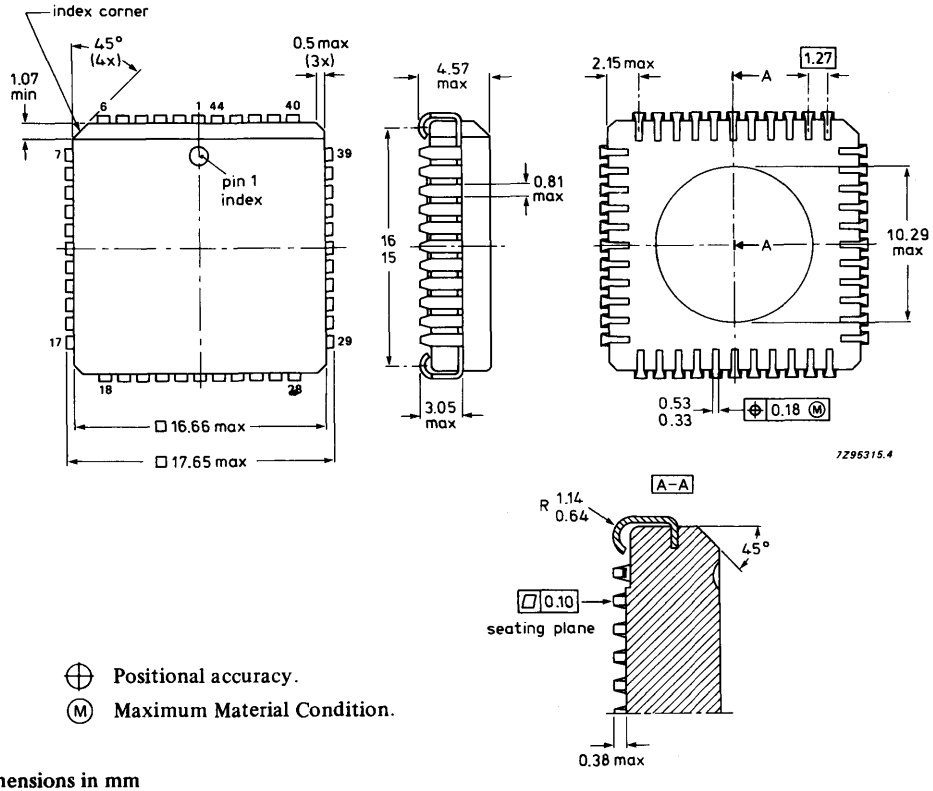


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

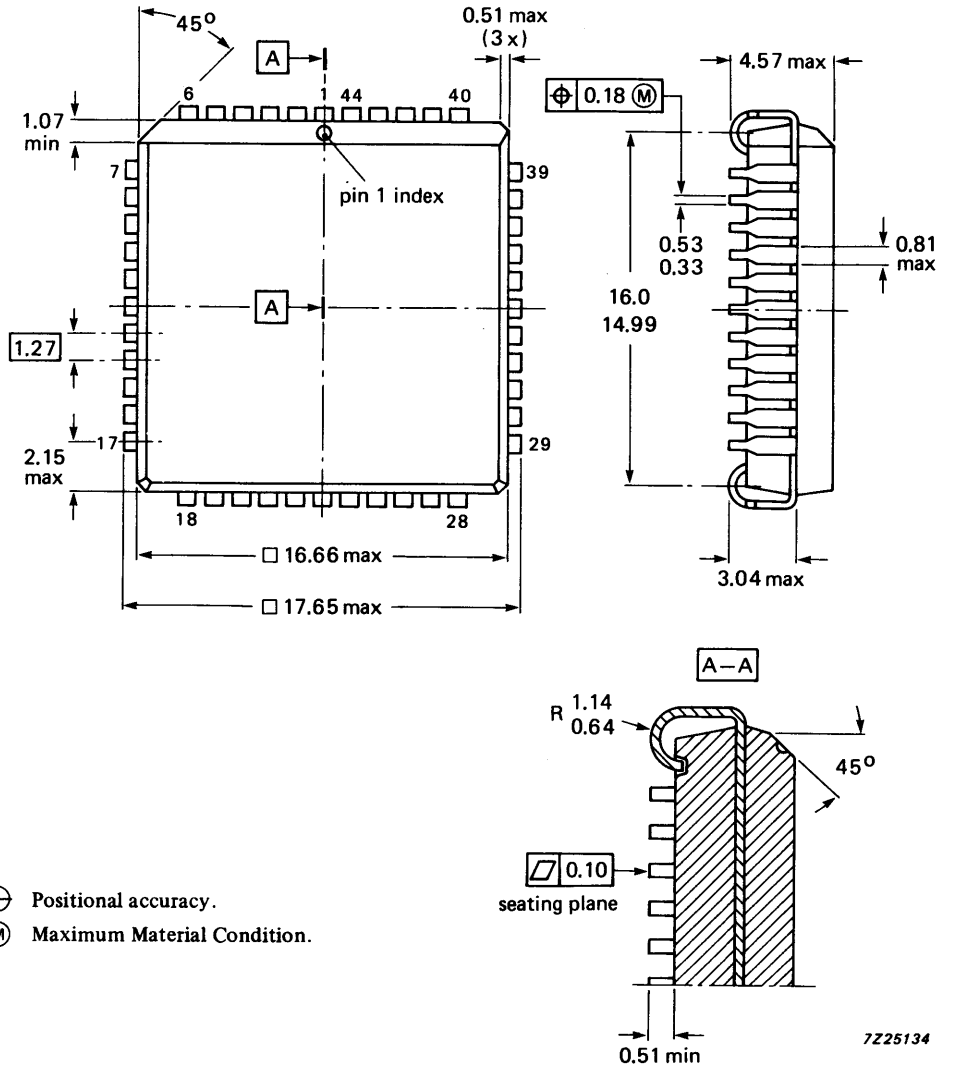
Dimensions in mm

44-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'PEDESTAL' VERSION (SOT187)



Dimensions in mm

44-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'POCKET' VERSION (SOT187AA)

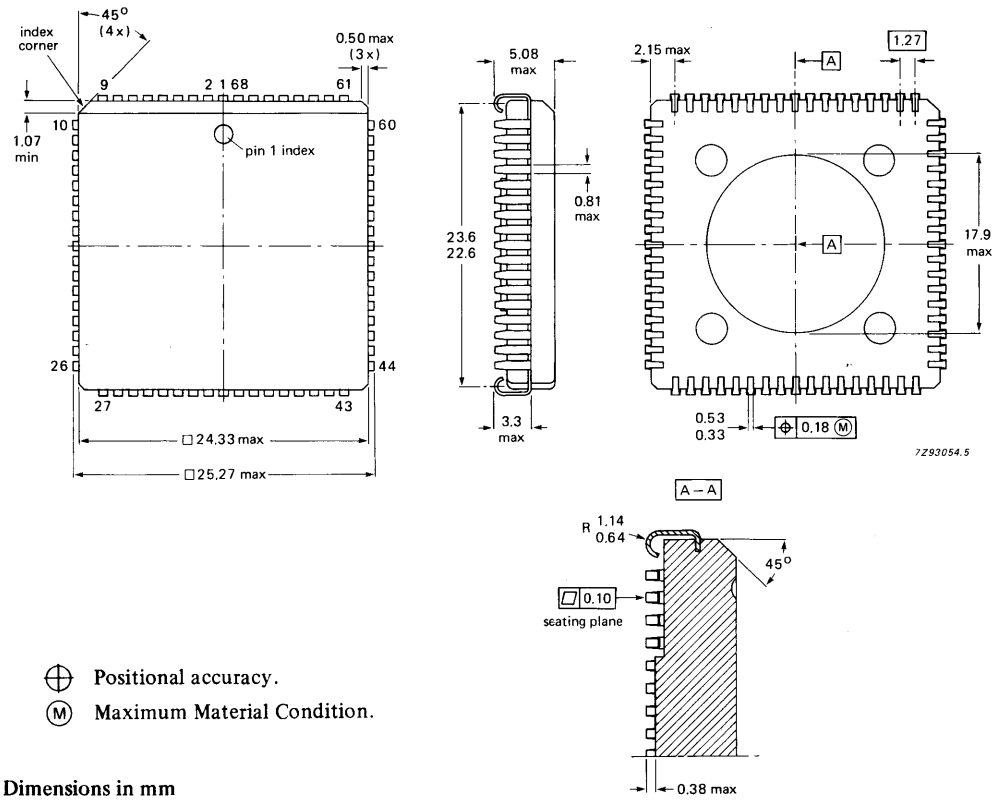


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

68-LEAD PLASTIC LEADED CHIP CARRIER (PLCC) (SOT188)

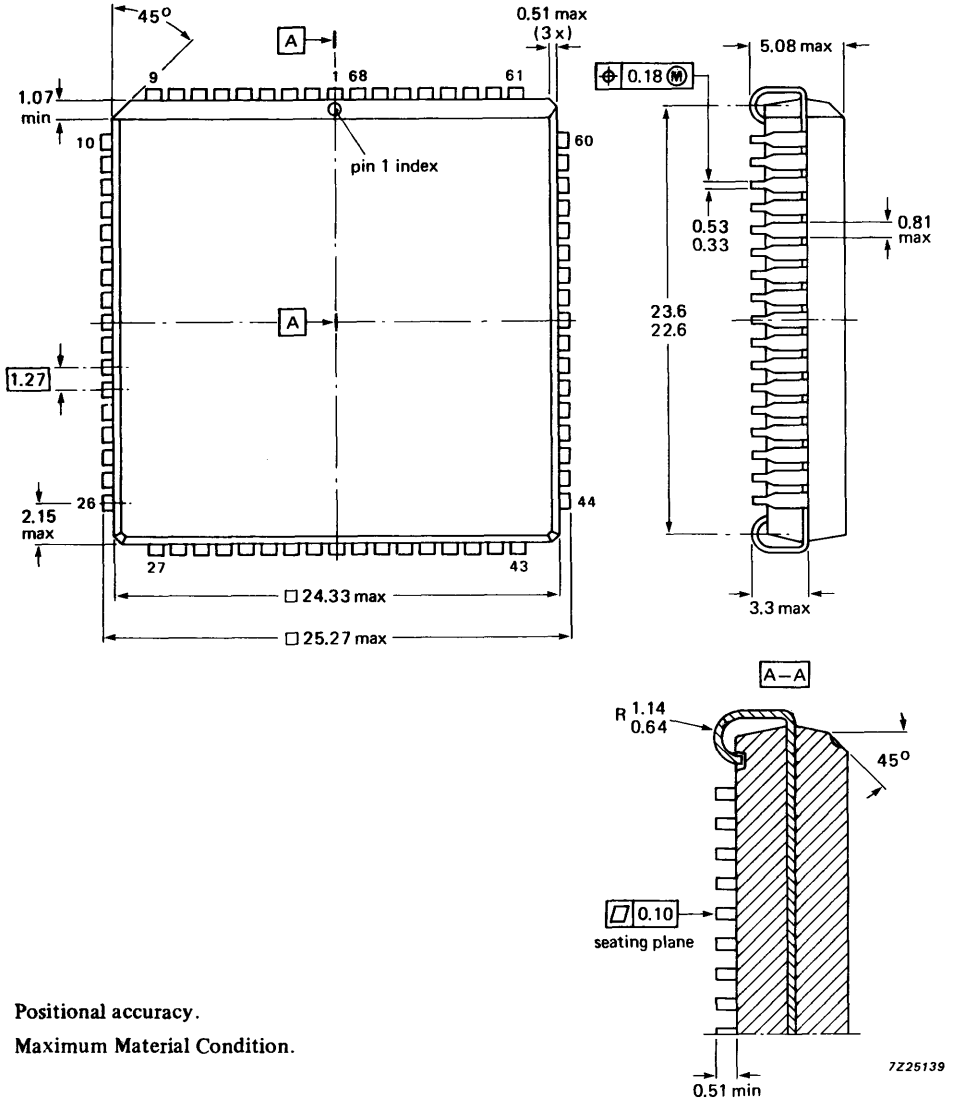


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

68-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'POCKET' VERSION (SOT188AA)

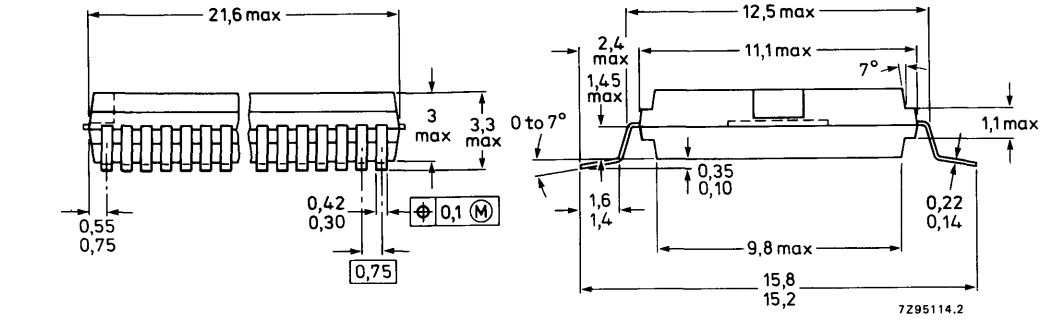


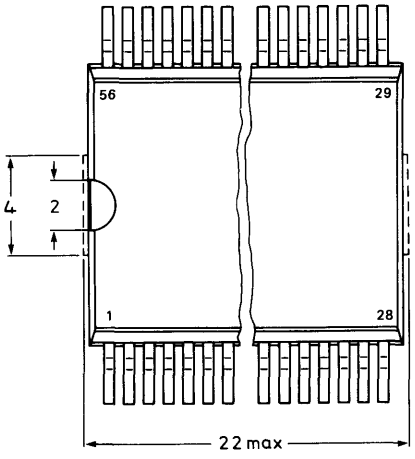
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

56-LEAD MINI-PACK; PLASTIC (VSO56; SOT190)





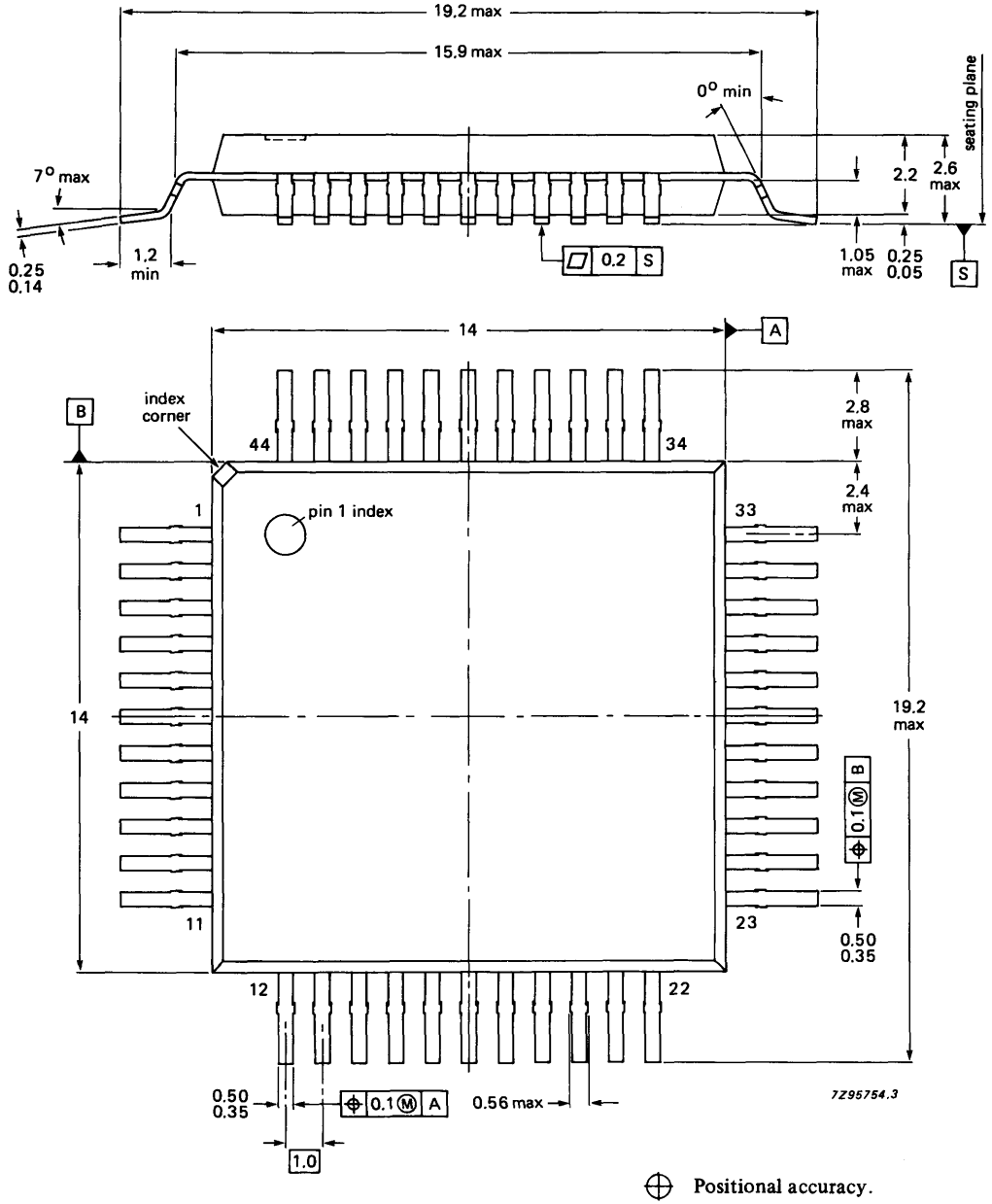
top view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

44-LEAD QUAD FLAT-PACK; PLASTIC (SOT205A)

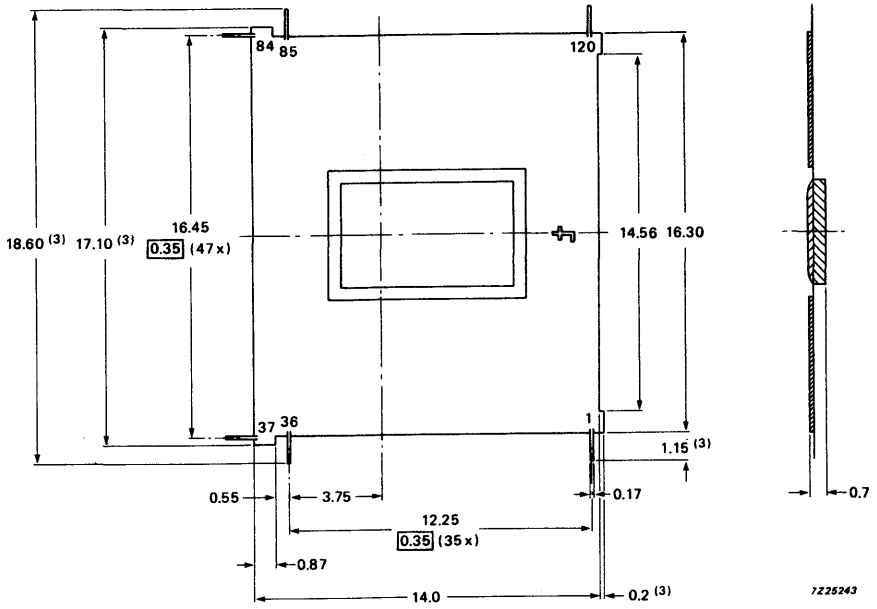


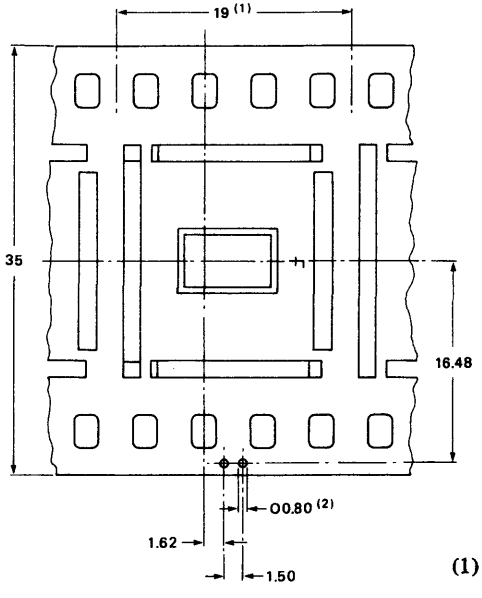
⊕ Positional accuracy.

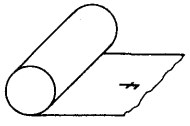
Ⓜ Maximum Material Condition.

Dimensions in mm

120-LEAD TAPE-AUTOMATED-BONDING (TAB) MODULE (SOT235)



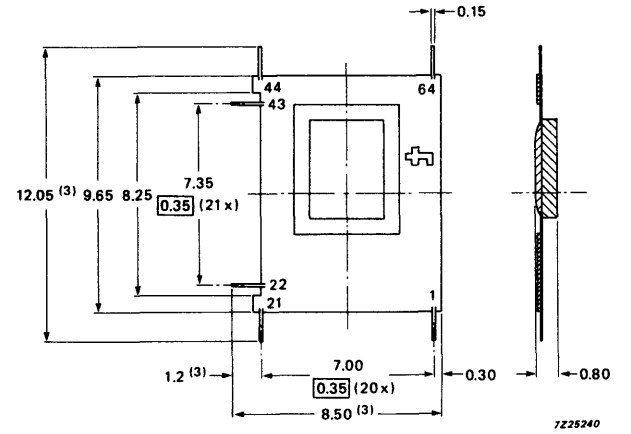


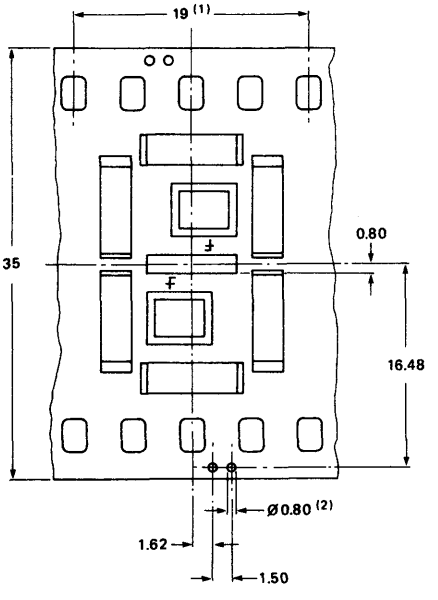


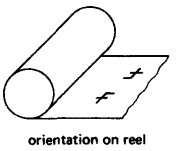
(1) 1 pattern = 4 perforation pitch intervals (contains one module)
(2) Circuit-test holes
(3) Fixed by the user

Dimensions in mm

64-LEAD TAPE-AUTOMATED-BONDING (TAB) MODULE (SOT267A,C,D)







7Z25241

(1) 1 pattern = 4 perforation pitch intervals (contains two modules)
(2) Circuit-test holes
(3) Fixed by the user

Dimensions in mm

SOLDERING

For type numbers with prefixes:
HEF, MAB, MAF, OM, PCA, PCB, PCF,
PNA, SAA, SAD, SAF, TDA, TDB, TDD, TEA and TSA

SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

SOLDERING TAB MODULES

1. Fluxing

(a) a flux that does not have to be removed,
or
(b) a water-soluble flux.

2. Soldering

The reflow soldering method using a pulse-heated soldering tool is usually suitable. Limit the soldering operation to 3 seconds at 250 °C at the leads.

3. Cleaning

Avoid cleaning if possible.

If cleaning is necessary, use cold or hot water. A detergent may be added to the water. Finally rinse with de-ionized water.

Do not use ultrasonic cleaning methods as these may damage the inner or outer leads.

Do not use solvents.

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Printed in The Netherlands (2.5M/889) © Philips Components Ltd., August 1989 9398 168 50051 Publication No. 809304B

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